# **DRC5124T** (Tentative)

### Silicon NPN epitaxial planar type

For digital circuits

#### ■ Absolute Maximum Ratings $T_a = 25$ °C

Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	V <sub>CBO</sub>	50	V
Collector-emitter voltage (Base open)	V <sub>CEO</sub>	50	V
Collector current	$I_{C}$	100	mA
Total power dissipation	P <sub>T</sub>	150	mW
Junction temperature	$T_j$	150	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C

#### ■ Package

• Code

SMini3-F2-B

- Pin Name
  - 1: Base
  - 2: Emitter
  - 3: Collector
- Marking Symbol: NH
- Internal Connection

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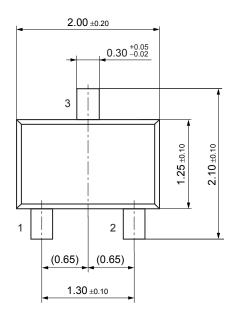
#### ■ Electrical Characteristics $T_a = 25$ °C±3°C

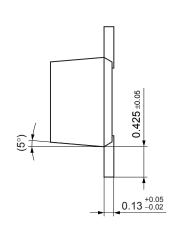
Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Collector-base voltage (Emitter open)	$V_{CBO}$	$I_C = 10 \mu A, I_E = 0$	50			V
Collector-emitter voltage (Base open)	V <sub>CEO</sub>	$I_C = 2 \text{ mA}, I_B = 0$	50			V
Collector-base cutoff current (Emitter open)	$I_{CBO}$	$V_{\rm CB} = 50 \text{ V}, I_{\rm E} = 0$			0.1	μΑ
Collector-emitter cutoff current (Base open)	I <sub>CEO</sub>	$V_{CE} = 50 \text{ V}, I_{B} = 0$			0.5	μΑ
Emitter-base cutoff current (Collector open)	$I_{EBO}$	$V_{EB} = 6 \text{ V}, I_C = 0$			0.01	mA
Forward current transfer ratio	$h_{\mathrm{FE}}$	$V_{CE} = 10 \text{ V}, I_{C} = 5 \text{ mA}$	160		460	
Collector-emitter saturation voltage	V <sub>CE(sat)</sub>	$I_C = 10 \text{ mA}, I_B = 0.5 \text{ mA}$			0.25	V
Output voltage high-level	V <sub>OH</sub>	$V_{CC} = 5 \text{ V}, V_{B} = 0.5 \text{ V}, R_{L} = 1 \text{ k}\Omega$	4.9			V
Output voltage low-level	V <sub>OL</sub>	$V_{CC} = 5 \text{ V}, V_{B} = 2.5 \text{ V}, R_{L} = 1 \text{ k}\Omega$			0.2	V
Input resistance	$R_1$		-30%	22	+30%	kΩ

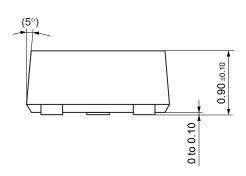
Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

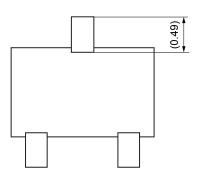
SMini3-F2-B

Unit: mm









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