Version : ***1.0***

# TECHNICAL SPECIFICATION

## MODEL NO. : PD057VU2

☐Customer's Confirmation

Customer _____

Date _____

By _____

☐PVI's Confirmation

| Dep | FAE | Panel Design | Electronic Design | Mechanical Design | Product Verification | Prepared by |
|---|---|---|---|---|---|---|
| Sign | | | | | | |

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# TECHNICAL SPECIFICATION

## CONTENTS



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## 1.Application

This data sheet applies to a color TFT LCD module, PD057VU2.
PD057VU1 module applies to OA product, car TV (must use Analog to Digital driving board), which requires high quality flat panel display. If you must use in severe reliability environment, please don't extend over PVI's reliability test conditions.

## 2. Features

. QVGA (320*240 pixels) resolution
. Amorphous silicon TFT LCD panel with back-light unit
. Pixel in stripe configuration
. Thin and light weight
. Display Colors：262,144 colors
. Optimum Viewing Direction：6 o'clock
. TTL interface

## 3.Mechanical Specifications

| Parameter | Specifications | Unit |
|---|---|---|
| Screen Size | 5.7 (diagonal) | inch |
| Display Format | 320×(R,G,B)×240 | dot |
| Display Colors | 262,144 | |
| Active Area | 115.2 (H)×86.4 (V) | mm |
| Pixel Pitch | 0.36(H)×0.36(V) | mm |
| Pixel Configuration | Stripe | |
| Outline Dimension | 143.4(W)×104.0(H)×12.7 (D) (typ.) | mm |
| Weight | 148±10 | g |
| Back-light | CCFL, 1 tube | |
| Surface treatment | Anti-glare (and wide view film) | |
| Display mode | Normally white | |

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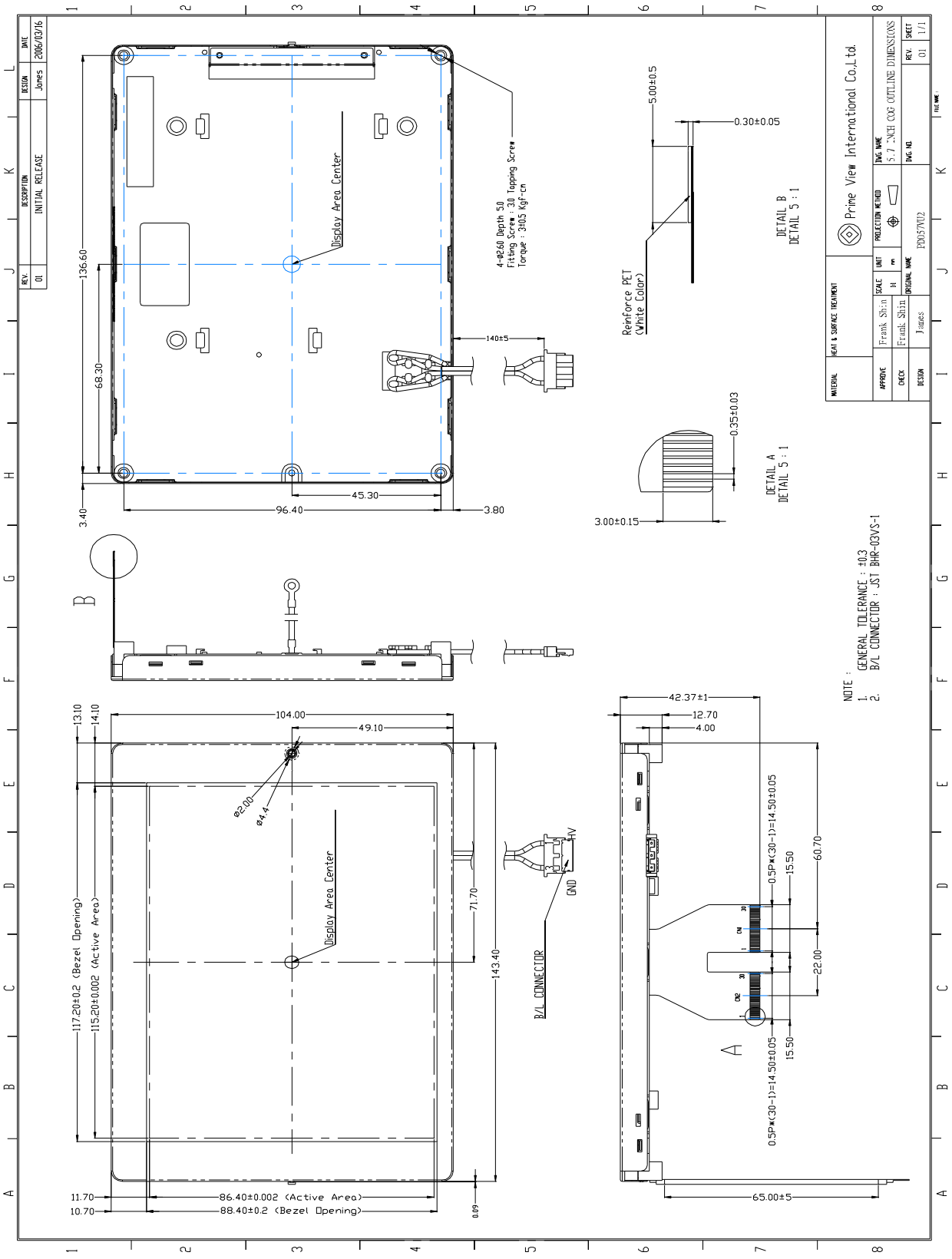
## 4.Mechanical Drawing of TFT-LCD Module

**Outline Drawing : Front View (unit : mm)**

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**5.Input / Output Terminals**

**CN1**

FPC Down Connect , 30Pins , Pitch : 0.5 mm

| Pin No | Symbol | I/O | Description | Remark |
|---|---|---|---|---|
| 1 | D13(G3) | I | Green Data | Note 5-1 |
| 2 | D12(G2) | I | Green Data | |
| 3 | D11(G1) | I | Green Data | |
| 4 | D10(G0) | I | Green Data(LSB) | |
| 5 | VDD2 | I | Analog power supply for source driver | Note 5-2 |
| 6 | V8 | I | Gamma correction voltage 8 | |
| 7 | V7 | I | Gamma correction voltage 7 | |
| 8 | V6 | I | Gamma correction voltage 6 | |
| 9 | V5 | I | Gamma correction voltage 5 | |
| 10 | V4 | I | Gamma correction voltage 4 | |
| 11 | V3 | I | Gamma correction voltage 3 | |
| 12 | V2 | I | Gamma correction voltage 2 | |
| 13 | V1 | I | Gamma correction voltage 1 | |
| 14 | VSS2 | I | Analog ground for source driver | |
| 15 | D07(R7) | I | Red Data(MSB) | Note 5-1 |
| 16 | D06(R6) | I | Red Data | |
| 17 | D05(R5) | I | Red Data | |
| 18 | D04(R4) | I | Red Data | |
| 19 | D03(R3) | I | Red Data | |
| 20 | D02(R2) | I | Red Data | |
| 21 | D01(R1) | I | Red Data | |
| 22 | D00(R0) | I | Red Data(LSB) | |
| 23 | CLK | I | Clock signal. Latching data at the rising edge | |
| 24 | HS | I | Horizontal sync input | Note 5-3 |
| 25 | VS | I | Vertical sync input | Note 5-4 |
| 26 | DEN | I | Input data enable control.(Normally pull low) | Note 5-5 |
| 27 | VCC | I | Digital power supply for source driver IC | Note 5-6 |
| 28 | VCOM | I | Voltage for common electrode | Note 5-7 |
| 29 | VEE | I | Negative power for gate driver | Note 5-8 |
| 30 | VCOM | I | Voltage for common electrode | Note 5-7 |

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**CN2**

FPC Down Connect , 30Pins , Pitch : 0.5 mm

| Pin No | Symbol | I/O | Description | Remark |
|---|---|---|---|---|
| 1 | VSS1 | I | Ground for gate driver | |
| 2 | VDD1 | I | Power supply for gate logic circuit | Note 5-9 |
| 3 | NC | - | NC | |
| 4 | VEE | I | Negative power for gate driver | Note 5-8 |
| 5 | NC | - | NC | |
| 6 | VGH | I | Positive power for gate driver | Note 5-10 |
| 7 | NC | - | NC | |
| 8 | GND | I | Digital ground for source driver IC | |
| 9 | RESETB | I | Hardware global reset, (low active) | |
| 10 | VSET | I | Externally/Internally gamma voltage setup | Note 5-11 |
| 11 | U/D | I | Up/Down control for gate driver | Note 5-12 |
| 12 | L/R | I | Left/Right control for source driver | |
| 13 | IF2 | I | Select the input data format (IF2:L,IF1:H Parallel RGB) | Note 5-13 |
| 14 | IF1 | I | | |
| 15 | SPENA | I | Serial port data enable signal (normally pull high) | |
| 16 | SPCK | I | Serial port clock. (Normally pull high) | |
| 17 | SPDA | I/O | Serial port data input/output | |
| 18 | POL | O | Polarity select for the line inversion control signal | Note 5-14 |
| 19 | D27(B7) | I | Blue Data(MSB) | Note 5-1 |
| 20 | D26(B6) | I | Blue Data | |
| 21 | D25(B5) | I | Blue Data | |
| 22 | D24(B4) | I | Blue Data | |
| 23 | D23(B3) | I | Blue Data | |
| 24 | D22(B2) | I | Blue Data | |
| 25 | D21(B1) | I | Blue Data | |
| 26 | D20(B0) | I | Blue Data(LSB) | |
| 27 | D17(G7) | I | Green Data(MSB) | |
| 28 | D16(G6) | I | Green Data | |
| 29 | D15(G5) | I | Green Data | |
| 30 | D14(G4) | I | Green Data | |

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Note 5-1 : Digital data input. DX0 is LSB and DX7 is MSB.
If parallel RGB input mode is used, D0X, D1X, and D2X indicate R, G and B data in turn.
If serial RGB or CCIR601/656 input mode is selected, only D07~D00 are used, and others short to Vss.

Note 5-2 : VDD2 Typ. = +5V.

Note 5-3 : Horizontal sync input in digital RGB mode. Or HREF input in CCIR601 mode.
( Short to Vss if not used )

Note 5-4 : Vertical sync input in digital RGB mode. Or V123 input in CCIR601 mode.
( Short to Vss if not used )

Note 5-5 : The SYNC(HS+VS) Mode and DEN mode are supported. If DEN signal is fixed low,SYNC Mode is used. Otherwise , DEN mode is used.

Note 5-6 : VCC Typ. = +3.3V.

Note 5-7 : VCOM Typ.＝+6V.

Note 5-8 : VEE Typ. = -10V.

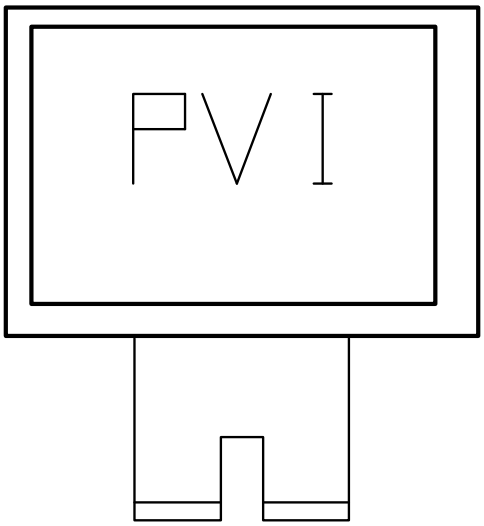
Note 5-9 : VDD1 Typ.＝+3.3V.

Note 5-10 : VGH Typ. =+15V.

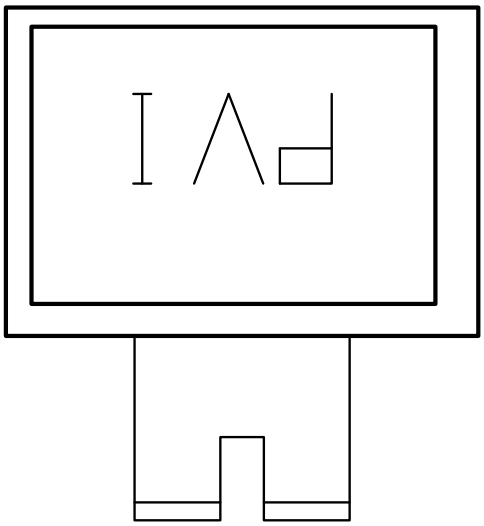
Note 5-11 :If.VSET="H",the gamma correction voltage generated externally.
VSET="L",the gamma correction voltage generated internally.

Note 5-12 : The definition of L/R , U/D

U/D(PIN 11)=Low L/R(PIN 12)=High



U/D(PIN 11)=High L/R(PIN 12)=Low



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Note 5-13 : IF1,IF2 control the input data format.

| IF2,IF1 | Input data format |
|---|---|
| L,L (default) | Serial RGB |
| L,H | Parallel RGB |
| H,L | CCIR601 |
| H,H | CCIR656 |

Note 5-14 : When POL=L, output voltage is negative polarity.
When POL=H, output voltage is positive polarity.

## 6. Absolute Maximum Ratings

VSS1=VSS2=0 V，Ta = 25 ℃

| Parameter | | Symbol | MIN. | MAX. | Unit | Remark |
|---|---|---|---|---|---|---|
| Supply voltage for source driver | | VCC | -0.3 | +7.0 | V | |
| | | VDD2 | -0.3 | +7.0 | V | |
| Supply voltage for gate driver | | VDD1 | -0.3 | +7.0 | V | |
| | H Level | VGH | -0.3 | +32.0 | V | |
| | L Level | VEE | -22.0 | +0.3 | V | |
| | | VGH-VEE | -0.3 | +45.0 | V | |
| Input signal voltage | | VIN | -0.3 | VDD+0.3 | V | |

## 7. Electrical Characteristics

7-1 Operating condition

VSS1=VSS2=0 V，Ta = 25 ℃

| Parameter | | Symbol | MIN. | Typ. | MAX. | Unit | Remark |
|---|---|---|---|---|---|---|---|
| Supply voltage for source driver | Logic | VCC | +3.0 | +3.3 | +3.6 | V | |
| | Analog | VDD2 | - | +5.0 | - | V | |
| Supply voltage for gate driver | Logic | VDD1 | +3.0 | +3.3 | +3.6 | V | |
| | H level | VGH | - | +15 | - | V | |
| | L level | VEE | - | -10 | - | V | |
| Signal input voltage | H level | VIH | 0.7V | - | VCC | V | |
| | L level | VIL | 0 | - | 0.3VCC | V | |
| Signal output voltage | H level | VoH | 0.8V | - | VCC | V | |
| | L level | VoL | 0 | - | 0.2VCC | V | |
| VCOM | | VCOMAC | - | 6 | - | $V_{P-P}$ | AC Component of VCOM |
| | | VCOMDC | - | 1.8 | - | V | DC Component of VCOM Note 7-1 |

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Note 7-1 : PVI strongly suggests that the VCOMDC level shall be adjustable , and the adjustable level range is 1.8V±1V , every module's VCOMDC level shall be carefully adjusted to show a best image performance.

**7-2) Recommended Driving Condition for Back Light** Ta=25℃

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| Lamp Voltage | $V_L$ | 760 | 710 | 660 | Vrms | $I_L$=5mA |
| Lamp Current | $I_L$ | 4 | 5 | 8 | mA | Note 7-2 |
| Lamp Frequency | $P_L$ | - | 35 | - | KHz | Note 7-3 |
| Starting Voltage (25℃) (Reference Value) | Vs | - | - | 1240 | Vrms | Note 7-4 |
| Starting Voltage (0℃) (Reference Value) | Vs | - | - | 1380 | Vrms | Note 7-4 |

Note 7-2：In order to have proper operation of the B/L, no matter what kind of inverters, the output lamp current must be between Min. and Max. values to avoid the abnormal display image caused by B/L.

Note 7-3：The driving frequency of the lamp may interfere with the horizontal synch signal, leaving interference stripes on the display. So please evaluate LCD panels beforehand.

To avoid interference stripes, we recommend to separate as far as possible the lamp frequency from the horizontal synchronous signal and its high harmonic frequency.

The inverter which PVI uses is TAD347-1.

Note 7-4：The "Starting Voltage" means the minimum voltage of inverter to turn on the lamp. And it should be applied to the lamp for more than 1 second to start up. Otherwise the lamp may not be turned on.

Backlight driving connector : JST BHR-03VS-1 , 3 Pins , Pitch：4 mm

| Pin No | Symbol | Description | Remark |
|---|---|---|---|
| 1 | VL1 | Input terminal (Hi voltage side) | |
| 2 | NC | No Connection | |
| 3 | VL2 | Input terminal (Low voltage side) | Note 7-5 |

Note 7-5：Low voltage side of backlight inverter connects with ground of inverter circuits.

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**7-3) Power Consumption**

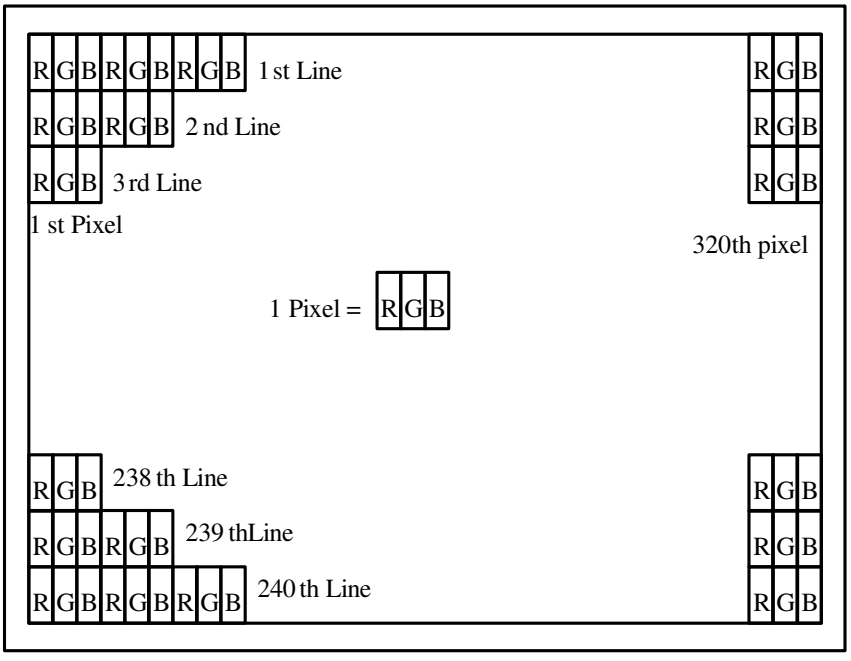
| Parameter | Symbol | Conditions | TYP. | MAX. | Unit | Remark |
|---|---|---|---|---|---|---|
| Supply current for gate driver (Hi level) | $I_{GH}$ | $V_{GH}$ =+15V | 0.048 | 0.055 | mA | |
| Supply current for gate driver (Logic) | $I_{DD1}$ | $V_{DD1}$=+3.3V | 0.0016 | 0.0017 | mA | |
| Supply current for gate driver (Low level) | $I_{EE}$ | $V_{EE}$ =-10V | 0.05 | 0.06 | mA | |
| Supply current for source driver (Analog) | $I_{DD2}$ | $V_{DD2}$=+5V | 4.95 | 5.55 | mA | |
| Supply current for source driver (Logic) | $I_{CC}$ | $V_{CC}$=+3.3V | 2.3 | 2.5 | mA | |
| LCD panel power consumption | - | - | 34 | 40 | mW | Note 7-6 |
| Backlight power consumption | - | - | 3550 | 3910 | mW | Note 7-7 |

Note 7-6：The power consumption for back light is not included.

Note 7-7：Back light lamp power consumption is calculated by $I_L \times V_L$.

**8. Pixel Arrangement**

The LCD module pixel arrangement is stripe configuration.

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**9. Display Color and Gray Scale Reference**

| Color | | Input Color Data | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Red | | | | | | | | Green | | | | | | | | Blue | | | | | | | |
| | | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | G7 | G6 | G5 | G4 | G3 | G2 | G1 | G0 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Basic Colors | Black | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Cyan | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Magent | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Yellow | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | White | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Red | Red | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Darker | | | | | | | | | | | | | | | | | | | | | | | | |
| | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| | Brighter | | | | | | | | | | | | | | | | | | | | | | | | |
| | Red | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Green | Green | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Darker | | | | | | | | | | | | | | | | | | | | | | | | |
| | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| | Brighter | | | | | | | | | | | | | | | | | | | | | | | | |
| | Green | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Blue | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | Darker | | | | | | | | | | | | | | | | | | | | | | | | |
| | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| | Brighter | | | | | | | | | | | | | | | | | | | | | | | | |
| | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

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## 10. SPI Register Description and Timing Characteristics

10.1 Function Control Register

**Register R0 :Address(A3~A0)→0000**

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | STHD1 | STHD0 | STHP4 | STHP3 | STHP2 | STHP1 | STHP0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

STHD [1:0] : adjust start pulse position by dot

| STHD1 | STHD0 | STH position adjust by dot |
|---|---|---|
| 1 | 1 | -1 |
| 1 | 0 | -2 |
| 0 | 0 | 0 |
| 0 | 1 | +1 |

STHP [4:0] : adjust start pulse position by pixel

| STHP4 | STHP3 | STHP2 | STHP1 | STHP0 | STH position adjust by pixel |
|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | -1 |
| 1 | 1 | 1 | 1 | 0 | -2 |
| 1 | 1 | 1 | 0 | 1 | -3 |
| 1 | 1 | 1 | 0 | 0 | -4 |
| 1 | 1 | 0 | 1 | 1 | -5 |
| 1 | 1 | 0 | 1 | 0 | -6 |
| 1 | 1 | 0 | 0 | 1 | -7 |
| 1 | 1 | 0 | 0 | 0 | -8 |
| 1 | 0 | 1 | 1 | 1 | -9 |
| 1 | 0 | 1 | 1 | 0 | -10 |
| 1 | 0 | 1 | 0 | 1 | -11 |
| 1 | 0 | 1 | 0 | 0 | -12 |
| 1 | 0 | 0 | 1 | 1 | -13 |
| 1 | 0 | 0 | 1 | 0 | -14 |
| 1 | 0 | 0 | 0 | 1 | -15 |
| 1 | 0 | 0 | 0 | 0 | -16 |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | +1 |
| 0 | 0 | 0 | 1 | 0 | +2 |
| 0 | 0 | 0 | 1 | 1 | +3 |
| 0 | 0 | 1 | 0 | 0 | +4 |
| 0 | 0 | 1 | 0 | 1 | +5 |
| 0 | 0 | 1 | 1 | 0 | +6 |
| 0 | 0 | 1 | 1 | 1 | +7 |
| 0 | 1 | 0 | 0 | 0 | +8 |
| 0 | 1 | 0 | 0 | 1 | +9 |
| 0 | 1 | 0 | 1 | 0 | +10 |
| 0 | 1 | 0 | 1 | 1 | +11 |
| 0 | 1 | 1 | 0 | 0 | +12 |
| 0 | 1 | 1 | 0 | 1 | +13 |
| 0 | 1 | 1 | 1 | 0 | +14 |
| 0 | 1 | 1 | 1 | 1 | +15 |

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**Register R1 :Address(A3~A0)→0001**

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Name | STVP3 | STVP2 | STVP1 | STVP0 | STVNT1 | STVNT0 | STVPAL1 | STVPAL0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

STVP [3:0] : adjust first line position by line

| STVP3 | STVP2 | STVP1 | STVP0 | STV position adjust by line |
|---|---|---|---|---|
| 1 | 1 | 1 | 1 | -1 |
| 1 | 1 | 1 | 0 | -2 |
| 1 | 1 | 0 | 1 | -3 |
| 1 | 1 | 0 | 0 | -4 |
| 1 | 0 | 1 | 1 | -5 |
| 1 | 0 | 1 | 0 | -6 |
| 1 | 0 | 0 | 1 | -7 |
| 1 | 0 | 0 | 0 | -8 |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | +1 |
| 0 | 0 | 1 | 0 | +2 |
| 0 | 0 | 1 | 1 | +3 |
| 0 | 1 | 0 | 0 | +4 |
| 0 | 1 | 0 | 1 | +5 |
| 0 | 1 | 1 | 0 | +6 |
| 0 | 1 | 1 | 1 | +7 |

STVNT[1:0]: When NTSC mode, the relationship of first line in Even field and Odd field.
00: First line in Even field = First line in Odd field.
01: First line in Even field = First line in Odd field +1.
10: No use.
11: First line in Even field = First line in Odd field –1.

STVPAL[1:0]: When PAL mode, the relationship of first line in Even field and Odd field.
(Only for CCIR601/656 mode)
00: First line in Even field = First line in Odd field.
01: First line in Even field = First line in Odd field +1.
10: No use.
11: First line in Even field = First line in Odd field –1.

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**Register R2 :Address(A3~A0)→0010**

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Name | reserved | reserved | reserved | reserved | HS_POL | VS_POL | NPC_IN | NPC_SET |
| Default | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |

HS_POL: HS polarity setting.

HS_POL = “L”, negative polarity.

HS_POL = “H”, positive polarity.

VS_POL: VS polarity setting.

VS_POL = “L”, negative polarity.

VS_POL = “H”, positive polarity.

NPC_IN: Define the NTSC/PAL mode by SPI.

NPC_IN = “L”, PAL. (Only for CCIR601/656 mode)

NPC_IN = “H”, NTSC.

NPC_SET: Set the NTSC/PAL auto detection or define by NPC_IN.

NPC_SET = “L”, auto detection.

NPC_SET = “H”, define by SPI.

**Register R3 :Address(A3~A0)→0011**

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Name | Reserved | Reserved | Reserved | Reserved | PWD_EN | Reserved | Reserved | Reserved |
| Default | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |

PWD_EN: Set DAC power saving function.

PWD_EN = “L”, disable. The DAC is always power on.

PWD_EN = “H”, enable.

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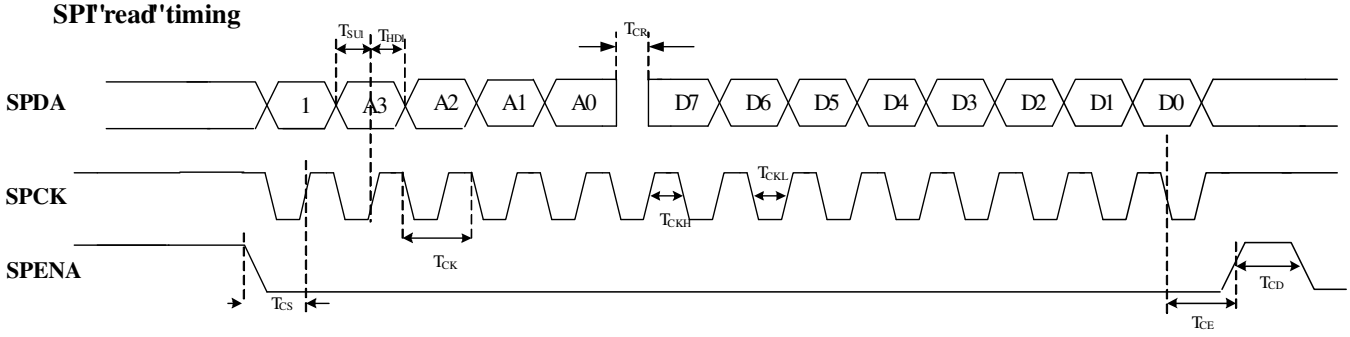
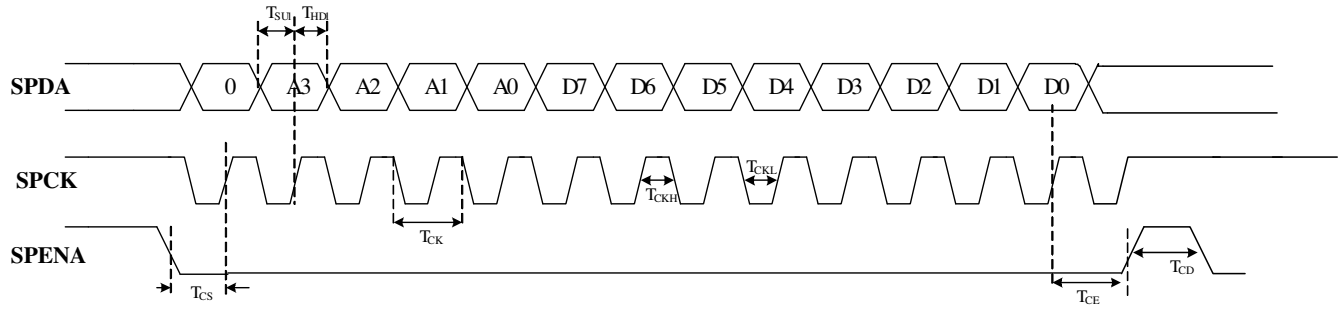
### 10-2 SPI timing characteristic

| Characteristics | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| SPCK period | $T_{CK}$ | 60 | - | - | ns | |
| SPCK high width | $T_{CKH}$ | 30 | - | - | ns | |
| SPCK low width | $T_{CKL}$ | 30 | - | - | ns | |
| Data setup time | $T_{SU1}$ | 12 | - | - | ns | |
| Data hold time | $T_{HD1}$ | 12 | - | - | ns | |
| SPENA to SPCK setup time | $T_{CS}$ | 20 | - | - | ns | |
| SPENA to SPDA hold time | $T_{CE}$ | 20 | - | - | ns | |
| SPENA high pulse width | $T_{CD}$ | 50 | - | - | ns | |
| SPDA output latency | $T_{CR}$ | - | 1/2 | - | $T_{CK}$ | |

**SPI 'read' timing**




**SPI 'write' timing**

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**10-3 Timing characteristics of input signals**

10-3.1 Serial 8 bits RGB interface

| Characteristics | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| CLK period | $T_{OSC}$ | - | 52 | - | ns | Note10-3 |
| Data setup time | $T_{SU}$ | 12 | - | - | ns | |
| Data hold time | $T_{HD}$ | 12 | - | - | ns | |
| HS period | $T_H$ | - | 1224 | - | $T_{OSC}$ | |
| HS pulse width | $T_{HS}$ | 5 | 90 | - | $T_{OSC}$ | |
| HS rising time | $T_{Cr}$ | - | - | 700 | ns | |
| HS falling time | $T_{Cf}$ | - | - | 300 | ns | |
| VS pulse width | $T_{VS}$ | 1 | 3 | 5 | $T_H$ | |
| VS rising time | $T_{Vr}$ | - | - | 700 | ns | |
| VS falling time | $T_{Vf}$ | - | - | 1.5 | us | |
| HS falling to VS falling time for odd field | $T_{HVO}$ | 0 | 3 | - | $T_{OSC}$ | |
| VS falling to HS falling time for even field | $T_{HVE}$ | 0 | 3 | - | $T_{OSC}$ | |
| VS-DEN time | $T_{VSE}$ | - | 18 | - | $T_H$ | |
| HS-DEN time | $T_{HE}$ | 108 | 204 | 264 | $T_{OSC}$ | |
| DEN pulse width | $T_{EP}$ | - | 960 | - | $T_{OSC}$ | |
| VS period | | - | 262 | - | $T_H$ | |

Note 10-3 : When SYNC mode is used, 1st data start from 204th CLK after HS fallings.

10-3.2 Parallel 24 bits RGB interface

| Characteristics | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| CLK period | $T_{OSC}$ | - | 156 | - | ns | Note10-2 |
| Data setup time | $T_{SU}$ | 12 | - | - | ns | |
| Data hold time | $T_{HD}$ | 12 | - | - | ns | |
| HS period | $T_H$ | - | 408 | - | $T_{OSC}$ | |
| HS pulse width | $T_{HS}$ | 5 | 30 | - | $T_{OSC}$ | |
| HS rising time | $T_{Cr}$ | - | - | 700 | ns | |
| HS falling time | $T_{Cf}$ | - | - | 300 | ns | |
| VS pulse width | $T_{VS}$ | 1 | 3 | 5 | $T_H$ | |
| VS rising time | $T_{Vr}$ | - | - | 700 | ns | |
| VS falling time | $T_{Vf}$ | - | - | 1.5 | us | |
| HS falling to VS falling time for odd field | $T_{HVO}$ | 0 | 3 | - | $T_{OSC}$ | |
| VS falling to HS falling time for even field | $T_{HVE}$ | 0 | 3 | - | $T_{OSC}$ | |
| VS-DEN time | $T_{VSE}$ | - | 18 | - | $T_H$ | |
| HS-DEN time | $T_{HE}$ | 36 | 68 | 88 | $T_{OSC}$ | |
| DEN pulse width | $T_{EP}$ | - | 320 | - | $T_{OSC}$ | |
| VS period | | - | 262 | - | $T_H$ | |

Note 10-2 : When SYNC mode is used, 1st data start from 68th CLK after HS fallings.

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10-3.3 CCIR601/656 Interface

| Characteristics | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| CLK period | $T_{OSC}$ | - | 37 | - | ns | |
| Data setup time | $T_{SU}$ | 12 | - | - | ns | |
| Data hold time | $T_{HD}$ | 12 | - | - | ns | |

10-3.4Hardware reset timing

| Characteristics | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| RESETB low pulse width | $T_{RSB}$ | 200 | - | - | ns | |

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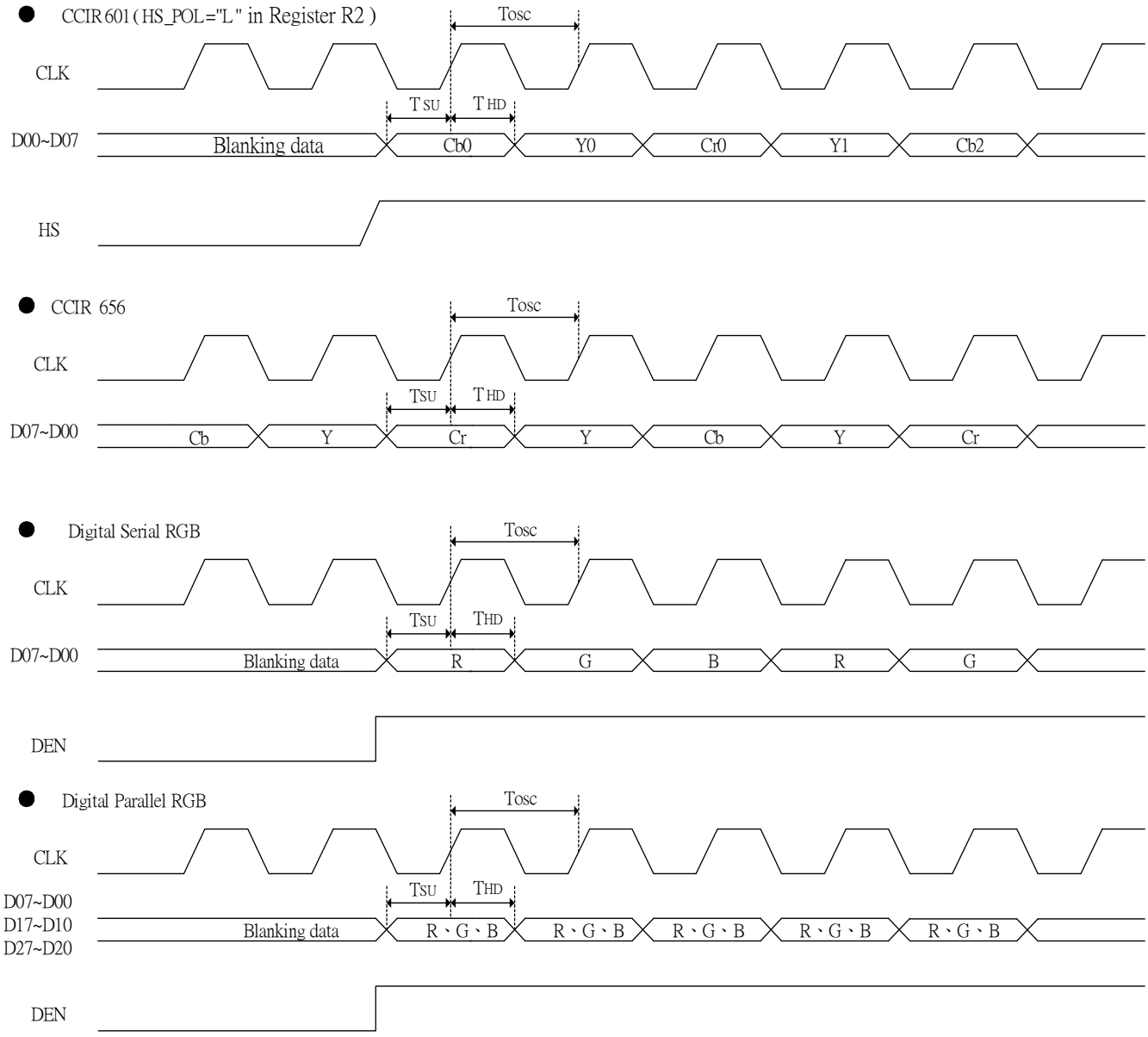
## 10-4 Timing controller timing chart

### 10-4.1Clock and Data waveform

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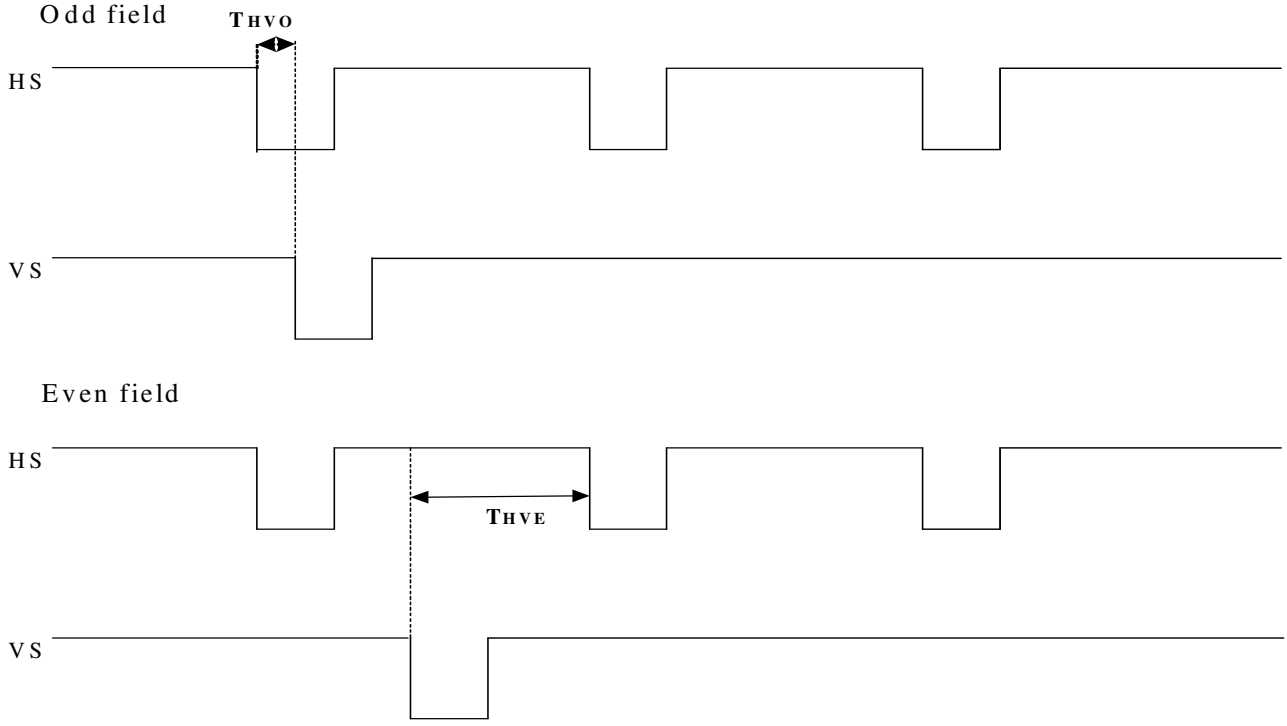
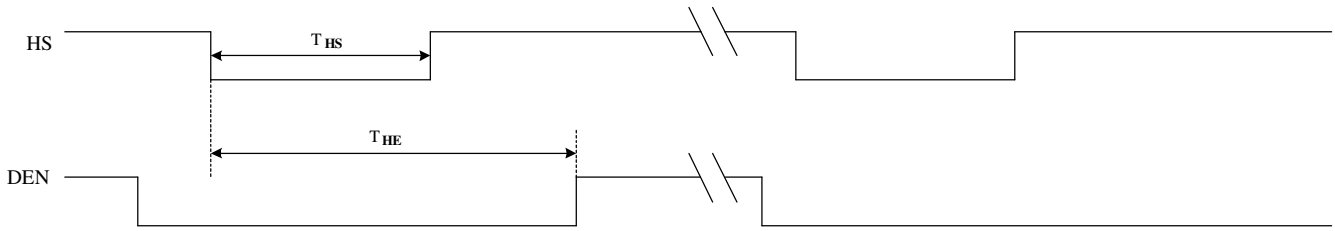
10-4.2 HS,VS,DEN timing waveform

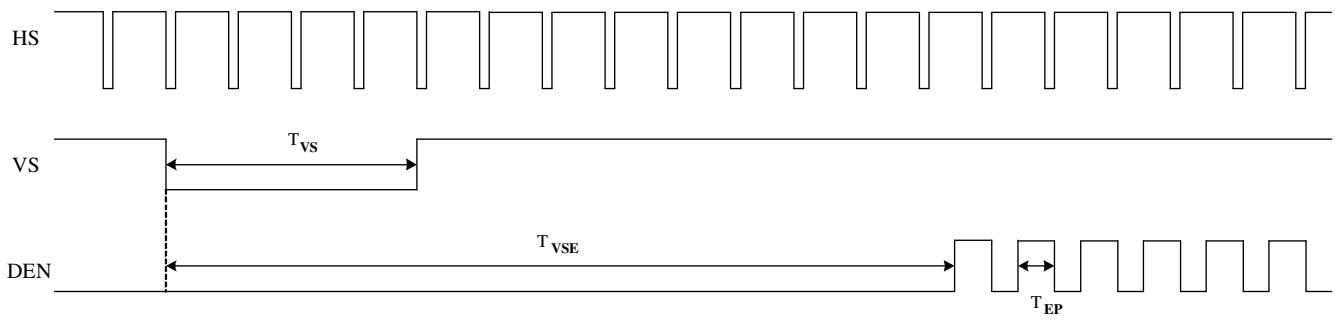
**HS and VS timing relationship**




**HS and DEN timing relationship**




**HS, VS and DEN timing relationship**

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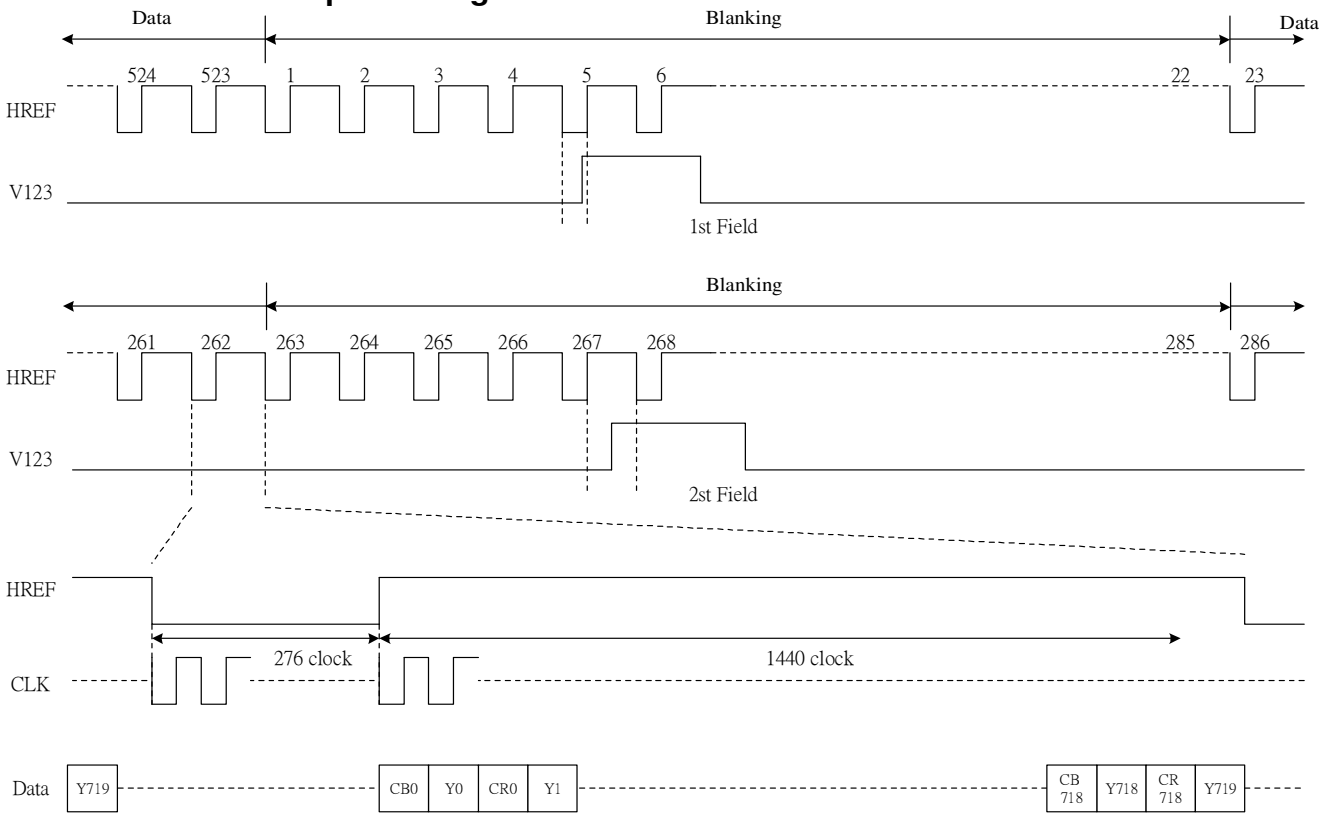
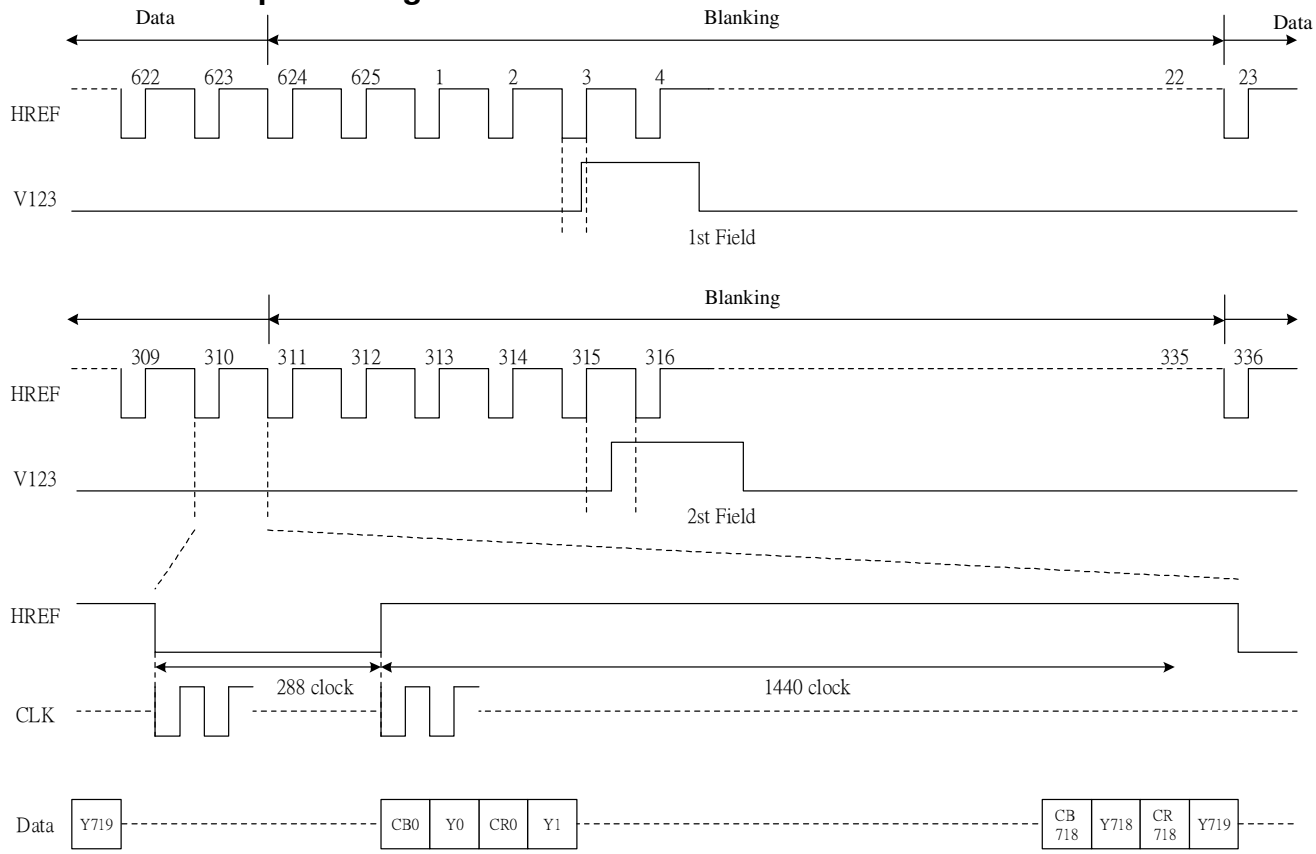
10-4.3 CCIR601 timing waveform (VS_POL="H", HS_POL="L" in Register R2)

**ITU-R BT.601 NTSC Input Timing**




**ITU-R BT.601 PAL Input Timing**

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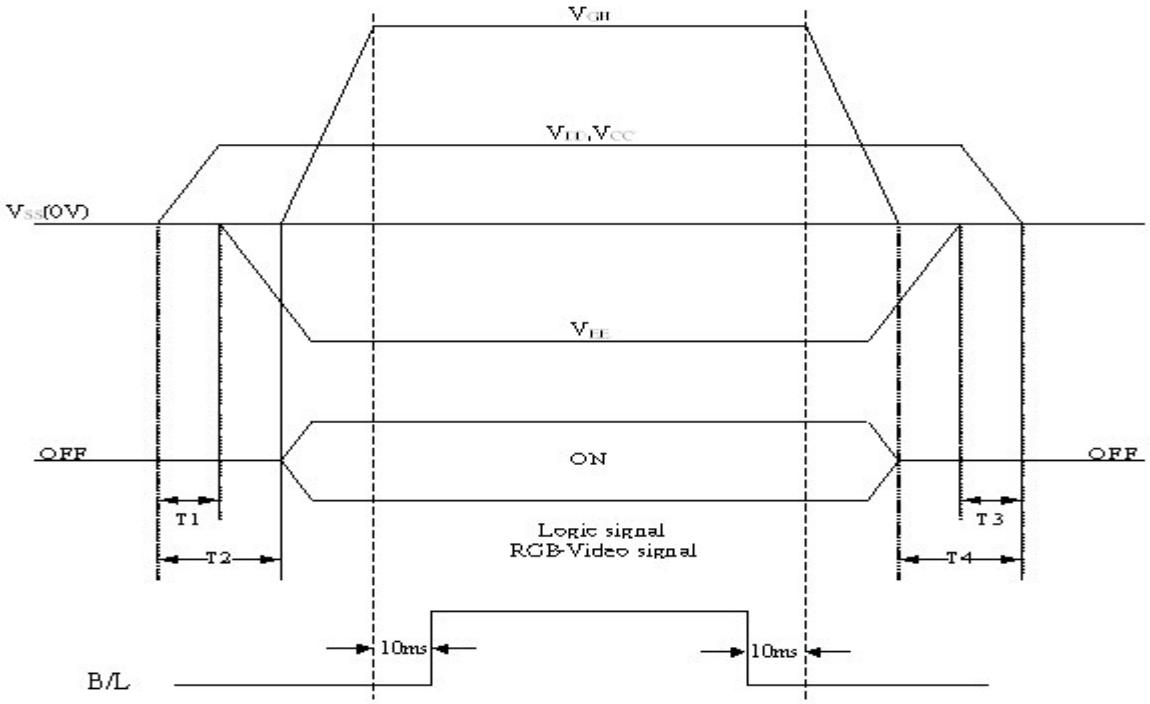
### 11. Power On Sequence

The Power on sequence only effect by $V_{CC}$,$V_{SS}$,$V_{DD}$,$V_{EE}$ and $V_{GH,}$ the others do not care.




(1) 10ms≦T1<T2

(2) 0ms<T3≦T4≦10ms

### 12. Optical Characteristics

#### 12-1) Specification:

Ta=25℃

| Parameter | | Symbol | Condition | MIN. | TYP. | MAX. | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| Viewing Angle | Horizontal | $\theta$ | CR≧5 | 55 | 60 | - | deg | Note 12-1 |
| | Vertical | $\theta$ (to 6 o'clock) | | 45 | 50 | - | deg | |
| | | $\theta$ (to 12 o'clock) | | 35 | 40 | - | deg | |
| Contrast Ratio | | CR | At optimized viewing angle | 200 | 400 | - | - | Note 12-2 |
| Response time | Rise | Tr | $\theta$ =0° | - | 15 | 30 | ms | Note 12-3 |
| | Fall | Tf | | - | 25 | 50 | ms | |
| Brightness | | | $\theta$ =0°/ $\varphi$ =0 | 450 | 500 | - | cd/㎡ | Note 12-4 |
| Luminance Uniformity | | U | | 75 | 80 | - | % | Note 12-5 |
| White Chromaticity | | x | | 0.29 | 0.32 | 0.35 | - | |
| | | y | | 0.33 | 0.36 | 0.39 | - | |
| Lamp Life | | | | - | 45000 | - | hr | At=5mA |

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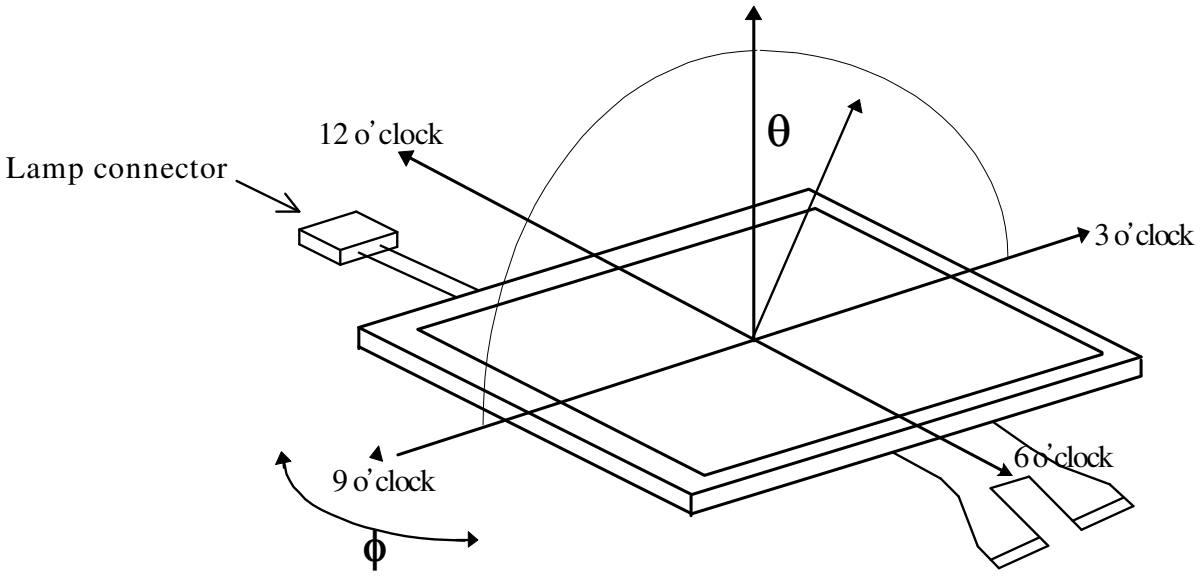
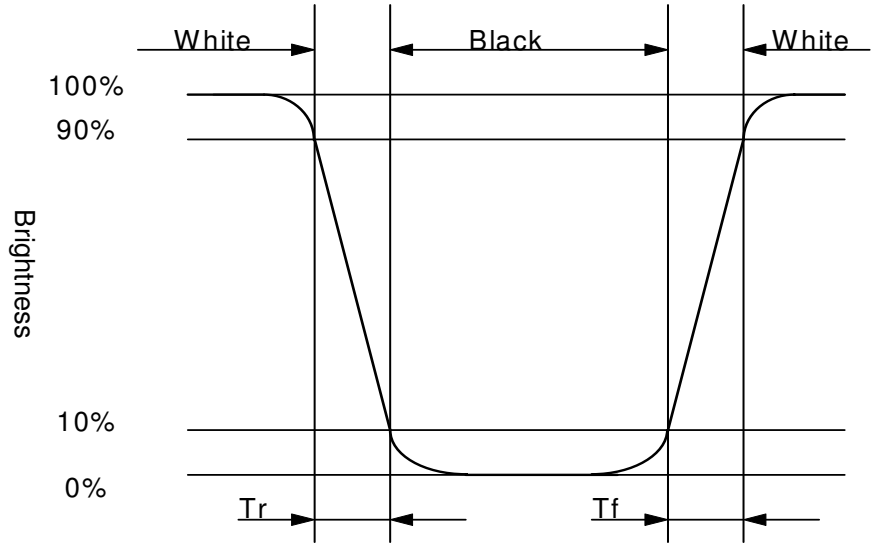
Note 12-1: The definitions of viewing angles are as follow




Note 12-2: The definition of contrast ratio $CR = \frac{\text{Luminance at gray level 63}}{\text{Luminance at gray level 0}}$

Note 12-3: Definition of Response Time Tr and Tf:

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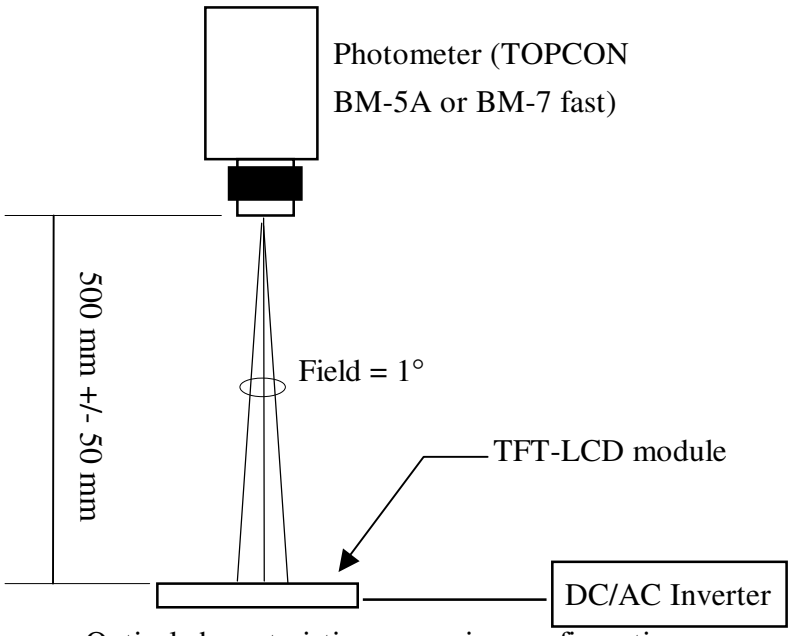
Note 12-4: All optical measurements shall be performed after backlight being turned-on for 30 mins. The optical characteristics shall be measured in dark room (ambient illumination on panel surface less than 1 Lux). The measuring configuration shows as following figure.




Optical characteristics measuring configuration

Note 12-5: The uniformity of LCD is defined as

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

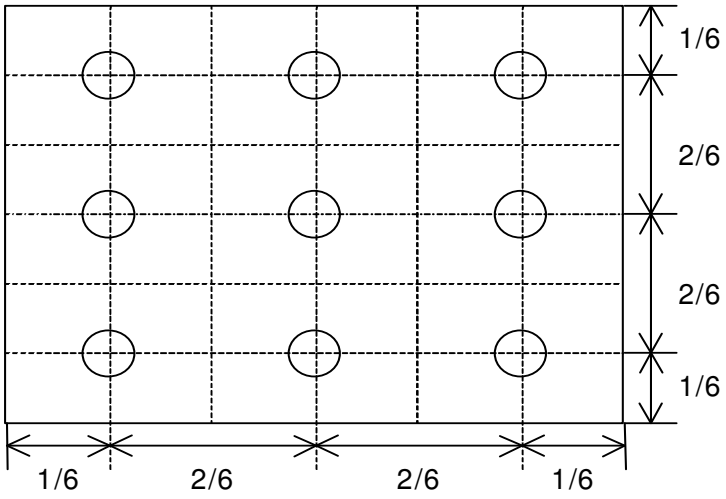
Luminance meter: BM-5A or BM-7 fast (TOPCON)

Measurement distance: 500 mm +/- 50 mm

Ambient illumination: < 1 Lux

Measuring direction: Perpendicular to the surface of module

The test pattern is white (Gray Level 63).

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## 13. Handling Cautions

### 13-1) Mounting of module

a) Please power off the module when you connect the input/output connector.

b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.

1. The noise from the backlight unit will increase.
2. The output from inverter circuit will be unstable.
3. In some cases a part of module will heat.

c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.

d) Protective film (Laminator) is applied on surface to protect it against scratches and dirts. It is recommended to peel off the laminator before use and taking care of static electricity.

### 13-2) Precautions in mounting

a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.

b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.

c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.

d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

### 13-3) Adjusting module

a) Adjusting volumes on the rear face of the module have been set optimally before shipment.

b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

### 13-4) Others

a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.

b) Store the module at a room temperature place.

c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.

d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.

e) Observe all other precautionary requirements in handling general electronic components.

f) Please adjust the voltage of common electrode as material of attachment by 1 module.

### 13-5) Polarizer mark

The polarizer mark is to describe the direction of wide view angle film how to match up with the rubbing direction.

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**14. Reliability Test**

| No | Test Item | Test Condition | Remark |
|---|---|---|---|
| 1 | High Temperature Storage Test | Ta = +80℃, 240 hrs | |
| 2 | Low Temperature Storage Test | Ta = -30℃, 240 hrs | |
| 3 | High Temperature Operation Test | Ta = +70℃, 240 hrs | |
| 4 | Low Temperature Operation Test | Ta = -20℃, 240 hrs | |
| 5 | High Temperature & High Humidity Operation Test | Ta = +60℃, 90%RH, 240 hrs<br>(No Condensation) | |
| 6 | Thermal Cycling Test<br>(non-operating) | -20℃→+70℃, 200 Cycles<br>30min 30min | |
| 7 | Vibration Test<br>(non-operating) | Frequency : 10 ~ 57 $H_Z$ /Vibration Width :0.075mm<br>58-500 H/ / Gravity :9.8m/s<br>Sweep time: 11 minutes<br>Test period: 3 hrs for each direction of X, Y, Z | |
| 8 | Shock Test<br>(non-operating) | Gravity :490m/s<br>Direction: ±X, ±Y, ±Z<br>Pulse Width :11ms,half sine wave | |
| 9 | Electrostatic Discharge Test<br>(non-operating) | Machine Mode = ±200V<br>C = 200pF , R = 0Ω<br>1 times discharge for each pad | |

Ta: ambient temperature

Note: The protective film must be removed before temperature test

[Criteria]

1. Main LCD should normally work under the normally condition no defect of function,screen quality and appearance (including : mura ,line defect ,no image)

2. After the temperature and humidity test, the luminance and CR (Contrast ratio) ,should not be lower than minimum of specification.

3. After the vibration and shock test , can't be found chip broken.

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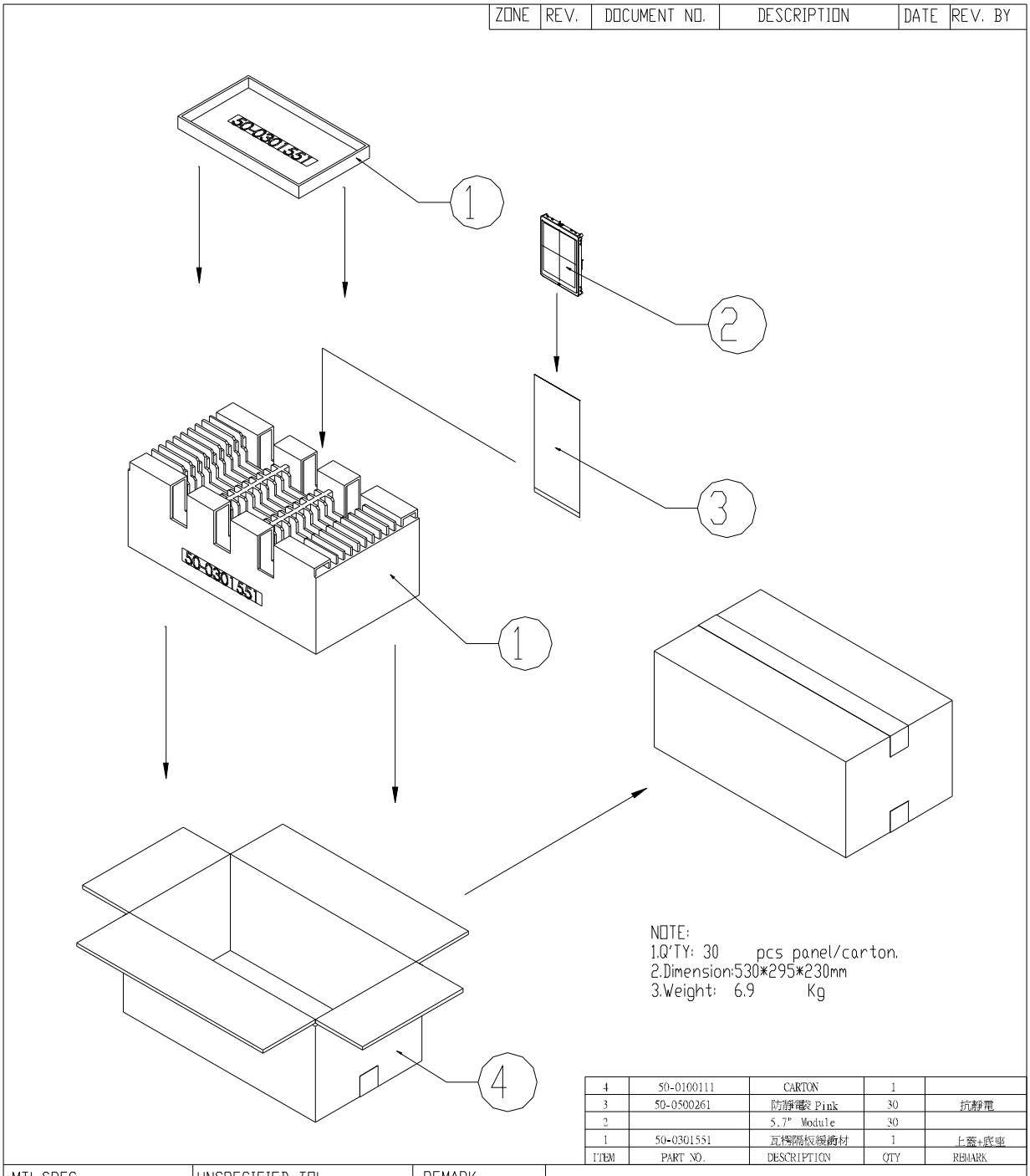
## 15. Packing Diagram

| ZONE | REV. | DOCUMENT NO. | DESCRIPTION | DATE | REV. BY |
|---|---|---|---|---|---|




NOTE:
1.Q'TY: 30 pcs panel/carton.
2.Dimension:530*295*230mm
3.Weight: 6.9 Kg

| ITEM | PART NO. | DESCRIPTION | QTY | REMARK |
|---|---|---|---|---|
| 4 | 50-0100111 | CARTON | 1 | |
| 3 | 50-0500261 | 防靜電袋 Pink | 30 | 抗靜電 |
| 2 | | 5.7" Module | 30 | |
| 1 | 50-0301551 | 瓦楞隔板緩衝材 | 1 | 上蓋+底座 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MTL.SPEC. | | UNSPECIFIED TOL.<br>ANGLE<br>ROUGHNESS | REMARK | 元太科技股份有限公司<br>Prime View Internation Co.,ltd. | | | |
| APPROVE | Frank Shin | 2006/03/16 | SCALE | UNIT | SHEET<br>1 OF 1 | DWG.TITLE<br>5.7" Module Packing Draw | |
| CHECK | Frank Shin | 2006/03/16 | | | | | |
| DESIGN | James | 2006/03/16 | MTL.NO.<br>PD057VU2 | | | DWG.NO. | REV.<br>01 / A4 SIZE |

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## Revision History

| Rev. | Issued Date | Revised Contents |
|---|---|---|
| 1.0 | May.11, 2006 | New |

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