

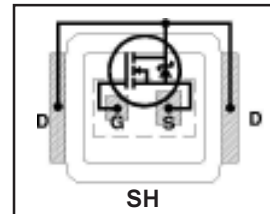
IRF6655

DirectFET™ Power MOSFET ②

Typical values (unless otherwise specified)

- RoHS compliant containing no lead or bromide ①
- Low Profile (<0.7 mm)
- Dual Sided Cooling Compatible ①
- Ultra Low Package Inductance
- Optimized for High Frequency Switching ①
- Ideal for High Performance Isolated Converter Primary Switch Socket
- Ideal for Control FET sockets in 36V – 75V in Synchronous Buck applications
- Low Conduction Losses
- Compatible with existing Surface Mount Techniques ①

V_{DSS}	V_{GS}	R_{DS(on)}
100V max	±20V max	53mΩ @ 10V
Q_{g tot}	Q_{gd}	V_{gs(th)}
8.7nC	2.8nC	3.9V



Applicable DirectFET Outline and Substrate Outline (see p.7,8 for details)①

SQ	SX	ST	SH	MQ	MX	MT	MN			
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Description

The IRF6655 combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest combined on-state resistance and gate charge in a package that has a footprint similar to that of a micro-8, and only 0.7mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infrared or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, improving previous best thermal resistance by 80%.

The IRF6655 is optimized for low power primary side bridge topologies in isolated DC-DC applications, and for high side control FET sockets in non-isolated synchronous buck DC-DC applications for use in wide range universal Telecom systems (36V – 75V), and for secondary side synchronous rectification in regulated DC-DC topologies. The reduced total losses in the device coupled with the high level of thermal performance enables high efficiency and low temperatures, which are key for system reliability improvements, and makes this device ideal for high performance isolated DC-DC converters.

Absolute Maximum Ratings

	Parameter	Max.	Units
V _{DS}	Drain-to-Source Voltage	100	V
V _{GS}	Gate-to-Source Voltage	±20	
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V ⑥	4.2	A
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ 10V ⑥	3.4	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V ⑥	19	
I _{DM}	Pulsed Drain Current ③	34	
E _{AS}	Single Pulse Avalanche Energy ④	11	mJ
I _{AR}	Avalanche Current ③	5.0	A

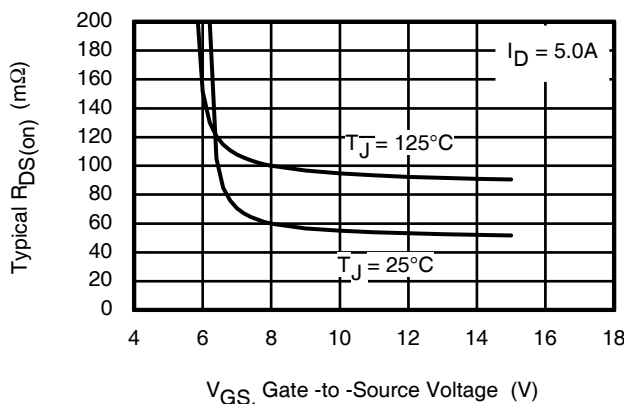


Fig 1. Typical On-Resistance Vs. Gate Voltage

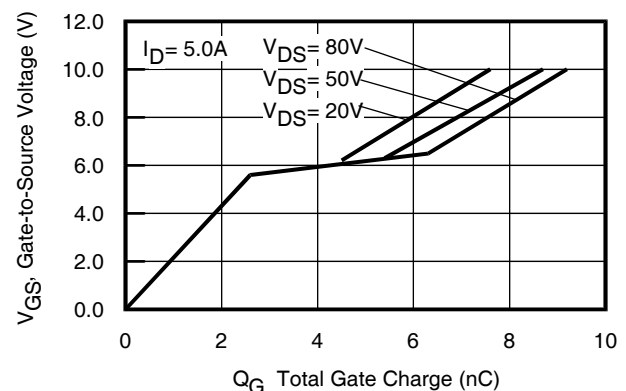


Fig 2. Typical On-Resistance Vs. Gate Voltage

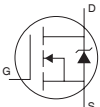
Notes:

- ① Click on this section to link to the appropriate technical paper.
- ② Click on this section to link to the DirectFET MOSFETs
- ③ Repetitive rating; pulse width limited by max. junction temperature.
- ④ Starting T_J = 25°C, L = 0.89mH, R_G = 25Ω, I_{AS} = 5.0A.
- ⑤ Surface mounted on 1 in. square Cu board, steady state.
- ⑥ T_C measured with thermocouple mounted to top (Drain) of part.

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$	
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.12	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$	
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	53	62	m Ω	$V_{GS} = 10V, I_D = 5.0A$ ⑤	
$V_{GS(th)}$	Gate Threshold Voltage	2.8	—	4.8	V	$V_{DS} = V_{GS}, I_D = 25\mu A$	
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-11	—	mV/ $^\circ\text{C}$		
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 100V, V_{GS} = 0V$	
		—	—	250		$V_{DS} = 80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$	
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$	
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$	
g_{fs}	Forward Transconductance	6.6	—	—	S	$V_{DS} = 10V, I_D = 5.0A$	
Q_g	Total Gate Charge	—	8.7	11.7	nC	$V_{DS} = 50V$ $V_{GS} = 10V$ $I_D = 5.0A$ See Fig. 17	
Q_{gs1}	Pre-V _{th} Gate-to-Source Charge	—	2.1	—			
Q_{gs2}	Post-V _{th} Gate-to-Source Charge	—	0.58	—			
Q_{gd}	Gate-to-Drain Charge	—	2.8	4.2			
Q_{godr}	Gate Charge Overdrive	—	3.2	—			
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	3.4	—			
Q_{oss}	Output Charge	—	4.5	—	nC	$V_{DS} = 16V, V_{GS} = 0V$	
R_G	Gate Resistance	—	1.9	2.9	Ω		
$t_{d(on)}$	Turn-On Delay Time	—	7.4	—	ns	$V_{DD} = 50V, V_{GS} = 10V$ ⑤ $I_D = 5.0A$ $R_G = 6.0\Omega$	
t_r	Rise Time	—	2.8	—			
$t_{d(off)}$	Turn-Off Delay Time	—	14	—			
t_f	Fall Time	—	4.3	—			
C_{iss}	Input Capacitance	—	530	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$	
C_{oss}	Output Capacitance	—	110	—			
C_{rss}	Reverse Transfer Capacitance	—	29	—			
C_{oss}	Output Capacitance	—	510	—			$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	67	—			$V_{GS} = 0V, V_{DS} = 80V, f = 1.0\text{MHz}$

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	38	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ⑤	—	—	34		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 5.0A, V_{GS} = 0V$ ⑤
t_{rr}	Reverse Recovery Time	—	31	47	ns	$T_J = 25^\circ\text{C}, I_F = 5.0A, V_{DD} = 25V$
Q_{rr}	Reverse Recovery Charge	—	37	56	nC	$di/dt = 100A/\mu s$ ⑤

Notes:

⑤ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.

Absolute Maximum Ratings

	Parameter	Max.	Units
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation ⑥	2.2	W
$P_D @ T_A = 70^\circ\text{C}$	Power Dissipation ⑥	1.4	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation ⑥	42	
T_P	Peak Soldering Temperature	270	°C
T_J	Operating Junction and	-40 to + 150	
T_{STG}	Storage Temperature Range		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ⑥⑩	—	58	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑦⑩	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑧⑩	20	—	
$R_{\theta JC}$	Junction-to-Case ⑨⑩	—	3.0	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted	1.4	—	

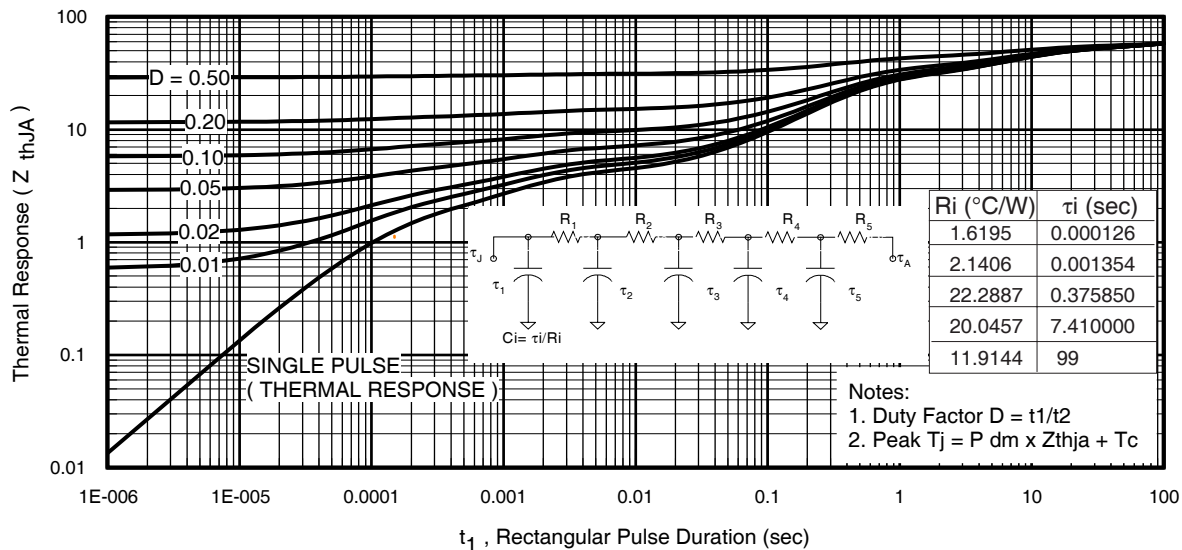


Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Notes:

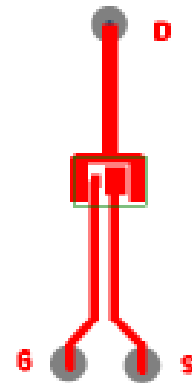
- ⑥ Surface mounted on 1 in. square Cu board, steady state.
- ⑦ Used double sided cooling, mounting pad.
- ⑧ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ⑨ T_C measured with thermocouple incontact with top (Drain) of part.
- ⑩ R_{θ} is measured at T_J of approximately 90°C .



⑥ Surface mounted on 1 in. square Cu board (still air).



⑦ Mounted to a PCB with a thin gap filler and heat sink (still air)



⑧ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)

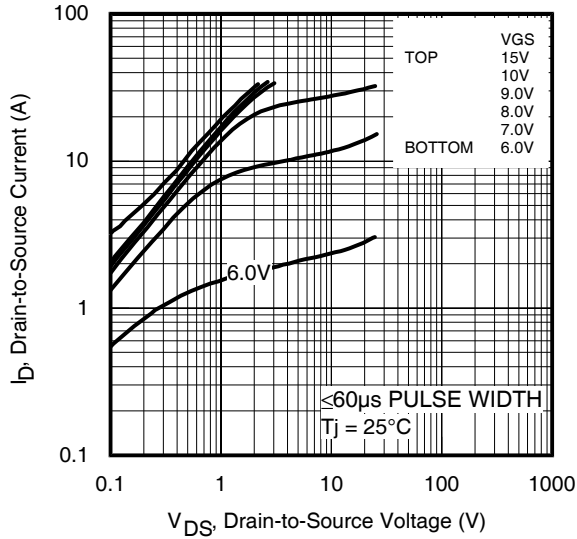


Fig 4. Typical Output Characteristics

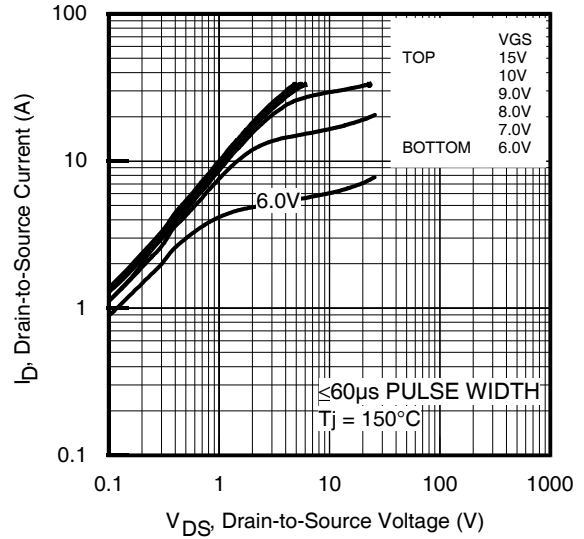


Fig 5. Typical Output Characteristics

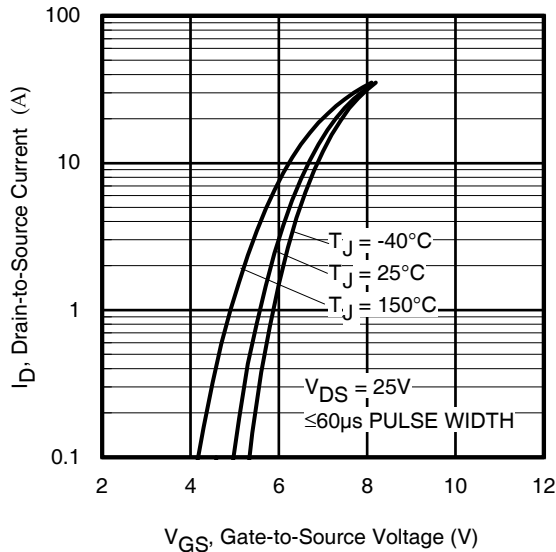


Fig 6. Typical Transfer Characteristics

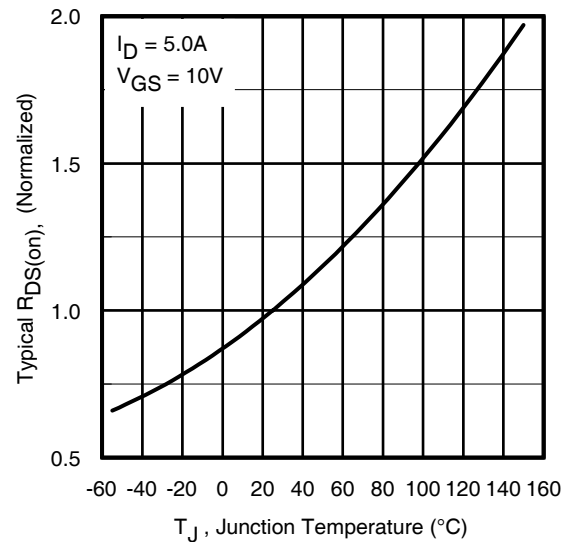


Fig 7. Normalized On-Resistance vs. Temperature

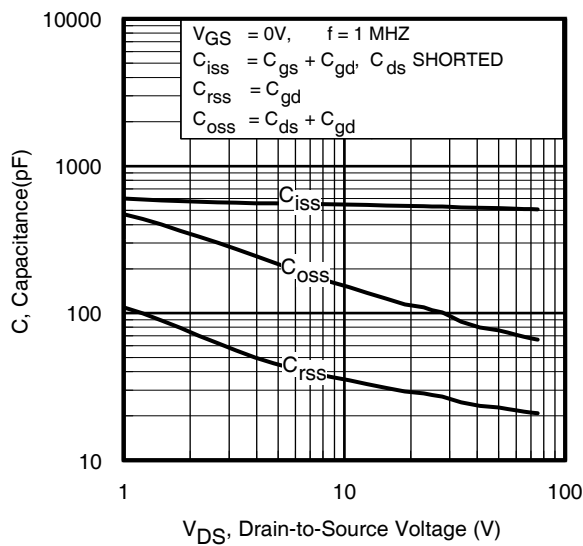


Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

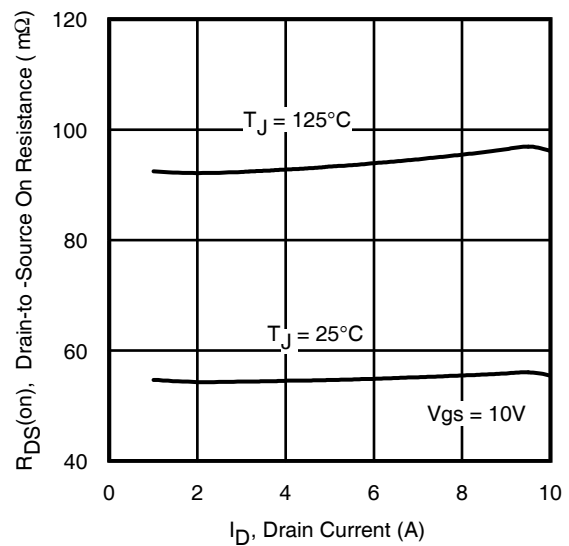


Fig 9. Normalized Typical On-Resistance vs. Drain Current and Gate Voltage

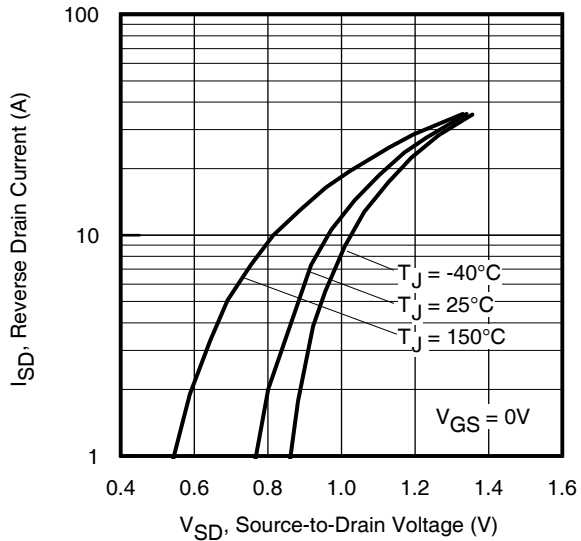


Fig 10. Typical Source-Drain Diode Forward Voltage

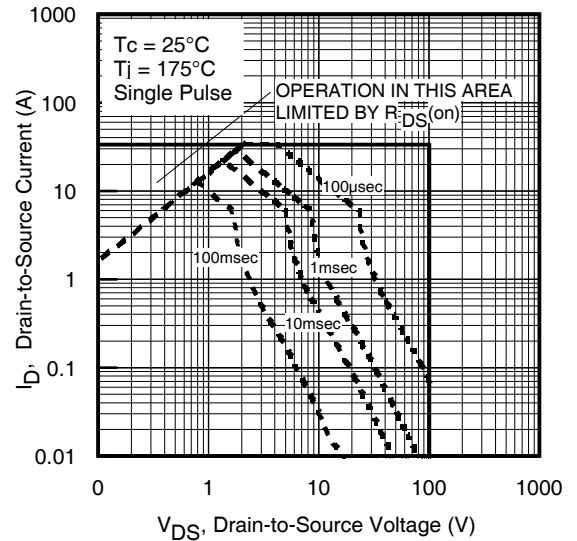


Fig11. Maximum Safe Operating Area

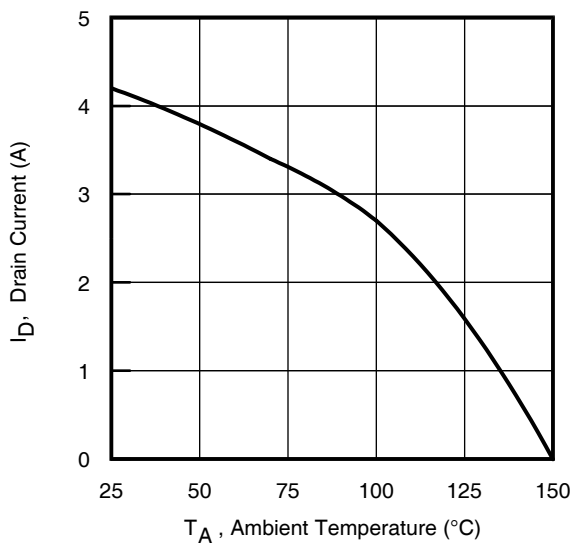


Fig 12. Maximum Drain Current vs. Ambient Temperature

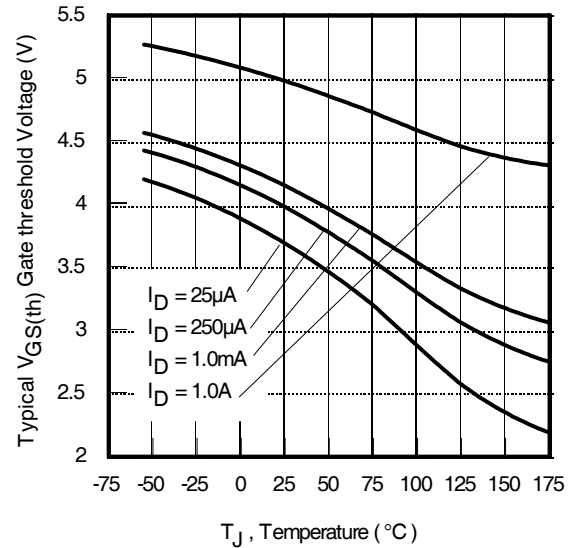


Fig 13. Threshold Voltage vs. Temperature

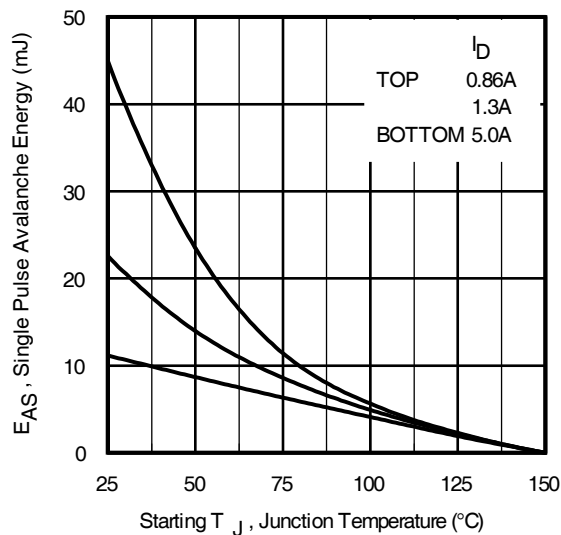


Fig 14. Maximum Avalanche Energy vs. Drain Current

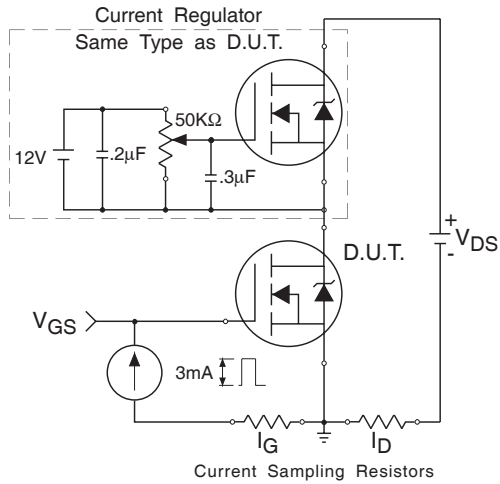


Fig 15a. Gate Charge Test Circuit

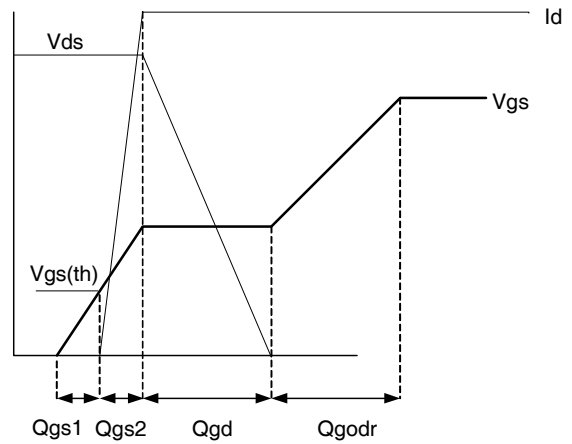


Fig 15b. Gate Charge Waveform

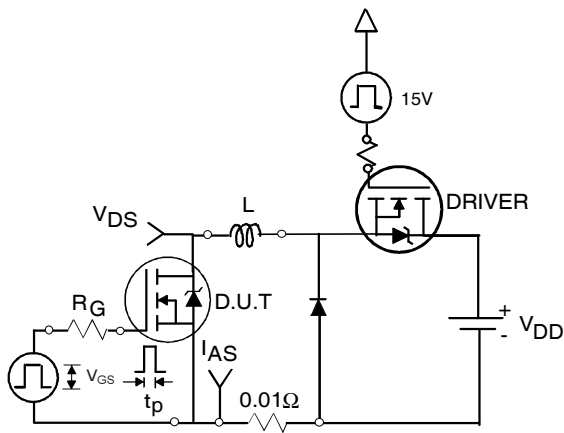


Fig 16a. Unclamped Inductive Test Circuit

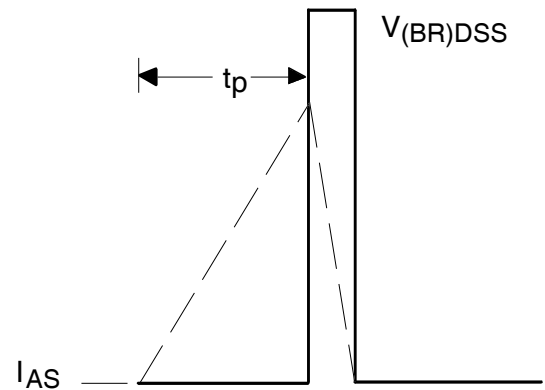


Fig 16b. Unclamped Inductive Waveforms

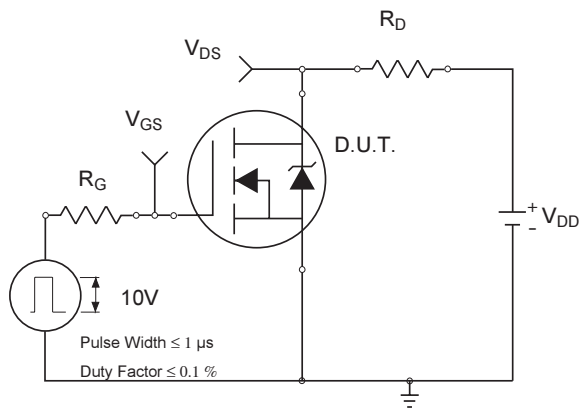


Fig 17a. Switching Time Test Circuit

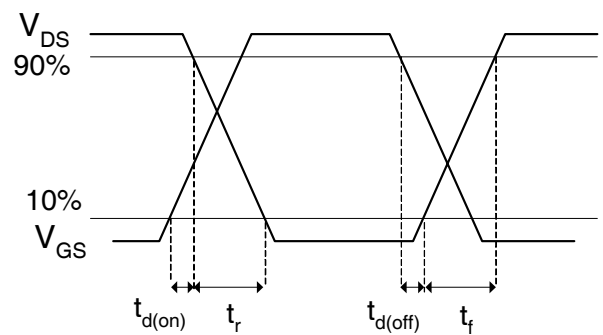
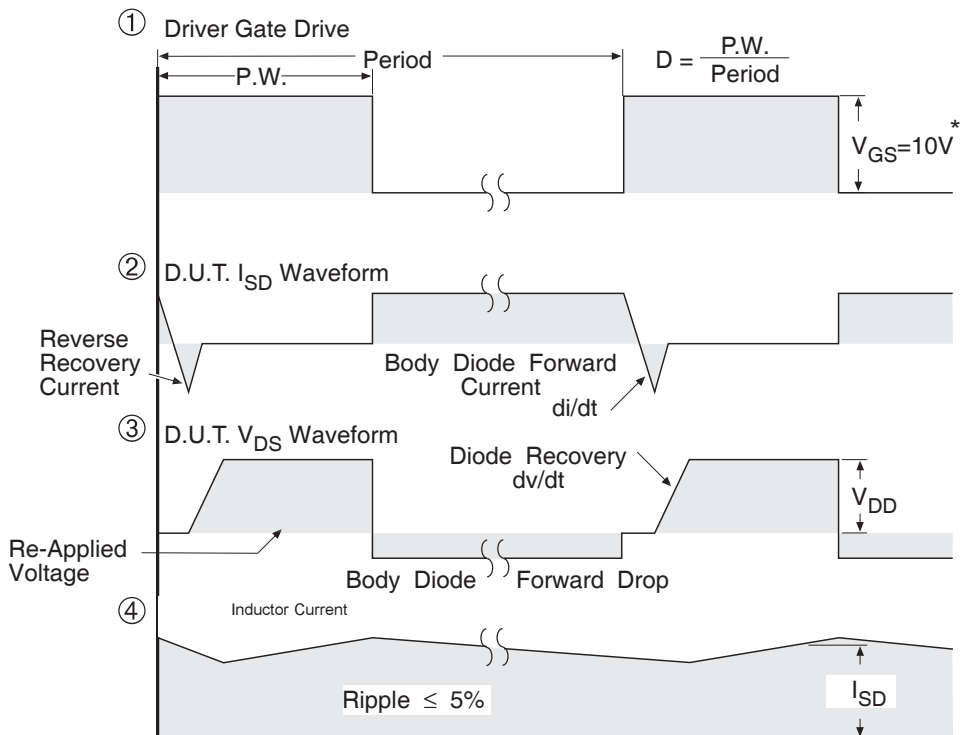
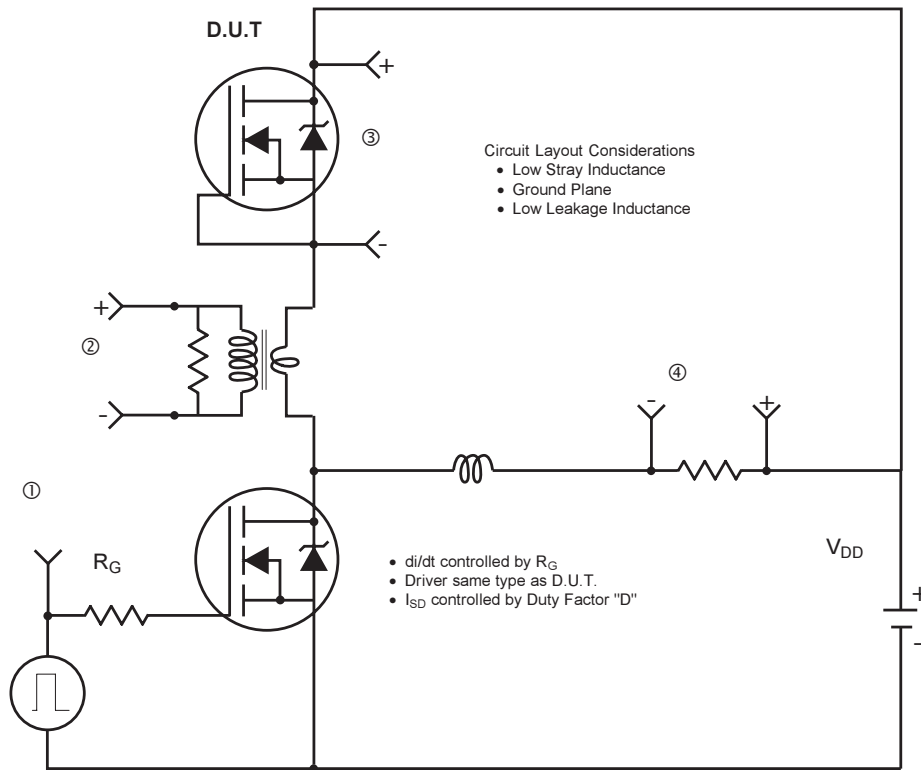


Fig 17b. Switching Time Waveforms



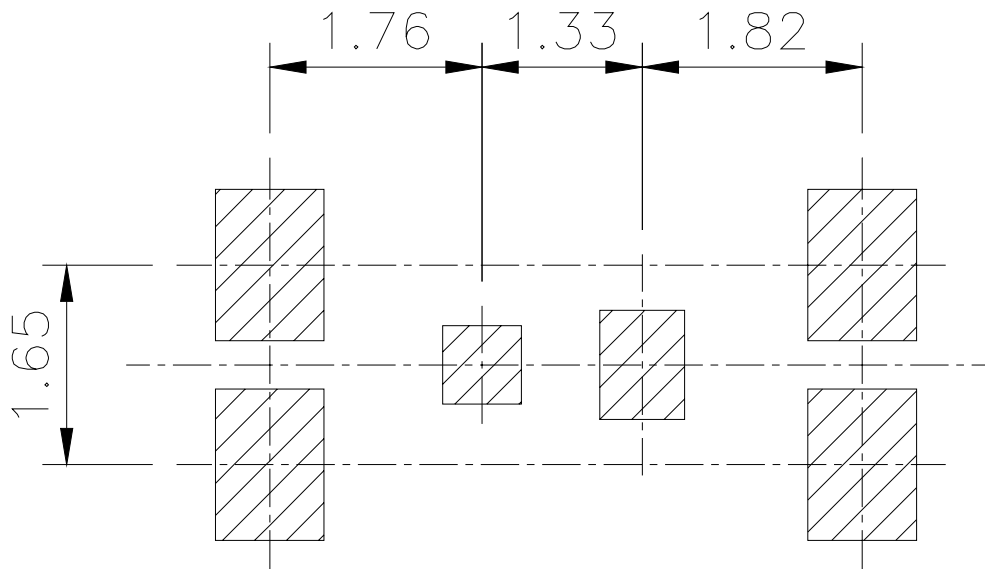
* $V_{GS} = 5V$ for Logic Level Devices

Fig 18. Diode Reverse Recovery Test Circuit for N-Channel HEXFET[®] Power MOSFETs

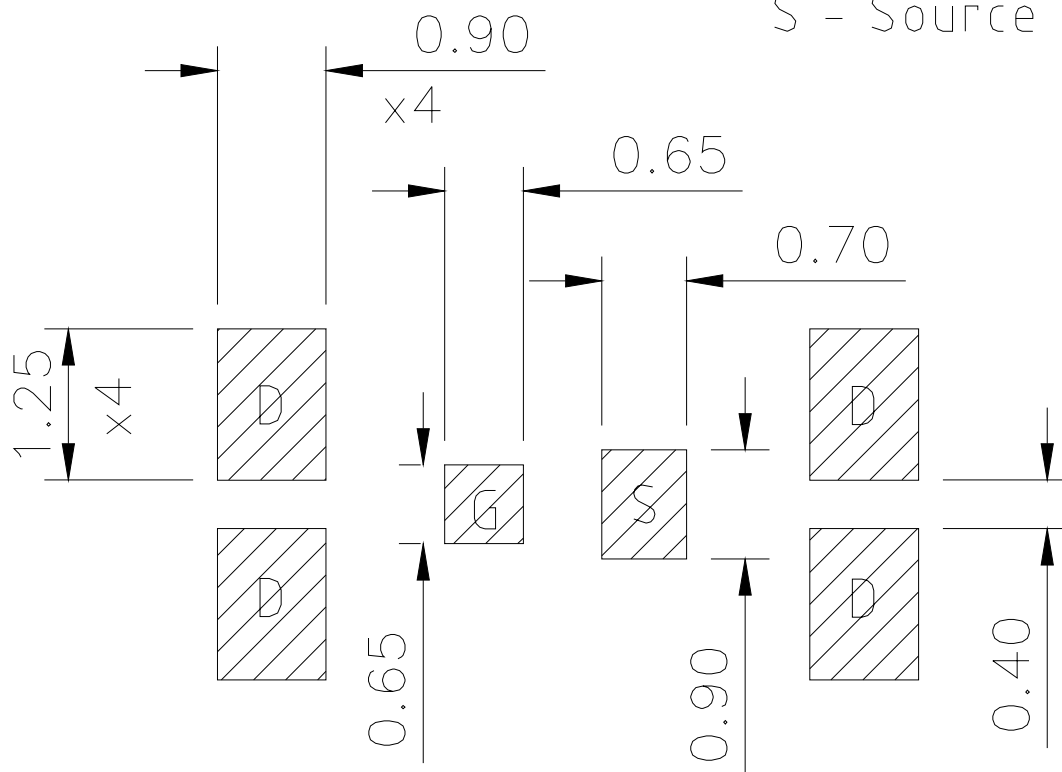
IRF6655

DirectFET™ Substrate and PCB Layout, SH Outline (Small Size Can, H-Designation).

Please see DirectFET application note AN-1035 for all details regarding PCB assembly using DirectFET. This includes all recommendations for stencil and substrate designs.

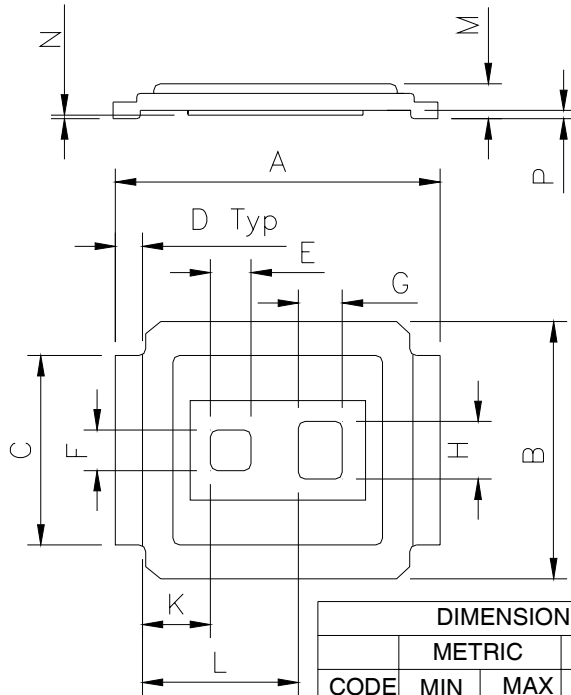


D - Drain
G - Gate
S - Source



**DirectFET™ Outline Dimension, SH Outline
(Small Size Can, H-Designation).**

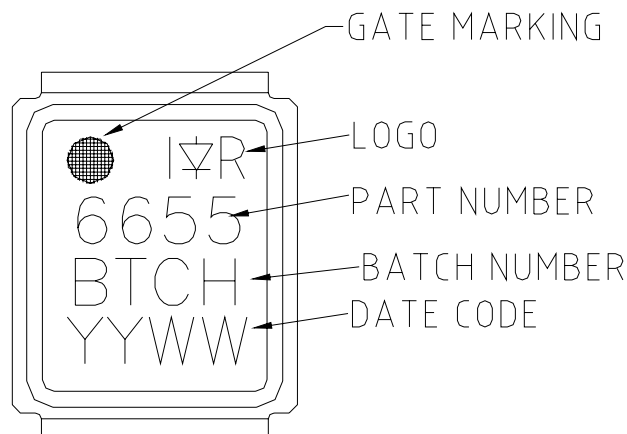
Please see DirectFET application note AN-1035 for all details regarding PCB assembly using DirectFET. This includes all recommendations for stencil and substrate designs.



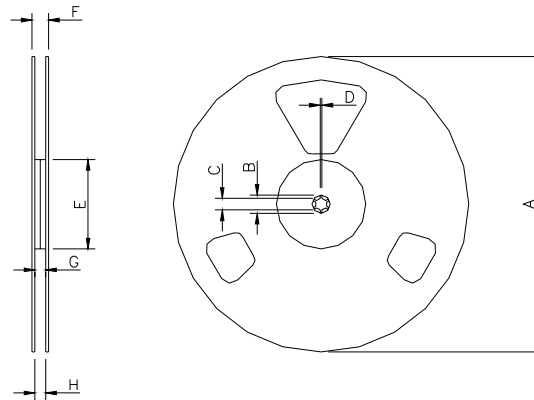
Note: Controlling dimensions are in mm.

DIMENSIONS				
CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	4.75	4.85	0.187	0.191
B	3.70	3.95	0.146	0.156
C	2.75	2.85	0.108	0.112
D	0.35	0.45	0.014	0.018
E	0.58	0.62	0.023	0.024
F	0.58	0.62	0.023	0.024
G	0.63	0.67	0.025	0.026
H	0.83	0.87	0.033	0.034
K	0.99	1.03	0.039	0.041
L	2.29	2.33	0.090	0.092
M	0.59	0.70	0.023	0.028
N	0.03	0.08	0.001	0.003
P	0.08	0.17	0.003	0.007

DirectFET™ Part Marking



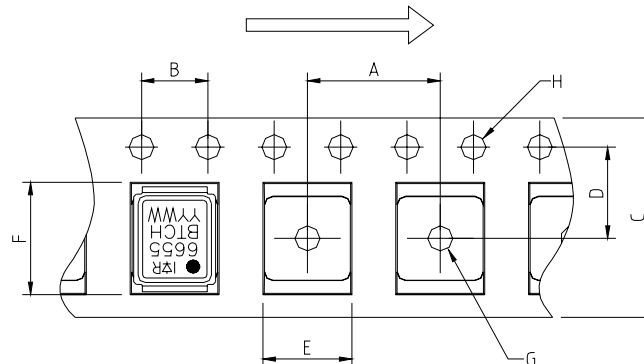
DirectFET™ Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm
Std reel quantity is 4800 parts. (ordered as IRF6655). For 1000 parts on 7" reel, order IRF6655TR1

REEL DIMENSIONS								
CODE	STANDARD OPTION (QTY 4800)				TR1 OPTION (QTY 1000)			
	METRIC		IMPERIAL		METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C	177.77	N.C	6.9	N.C
B	20.2	N.C	0.795	N.C	19.06	N.C	0.75	N.C
C	12.8	13.2	0.504	0.520	13.5	12.8	0.53	0.50
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C	58.72	N.C	2.31	N.C
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C	0.53
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47	N.C
H	11.9	15.4	0.469	0.606	11.9	12.01	0.47	N.C

Loaded Tape Feed Direction



NOTE: CONTROLLING DIMENSIONS IN MM

CODE	DIMENSIONS			
	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	4.00	4.20	0.157	0.165
F	5.00	5.20	0.197	0.205
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>