PRELIMINARY **AUDIO POWER AMPLIFIER**

■ DESCRIPTION

The AA4838 is a monolithic integrated circuit that provides DC volume control, and stereo bridged audio power amplifiers capable of producing 2W into 4Ω with less than 1.0% THD or 2.2W into 3Ω with less than 1.0% THD. The audio integrated circuits were designed specifically to provide high quality audio while requiring a minimum amount of external components. The AA4838 incorporates a DC volume control, stereo bridged audio power amplifiers and a selectable gain or bass boost, making it optimally suited for multimedia monitors, portable radios, and desktop and portable computer applications. The AA4838 features an externally controlled, low-power consumption shutdown mode, and both a power amplifier and headphone mute for maximum system flexibility and performance.

■ FEATURES

- DC volume control interface.
- System beep detects.
- Stereo switchable bridged/single-ended power amplifiers
- Selectable internal/external gain or bass boost
- “Click and pop” suppression circuitry
- Thermal shutdown protection circuitry

■ APPLICATIONS

- Portable and desktop computers
- Multimedia monitors
- Portable radios, PDAs, and portable TVs

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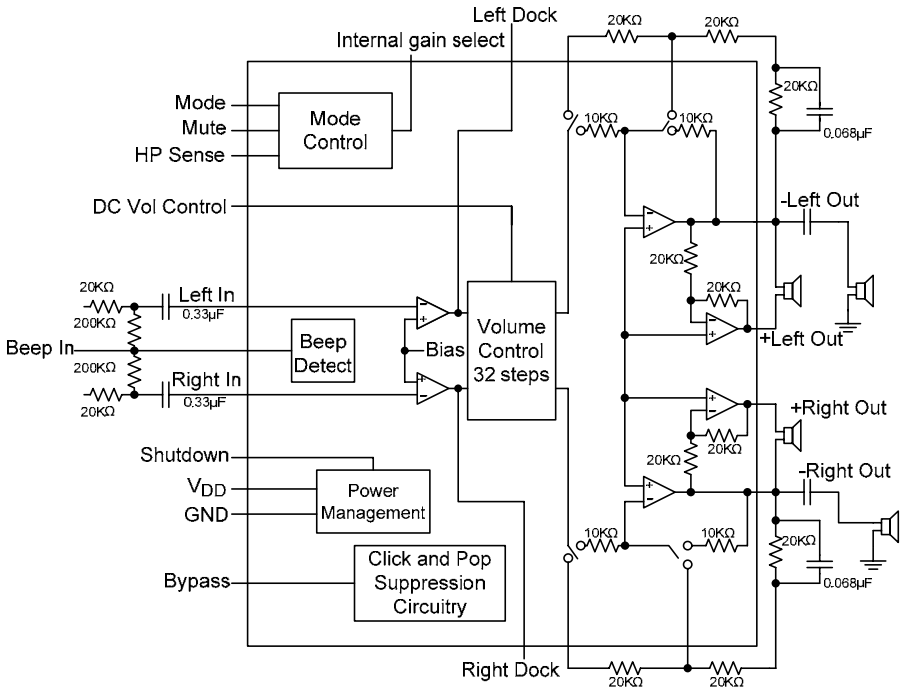
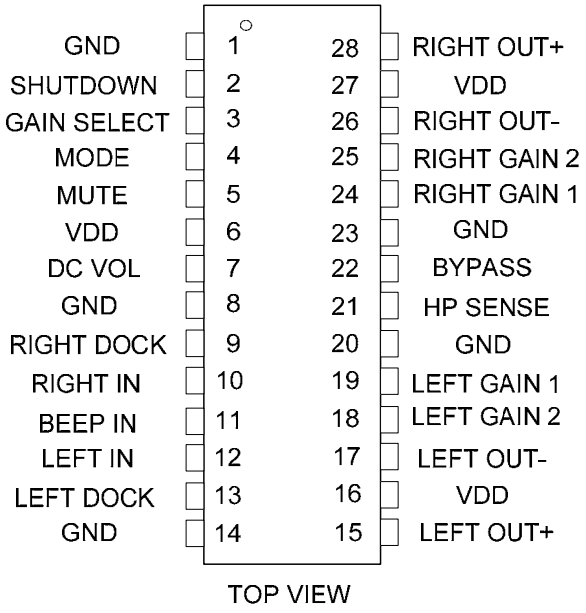
■ BLOCK DIAGRAM



■ PIN DESCRIPTION



TOP VIEW

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PIN NO	PIN NAME	FUNCTION
1,8,14,20,23	GND	Supply ground
2	SHUTDOWN	Shutdown function control
3	GAIN SELECT	Gain selection(internal gain/external gain)
4	MODE	Output stage control(BTL/SE)
5	MUTE	Mute function control
6,16,27	VDD	Supply voltage
7	DC VOL	DC volume control(fixed/or adjustable)
9	RIGHT DOCK	Right dock
10	RIGHT IN	Right audio input
11	BEEP IN	Beep input
12	LEFT IN	Left audio input
13	LEFT DOCK	Left Dock
15	LEFT OUT+	Positive left audio output
17	LEFT OUT-	Negative left audio output
18	LEFT GAIN 2	External left gain control pin2
19	LEFT GAIN 1	External left gain control pin1
21	HP SENSE	Headphone sense
22	BYPASS	Bypass voltage
24	RIGHT GAIN 1	External right gain control pin1
25	RIGHT GAIN 2	External right gain control pin2
26	RIGHT OUT-	Negative left audio output
28	RIGHT OUT+	Positive left audio output

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■ ABSOLUTE MAXIMUM RATINGS

(TA = +25°C)

PARAMETER	SYMBOL	RATING	UNIT
Power supply voltage	VCC	6	V
Storage temperature	Tstg	–65 ~+150	°C
Input voltage	VIN	–0.3 ~VDD+0.3	V
Power dissipation	PD	Internally limited	mW
ESD susceptibility	HBM	2000	V

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ ELECTRICAL CHARACTERISTICS FOR ENTIRE IC

The following specifications apply for VDD = 5V unless otherwise noted. Limits apply for TA = 25˚C

PARAMETER	SYMBOL	TEST CONDITION	VALUE			UNIT
			MIN	TYP	MAX	
Supply Voltage	VDD		2.7	-	5.5	V
Quiescent Power Supply Current	IDD	VIN= 0V, IO= 0A	-	15	30	mA
Shutdown Current	ISD	Vshutdown = VDD		0.7	2.0	μA
Headphone Sense High Input Voltage	VIH		4	-	-	V
Headphone Sense Low Input Voltage	VIL		-	-	0.8	V

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■ ELECTRICAL CHARACTERISTICS FOR VOLUME ATTENUATORS

The following specifications apply for VDD = 5V unless otherwise noted. Limits apply for TA = 25˚C

PARAMETER	SYMBOL	TEST CONDITION	VALUE			UNIT
			MIN	TYP	MAX	
Attenuator Range	CRANGE	Gain with VDCVOL = 5V, No Load	-	-	±0.75	dB
		Attenuation with VDCVOL = 0V (BM & SE)	-75	-	-	dB
Mute Attenuation	AM	VMUTE = 5V, Bridged Mode (BM)	-78	-	-	dB
		VMUTE = 5V, Single-Ended Mode (SE)	-78	-	-	dB

■ ELECTRICAL CHARACTERISTICS FOR SINGLE-ENDED MODE OPERATION

The following specifications apply for VDD = 5V unless otherwise noted. Limits apply for TA = 25˚C

PARAMETER	SYMBOL	TEST CONDITION	VALUE			UNIT
			MIN	TYP	MAX	
Output Power	PO	THD = 1.0%; f = 1kHz; RL = 32Ω	-	85	-	mW
		THD = 10%; f = 1 kHz; RL= 32Ω	-	95	-	mW
Total Harmonic Distortion+ Noise	THD+N	VOUT = 1VRMS, f=1kHz, RL = 10kΩ, AVD = 1	-	0.065	-	%
Power Supply Rejection Ratio	PSRR	CB = 1.0 µF,f=120Hz, VRIPPLE =200mVrms	-	58	-	dB
Signal to Noise Ratio	SNR	POUT =75 mW, RL = 32Ω, A-Wtd Filter	-	102	-	dB
Channel Separation	XTALK	f=1kHz, CB = 1.0 µF	-	65	-	dB

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■ ELECTRICAL CHARACTERISTICS FOR BRIDGED MODE OPERATION

The following specifications apply for VDD = 5V unless otherwise noted. Limits apply for TA = 25˚C

PARAMETER	SYMBOL	TEST CONDITION	VALUE			UNIT
			MIN	TYP	MAX	
Output Offset Voltage	VOS	VIN = 0V, No Load	-	5	±50	mV
Output Power	PO	THD+N=1.0%; f=1kHz; RL=3Ω	-	2.2	-	W
		THD+N=1.0%; f=1kHz; RL=4Ω	-	2	-	W
		THD=1% (max);f=1 kHz; RL= 8Ω	1.0	1.1	-	W
		THD+N=10%;f=1 kHz; RL= 8Ω	-	1.5	-	W
Total Harmonic Distortion+ Noise	THD+N	PO = 1W, 20 Hz< f < 20 kHz,RL=8Ω, AVD=2	-	0.3	-	%
		PO=340 mW, RL = 32Ω	-	1.0	-	%
Power Supply Rejection Ratio	PSRR	CB=1.0 µF, f=120 Hz, VRIPPLE=200 mVrms; RL=8Ω	-	74	-	dB
Signal to Noise Ratio	SNR	VDD=5V, POUT=1.1W, RL=8Ω, A-Wtd Filter	-	93	-	dB
Channel Separation	XTALK	f=1kHz, CB=1.0 µF	-	70	-	dB

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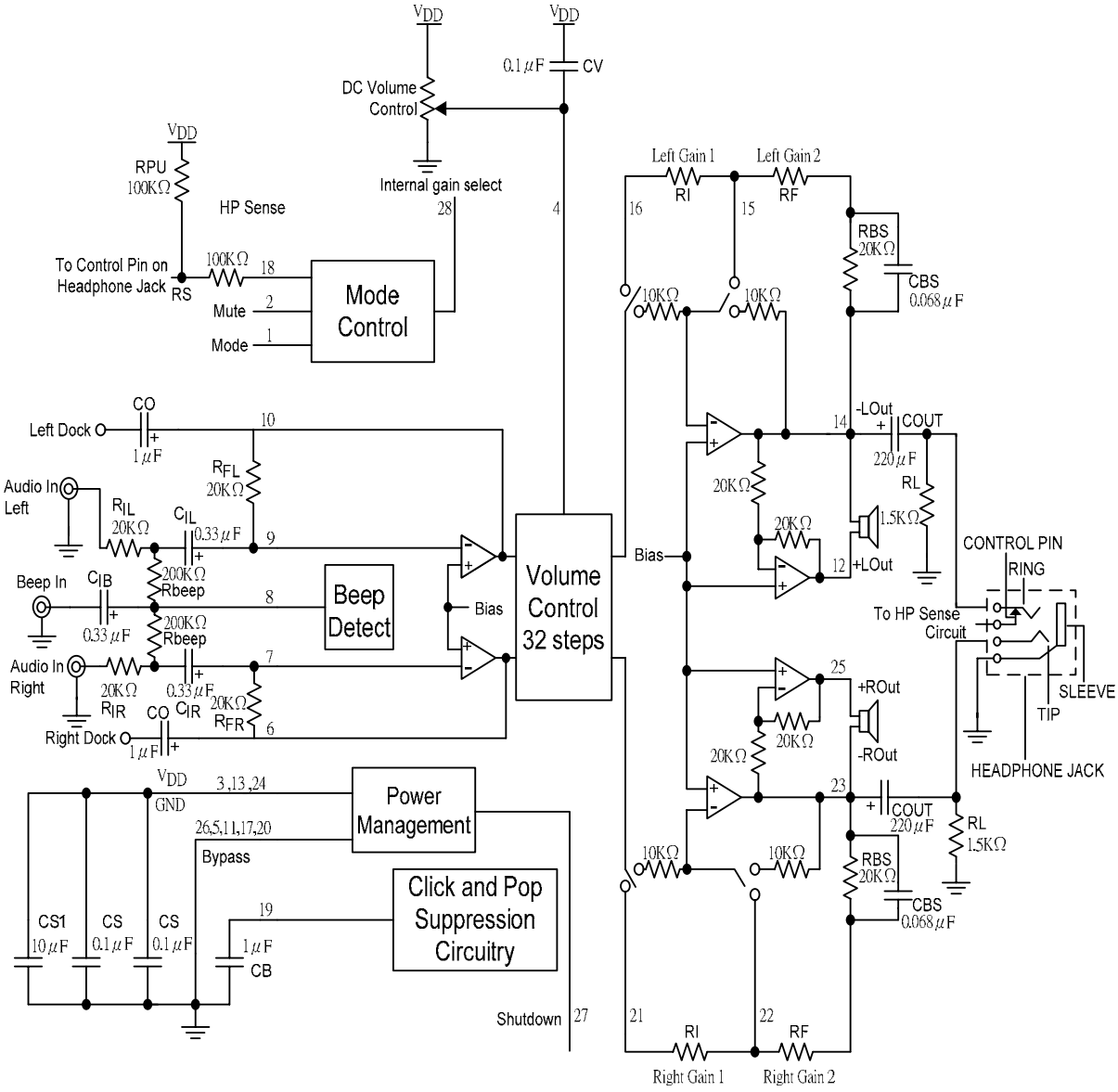
■ TYPICAL APPLICATION



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■ TRUTH TABLE FOR LOGIC INPUTS (Note)

Gain Sel	Mode	Headphone Sense	Mute	Shutdown	Output Stage Set To	DC Volume	Output Stage Configuration
0	0	0	0	0	Internal Gain	Fixed	BTL
0	0	1	0	0	Internal Gain	Fixed	SE
0	1	0	0	0	Internal Gain	Adjustable	BTL
0	1	1	0	0	Internal Gain	Adjustable	SE
1	0	0	0	0	External Gain	Fixed	BTL
1	0	1	0	0	External Gain	Fixed	SE
1	1	0	0	0	External Gain	Adjustable	BTL
1	1	1	0	0	External Gain	Adjustable	SE
X	X	X	1	0	Muted	X	Muted
X	X	X	X	1	Shutdown	X	X

Note: If system beep is detected on the Beep In pin, the system beep will be passed through the bridged amplifier regardless of the logic of the Mute and HP sense pins.

■ APPLICATION INFORMATION

• PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 3Ω AND 4Ω LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by a 4Ω load from 2.1W to 2.0W. This problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible. Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated sup- plies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

• BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 2, the AA4838 output stage consists of two pairs of operational amplifiers, forming a two-channel (channel A and channel B) stereo amplifier. (Though the following discusses channel A, it applies equally to channel B.) Figure 2 shows that the first amplifier's

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negative (-) output serves as the second amplifier's input. This results in both amplifiers producing signals identical in magnitude, but 180˚ out of phase. Taking advantage of this phase difference, a load is placed between −OUTA and +OUTA and driven differentially (commonly referred to as "bridge mode"). This result in a differential gain of **AVD=2*(Rf/Ri)…(1)**.

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. This produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or that the output signal is not clipped. To ensure minimum output signal clipping when choosing an amplifier's closed-loop gain, refer to the Audio Power Amplifier Design section. Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing channel A's and channel B's outputs at half-supply. This eliminates the coupling capacitor that single supply, single- ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

• POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier. Equation (2) states the maximum power dissipation point for a single- ended amplifier operating at a given supply voltage and driving a specified output load.

$P_{DMAX}=V_{DD}^2/2\pi^2R_L$ Single-Ended…(2)

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation for the same conditions. The AA4838 has two operational amplifiers per channel. The maximum internal power dissipation per channel operating in the bridge mode is four times that of a single-ended amplifier. From Equation (3), assuming a 5V power supply and a 4Ω load, the maximum single channel power dissipation is 1.27W or 2.54W for stereo operation.

$P_{DMAX}=4*(V_{DD})^2/2\pi^2R_L$ Bridge Mode…(3)

The AA4838's power dissipation is twice that given by Equation (2) or Equation (3) when operating in the single-ended mode or bridge mode, respectively. Twice the maximum power dissipation point given by Equation (3) must not exceed the power dissipation given by Equation (4):

$P_{DMAX}'=(T_{JMAX}-T_A)/\theta_{JA}$…(4)

The AA4838's TJMAX=150˚C. In the LQ package soldered to a DAP pad that expands to a copper area of 5in² on a PCB, the AA4838's θ_{JA} is 20˚C/W. In the MTE package soldered to

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a DAP pad that expands to a copper area of 2in² on a PCB, the AA4838MTE's θJA is 41˚C/W. For the AA4838MT package, θJA=80˚C/W. At any given ambient temperature TA, use Equation (4) to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation (4) and substituting PDMAX for PDMAX' results in Equation (5). This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the AA4838's maximum junction temperature. **TA=TJMAX–2*PDMAX θJA…(5)**.

For a typical application with a 5V power supply and a 4Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 99˚C for the LQ package and 45˚C for the MTE package.

TJMAX=PDMAX θJA+TA…(6).

Equation (6) gives the maximum junction temperature TJMAX. If the result violates the AA4838's 150˚C TJMAX, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases.

If the result of Equation (2) is greater than that of Equation (3), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θJA. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heat sinks such as the Thermally 7106D can also improve power dissipation. When adding a heat sink, the θJA is the sum of θJC, θCS, and θSA. (θJC is the junction-to-case thermal impedance, θCS is the case-to-sink thermal impedance, and θSA is the sink-to-ambient thermal impedance.) Refer to the Typical Performance Characteristics curves for power dissipation information at lower output power levels.

• POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10 µF in parallel with a 0.1 µF filter capacitor to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0µF tantalum bypass capacitance connected between the AA4838's supply pins and ground. Do not substitute a ceramic capacitor for the tantalum. Doing so may cause oscillation. Keep the length of leads and traces that connect capacitors between the AA4838's power supply pin and ground as short as possible. Connecting a 1µF

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capacitor, CB, between the BYPASS pin and ground improves the internal bias voltage's stability and the amplifier's PSRR. The PSRR improvements increase as the BYPASS pin capacitor value increases. Too large a capacitor, however, increases turn-on time and can compromise the amplifier's click and pop performance. The selection of bypass capacitor values, especially CB, depends on desired PSRR requirements, click and pop performance (as explained in the following section, Selecting Proper External Components), system cost, and size constraints.

• SELECTING PROPER EXTERNAL COMPONENTS

Optimizing the AA4838's performance requires properly selecting external components. Though the AA4838 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values. The AA4838 is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain circuits demand input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of 1VRMS (2.83VP-P). Please refer to the Audio Power Amplifier Design section for more information on selecting the proper gain.

• INPUT CAPACITOR VALUE SELECTION

Amplifying the lowest audio frequencies requires a high value input coupling capacitor (0.33μF in Figure 2), but high value capacitors can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using a large input capacitor. Besides effecting system cost and size, the input coupling capacitor has an affect on the AA4838's click and pop performance. When the supply voltage is first applied, a transient (pop) is created as the charge on the input capacitor changes from zero to a quiescent state. The magnitude of the pop is directly proportional to the input capacitor's size. Higher value capacitors need more time to reach a quiescent DC voltage (usually VDD/2) when charged with a fixed current. The amplifier's output charges the input capacitor through the feedback resistor, Rf. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired −6dB frequency.

As shown in Figure 2, the input resistor (RIR, RIL = 20k) (and the input capacitor (CIR, CIL= 0.33μF) produce a −6dB high pass filter cutoff frequency that is found using Equation (7).

$$f_{-6\,dB} = \frac{1}{2\pi R_{IN} C_I} \quad \ldots (7)$$

As an example when using a speaker with a low frequency limit of 150Hz, the input coupling capacitor, using Equation (7), is 0.053μF. The 0.33μF input coupling capacitor shown in Figure 2 allows the AA4838 to drive a high efficiency, full range speaker whose response

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extends below 30Hz.

• OPTIMIZING CLICK AND POP REDUCTION PERFORMANCE

The AA4838 contains circuitry that minimizes turn-on and shutdown transients or “clicks and pops”. For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. While the power supply is ramping to its final value, the AA838’s internal amplifiers are configured as unity-gain buffers. An internal current source changes the voltage of the BYPASS pin in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the BYPASS pin reaches 1/2 VDD. As soon as the voltage on the BYPASS pin is stable, the device becomes fully operational. Although the BYPASS pin current cannot be modified, changing the size of CB alters the device’s turn-on time and the magnitude of “clicks and pops”. Increasing the value of CB reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of CB increases, the turn-on time increases. There is a linear relationship between the size of CB and the turn-on time. Here are some typical turn-on times for various values of CB:

C	T
0.01µF	2ms
0.1µF	20ms
0.22µF	44ms
0.47µF	94ms
1.0µF	200ms

• DOCKING STATION INTERFACE

Applications such as notebook computers can take advantage of a docking station to connect to external devices such as monitors or audio/visual equipment that sends or receives line level signals. The AA4838 has two outputs, Right Dock and Left Dock, which connect to outputs of the internal input amplifiers that drive the volume control inputs. These input amplifiers can drive loads of >1kΩ(such as powered speakers) with a rail-to-rail signal. Since the output signal present on the RIGHT DOCK and LEFT DOCK pins is biased to VDD/2, coupling capacitors should be connected in series with the load when using these outputs. Typical values for the output coupling capacitors are 0.33µF to 1.0µF. If polarized coupling capacitors are used, connect their "+" terminals to the respective output pin, see Figure 2.

Since the DOCK outputs precede the internal volume control, the signal amplitude will be equal to the input signal’s magnitude and cannot be adjusted. However, the input amplifier’s closed-loop gain can be adjusted using external resistors. These 20k resistors (RFR, RFL) are shown in Figure 2 and they set each input amplifier’s gain to -1. Use Equation 7 to determine the input and feedback resistor values for a desired gain.

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AVR=RFR/RIR and - AVL=RFL/RIL… (8)

Adjusting the input amplifier's gain sets the minimum gain for that channel. Although the single ended output of the Bridge Output Amplifiers can be used to drive line level outputs, it is recommended that the R & L Dock Outputs simpler signal path be used for better performance.

• BEEP DETECT FUNCTION

Computers and notebooks produce a system "beep"signal that drives a small speaker. The speaker's auditory output signifies that the system requires user attention or input. To accommodate this system alert signal, the AA4838's beep input pin is a mono input that accepts the beep signal. Internal level detection circuitry at this input monitors the beep signal's magnitude. When a signal level greater than VDD/2 is detected on the BEEP IN pin, the bridge output amplifiers are enabled. The beep signal is amplified and applied to the load connected to the output amplifiers. A valid beep signal will be applied to the load even when MUTE is active. Use the input resistors connected between the BEEP IN pin and the stereo input pins to accommodate different beep signal amplitudes. These resistors (RBEEP) are shown as 200kΩ devices in Figure 2. Use higher value resistors to reduce the gain applied to the beep signal. The resistors must be used to pass the beep signal to the stereo inputs. The BEEP IN pin is used only to detect the beep signal's magnitude: it does not pass the signal to the output amplifiers. The AA4838's shutdown mode must be deactivated before a system alert signal is applied to BEEP IN pin.

• MICRO-POWER SHUTDOWN

The voltage applied to the SHUTDOWN pin controls the AA4838's shutdown function. Activate micro-power shutdown by applying VDD to the SHUTDOWN pin. When active, the AA4838's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The logic threshold is typically VDD/2. The low 0.7 µA typical shutdown current is achieved by applying a voltage that is as near as VDD as possible to the SHUTDOWN pin. A voltage that is less than VDD may increase the shutdown current. There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 10kΩ pull-up resistor between the SHUTDOWN pin and VDD. Connect the switch between the SHUTDOWN pin and ground. Select normal amplifier operation by closing the switch. Opening the switch connects the SHUTDOWN pin to VDD through the pull-up resistor, activating micro-power shutdown. The switch and resistor guarantee that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the need for a pull up resistor.

• MODE FUNCTION

The AA4838's MODE function has 2 states controlled by the voltage applied to the MODE pin. Mode 0, selected by applying 0V to the MODE pin, forces the AA4838 to effectively function

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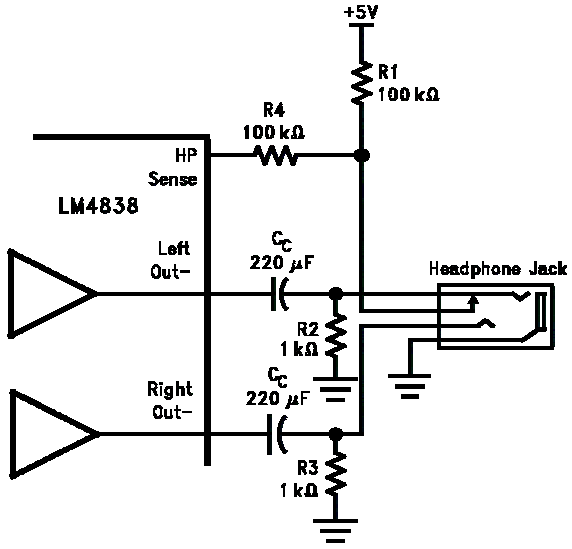
as a "line-out," unity-gain amplifier. Mode 1, which uses the internal DC controlled volume control is selected by applying VDD to the MODE pin. This mode sets the amplifier's gain according to the DC voltage applied to the DC VOL CONTROL pin. Unanticipated gain behavior can be prevented by connecting the MODE pin to VDD or ground. Note: Do not let the mode pin float.

• MUTE FUNCTION

The AA4838 mutes the amplifier and DOCK outputs when VDD is applied to the MUTE pin. Even while muted, the AA4838 will amplify a system alert (beep) signal whose magnitude satisfies the BEEP DETECT circuitry. Applying 0V to the MUTE pin returns the AA4838 to normal, unmuted operation. Prevent unanticipated mute behavior by connecting the MUTE pin to VDD or ground. Do not let the mute pain float.



• HP SENSE FUNCTION (HEAD PHONE IN)

Applying a voltage between 4V and VDD to the AA4838's HP-IN headphone control pin turns off the amps that drive the Left out "+" and Right out "+" pins. This action mutes a ridged-connected load. Quiescent current consumption is reduced when the IC is in this single-ended mode. Figure 3 shows the implementation of the AA4838's head- phone control function. With no headphones connected to the headphone jack, the R1-R2 voltage divider sets the voltage applied to the HP SENSE pin at approximately 50mV. This 50mV puts the AA4838 into bridged mode operation. The output coupling capacitor blocks the amplifier's half supply DC voltage, protecting the headphones. The HP-IN threshold is set at 4V. While the AA4838 operates in bridged mode, the DC potential across the load is essentially 0V. Therefore, even in an ideal situation, the output swing cannot cause a false single-ended trigger. Connecting headphones to the headphone jack disconnects the head phone jack contact pin from R2 and allows R1 to pull the HP Sense pin up to VDD through R4. This

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enables the headphone function, turns off both of the "+" output amplifiers, and mutes the bridged speaker. The remaining single-ended amplifiers then drive the headphones, whose impedance is in parallel with resistors R2 and R3. These resistors have negligible effect on the AA4838's output drive capability since the typical impedance of headphones is 32Ω. Figure 3 also shows the suggested headphone jack electrical connections. The jack is designed to mate with a three-wire plug. The plug's tip and ring should each carry one of the two stereo output signals, whereas the sleeve should carry the ground return. A headphone jack with one control pin contact is sufficient to drive the HP-IN pin when connecting headphones. A microprocessor or a switch can replace the headphone jack contact pin. When a microprocessor or switch applies a voltage greater than 4V to the HP-IN pin, a bridge-connected speaker is muted and the single ended output amplifiers 1A and 2A will drive a pair of headphones.

• GAIN SELECT FUNCTION (Bass Boost)

The AA4838 features selectable gain, using either internal or external feedback resistors. Either set of feedback resistors set the gain of the output amplifiers. The voltage applied to the GAIN SELECT pin controls which gain is selected. Applying VDD to the GAIN SELECT pin selects the external gain mode. Applying 0V to the GAIN SELECT pin selects the internally set unity gain. At low, frequencies CLFE is a virtual open circuit and at high frequencies, it's nearly zero ohm impedance shorts RLFE. The result is increased bridge-amplifier gain at low frequencies. The combination of RLFE and CLFE form a -6dB corner frequency at **fC=1/(2 π RLFECLFE)…(9)** The bridged-amplifier low frequency differential gain is: **AVD= 2(RF+ RLFE) / R i…(10)** Using the component values shown in Figure 1 (RF=20kΩ, RLFE = 20kΩ, and CLFE = 0.068μF), a first-order, -6dB pole is created at 120Hz. Assuming Ri=20kΩ, the low frequency differential gain is 4. The input (Ci) and output (CO) capacitor values must be selected for a low frequency response that covers the range of frequencies affected by the desired bass-boost operation. In some cases a designer may want to improve the low frequency response of the bridged amplifier or incorporate a bass boost feature. This bass boost can be useful in systems where speakers are housed in small enclosures. A resistor, RLFE, and a capacitor, CLFE, in parallel, can be placed in series with the feedback resistor of the bridged amplifier as seen in Figure 4.

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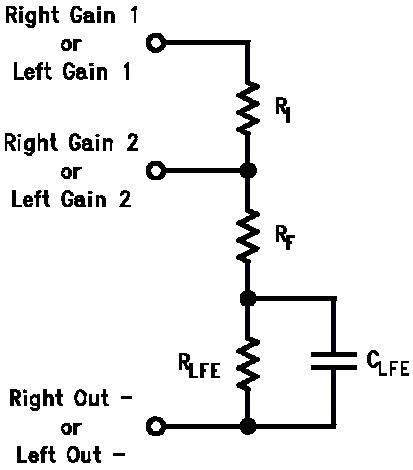

• DC VOLUME CONTROL

The AA4838 has an internal stereo volume control whose setting is a function of the DC voltage applied to the DC VOL CONTROL pin. The AA4838 volume control consists of 31 steps that are individually selected by a variable DC voltage level on the volume control pin. The range of the steps, controlled by the DC voltage, is from 0dB - 78dB. Each gain step corresponds to a specific input voltage range, as shown in table 2. To minimize the effect of noise on the volume control pin, which can affect the selected gain level, hysteresis has been implemented. The amount of hysteresis corresponds to half of the step width, as shown in Volume Control Characterization Graph (DS200133-40). For highest accuracy, the voltage shown in the 'recommended voltage' column of the table is used to select a desired gain. This recommended voltage is exactly halfway between the two nearest transitions to the next highest or next lowest gain levels. The gain levels are 1dB/step from 0dB to -6dB, 2dB/step from -6dB to -36dB, 3dB/step from -36dB to -47dB, 4dB/step from -47db to -51dB, 5dB/step from -51dB to -66dB, and 12dB to the last step at -78dB.

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• VOLUME CONTROL TABLE (Table 2)

Gain (dB)	Voltage Range (% of Vdd)			Voltage Range (Vdd = 5)			Voltage Range (Vdd = 3)		
	Low	High	Recommended	Low	High	Recommended	Low	High	Recommended
0	77.5	100.00	100.000%	3.875	5.000	5.000	2.325	3.000	3.000
-1	75.0	78.5%	76.875%	3.750	3.938	3.844	2.250	2.363	2.306
-2	72.5	76.25%	74.375%	3.625	3.813	3.719	2.175	2.288	2.231
-3	70.0	73.75%	71.875%	3.500	3.688	3.594	2.100	2.213	2.156
-4	67.5	71.25%	69.375%	3.375	3.563	3.469	2.025	2.138	2.081
-5	65.0	68.75%	66.875%	3.250	3.438	3.344	1.950	2.063	2.006
-6	62.5	66.25%	64.375%	3.125	3.313	3.219	1.875	1.988	1.931
-8	60.0	63.75%	61.875%	3.000	3.188	3.094	1.800	1.913	1.856
-10	57.5	61.25%	59.375%	2.875	3.063	2.969	1.725	1.838	1.781
-12	55.0	58.75%	56.875%	2.750	2.938	2.844	1.650	1.763	1.706
-14	52.5	56.25%	54.375%	2.625	2.813	2.719	1.575	1.688	1.631
-16	50.0	53.75%	51.875%	2.500	2.688	2.594	1.500	1.613	1.556
-18	47.5	51.25%	49.375%	2.375	2.563	2.469	1.425	1.538	1.481
-20	45.0	48.75%	46.875%	2.250	2.438	2.344	1.350	1.463	1.406
-22	42.5	46.25%	44.375%	2.125	2.313	2.219	1.275	1.388	1.331
-24	40.0	43.75%	41.875%	2.000	2.188	2.094	1.200	1.313	1.256
-26	37.5	41.25%	39.375%	1.875	2.063	1.969	1.125	1.238	1.181
-28	35.0	38.75%	36.875%	1.750	1.938	1.844	1.050	1.163	1.106
-30	32.5	36.25%	34.375%	1.625	1.813	1.719	0.975	1.088	1.031
-32	30.0	33.75%	31.875%	1.500	1.688	1.594	0.900	1.013	0.956
-34	27.5	31.25%	29.375%	1.375	1.563	1.469	0.825	0.937	0.881
-36	25.0	28.75%	26.875%	1.250	1.438	1.344	0.750	0.862	0.806
-39	22.5	26.25%	24.375%	1.125	1.313	1.219	0.675	0.787	0.731
-42	20.0	23.75%	21.875%	1.000	1.188	1.094	0.600	0.712	0.656
-45	17.5	21.25%	19.375%	0.875	1.063	0.969	0.525	0.637	0.581
-47	15.0	18.75%	16.875%	0.750	0.937	0.844	0.450	0.562	0.506
-51	12.5	16.25%	14.375%	0.625	0.812	0.719	0.375	0.487	0.431
-56	10.0	13.75%	11.875%	0.500	0.687	0.594	0.300	0.412	0.356
-61	7.5%	11.25%	9.375%	0.375	0.562	0.469	0.225	0.337	0.281
-66	5.0%	8.75%	6.875%	0.250	0.437	0.344	0.150	0.262	0.206
-78	0.0%	6.25%	0.000%	0.000	0.312	0.000	0.000	0.187	0.000

• AUDIO POWER AMPLIFIER DESIGN

Audio Amplifier Design: Driving 1W into an 8Ω Load

The following are the desired operational parameters:

Power Output: 1 WRMS, Load Impedance: 8Ω, Input Level:1 VRMS,

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Input Impedance: 20 kΩ, Bandwidth: 100 Hz−20 kHz ± 0.25 dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the Output Power vs. Supply Voltage curve in the Typical Performance Characteristics section. Another way, using Equation (10), is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the Dropout Voltage vs. Supply Voltage in the Typical Performance Characteristics curves, must be added to the result obtained by

Equation (10). The result is Equation (11).

$V_{outpeak} = \sqrt{(2R_L P_O)}$ **... (11)**,

VDD≧ (VOUTPEAK+ (VODTOP+VODBOT))... (12)

The Output Power vs. Supply Voltage graph for an 8Ω load indicates a minimum supply voltage of 4.6V. This is easily met by the commonly used 5V supply voltage. The additional voltage creates the benefit of headroom, allowing the AA4838 to produce peak output power in excess of 1W without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates of maximum power dissipation as explained above in the Power Dissipation section. After satisfying the AA4838's power dissipation requirements, the minimum differential gain needed to achieve 1W dissipation in an 8Ωload is found using Equation (12).

$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms}$ **... (13)**

Thus, a minimum overall gain of 2.83 allow the AA4838's to reach full output swing and maintain low noise and THD+N performance. The last step in this design example is setting the amplifier's −6dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are an **fL=100Hz/5=20Hz...(14)** and an **fH=20kHz x 5=100kHz...(15)** As mentioned in the Selecting Proper External Components section, Ri (Right & Left) and Ci (Right & Left) create a high pass filter that sets the amplifier's lower band pass frequency limit. Find the input coupling capacitor's value using Equation (14).

Ci≧1/(2π RifL)...(16) The result is

1/(2π *20kΩ*20Hz)=0.397μF...(17)

Use a 0.39μF capacitor, the closest standard value.

The product of the desired high frequency cutoff (100 kHz in this example) and the differential gain AVD, determines the upper pass band response limit. With AVD= 3 and fH =100 kHz, the closed-loop gain bandwidth product (GBWP) is 300 kHz. This is less than the AA4838's

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3.5MHz GBWP. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance, restricting bandwidth limitations.

• RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT

The following figures show the recommended PC board layouts that are optimized for the different package options of the AA4838 and associated external components. This circuit is designed for use with an external 5V supply and 4Ω speakers. This circuit board is easy to use. Apply 5V and ground to the board's VDD and GND pads, respectively. Connect 4Ω speakers between the board's −OUTA and +OUTA and OUTB and +OUTB pads.

■ ORDERING INFORMATION

ORDER NO.	PACKAGE	PACKING	ONE REEL Q'TY	MARK CHART
AA4838A	TSSOP 28L	Tape & Reel	2,500ea	AA4838 XXXX A

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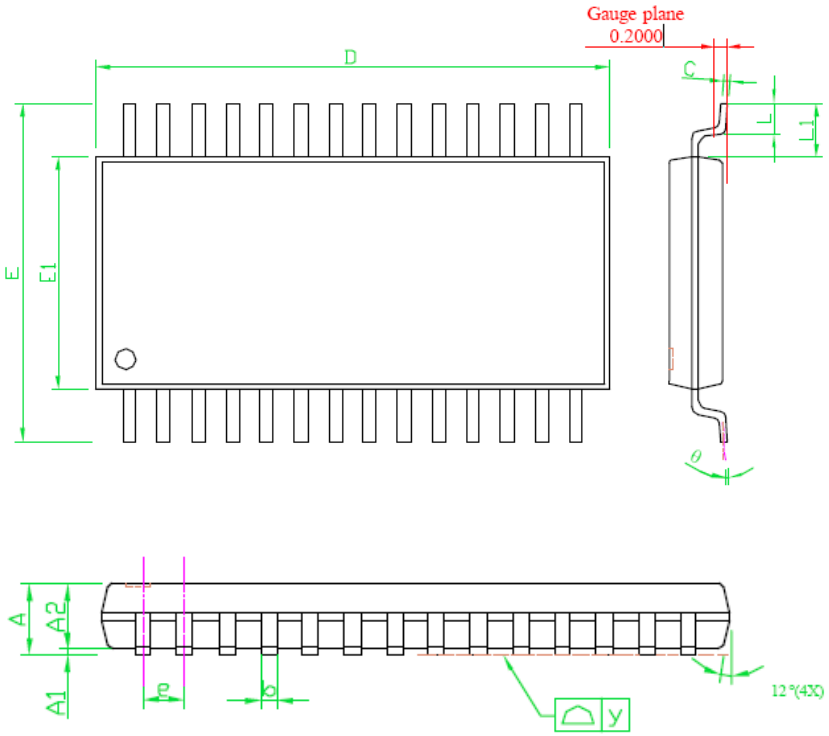
■ PACKAGE DIMENSIONS

TSSOP 28L



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.20	---	---	0.048
A1	0.05	---	0.15	0.002	---	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	---	0.30	0.007	---	0.012
C	0.09	---	0.20	0.004	---	0.008
D	9.60	9.70	9.80	0.378	0.382	0.386
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	---	0.65	---	---	0.026	---
L	0.45	0.60	0.75	0.018	0.024	0.030
y	---	---	0.10	---	---	0.004
θ	0°	---	8°	0°	---	8°
L1	0.90	1.00	1.10	0.035	0.039	0.043

NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS
2. TOLERANCE ±0.1 mm UNLESS OTHERWISE SPECIFIED
3. COPLANARITY : 0.1 mm
4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
5. FOLLOWED FROM JEDEC MO-153

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