Integrated Device Technology, Inc.

RISC CPU WRITE BUFFER

PRELIMINARY
IDT 79R2020A

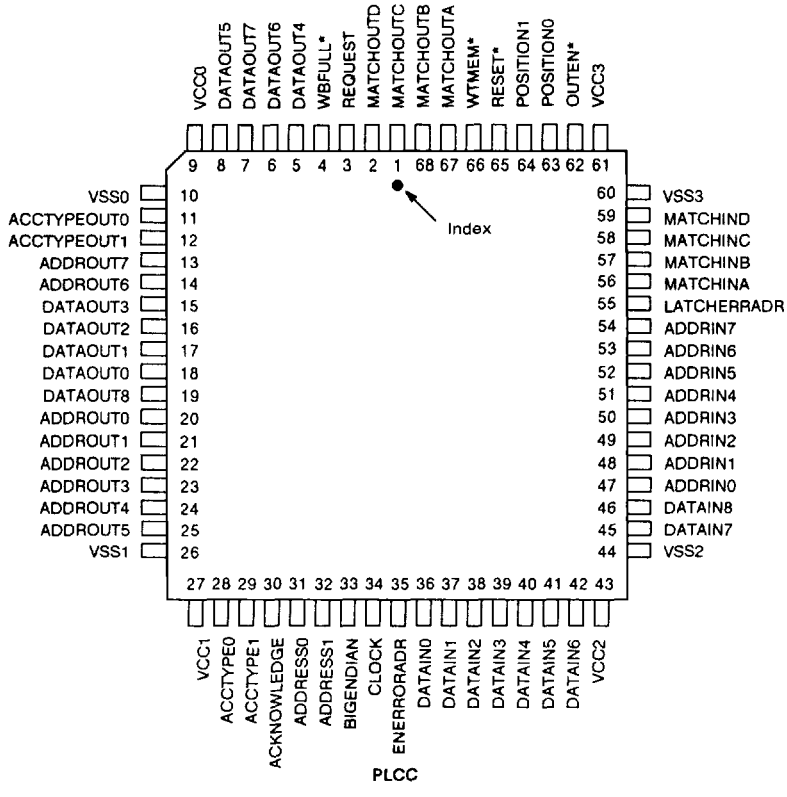
FEATURES:

- Temporary storage buffers to enhance the performance of the IDT79R2000A RISC CPU processor
- Allows for write operations by the RISC processor during Run cycles
- Each Write Buffer has four locations to handle an 8-bit address slice and a 9-bit data slice (including a parity bit)
- High-speed CEMOS™ technology
- Pin and functionally compatible with the MIPS Computer Systems R2020A Write Buffer
- Used in a 12.5 or 16.7 MHz IDT79R2000 system configuration
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

Please see the Data Sheet for 79R3020 for complete description.

PIN CONFIGURATION (TOP VIEW)



PLCC

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1, 3]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
V_{IN}	Input Voltage [2]	-0.5 to +7.0	-0.5 to +7.0	V

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = 3.0V for pulse width less than 15ns. V_{IN} should not exceed V_{CC} + 0.5 volts.
3. Not more than one output at a time should be shorted. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

DC ELECTRICAL CHARACTERISTICS – COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to + 70°C, V_{CC} = +5V± 5%)

SYMBOL	PARAMETER	TEST CONDITIONS	12.5 MHz MIN.	12.5 MHz MAX.	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4mA	3.5	–	3.5	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	–	0.4	–	0.4	V
V_{IH}	Input HIGH Voltage (1)		2.4	–	2.4	–	V
V_{IL}	Input LOW Voltage (2)		–	0.8	–	0.8	V
C_{IN}	Input Capacitance		10	–	10	–	pF
C_{OUT}	Output Capacitance		10	–	10	–	pF
I_{CC}	Operating Current	V_{CC} = Max.	–	50	–	50	mA
I_{IH}	Input HIGH Leakage	V_{IH} = V_{CC}	–	10	–	10	µA
I_{IL}	Input LOW Leakage	V_{IL} = GND	-10	–	-10	–	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	-40	40	-40	40	µA

NOTES:

1. V_{IH} should not be held above V_{CC} + 0.5 Volts.
2. V_{IL} Min. = -3.0V for less than 15ns. V_{IL} should not fall below -0.5V for longer periods.

DC ELECTRICAL CHARACTERISTICS – MILITARY TEMPERATURE RANGE (T_A = -55°C to + 125°C, V_{CC} = +5V±10%)

SYMBOL	PARAMETER	TEST CONDITIONS	12.5 MHz MIN.	12.5 MHz MAX.	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4mA	3.5	–	3.5	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	–	0.4	–	0.4	V
V_{IH}	Input HIGH Voltage (1)		2.4	–	2.4	–	V
V_{IL}	Input LOW Voltage (2)		–	0.8	–	0.8	V
C_{IN}	Input Capacitance		10	–	10	–	pF
C_{OUT}	Output Capacitance		10	–	10	–	pF
I_{CC}	Operating Current	V_{CC} = Max.	–	90	–	90	mA
I_{IH}	Input HIGH Leakage	V_{IH} = V_{CC}	–	10	–	10	µA
I_{IL}	Input LOW Leakage	V_{IL} = GND	-10	–	-10	–	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	-40	40	-40	40	µA

NOTES:

1. V_{IH} should not be held above V_{CC} + 0.5 Volts.
2. V_{IL} Min. = -3.0V for less than 15ns. V_{IL} should not fall below -0.5V for longer periods.

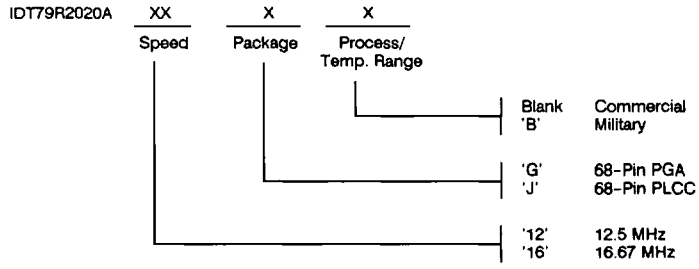
AC ELECTRICAL CHARACTERISTICS – COMMERCIAL TEMPERATURE RANGE (T_A = 0°C to + 70°C, V_{CC} = +5V± 5%)

SYMBOL	PARAMETER	12.5 MHz MIN.	12.5 MHz MAX.	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
t1	AddrIn (3:0) to Clock falling set-up	12	–	8	–	ns
t2	AddrIn (3:0) to Clock falling hold	4	–	4	–	ns
t3	Address 1:0 to Clock falling set-up	12	–	8	–	ns
t4	Address 1:0 to Clock falling hold	4	–	4	–	ns
t5	Access Type 1:0 to Clock rising set-up	10	–	7	–	ns
t6	Access Type 1:0 to Clock rising hold	4	–	3	–	ns
t7	AddrIn (7:4) to Clock rising set-up	10	–	7	–	ns
t8	AddrIn (7:4) to Clock rising hold	4	–	3	–	ns
t9	DataIn (8:0) to Clock rising set-up	10	–	7	–	ns
t10	DataIn (8:0) to Clock rising hold	4	–	3	–	ns
t11	WrtMem* to Clock rising set-up	14	–	10	–	ns
t12	WrtMem* to Clock rising hold	8	–	6	–	ns
t13	Request from Clock rising	–	35	–	32	ns
t14	Acknowledge to Clock rising set-up	15	–	12	–	ns
t15	Acknowledge to Clock rising hold	7	–	7	–	ns
t16	LatchErrAdr rising to Acknowledge	5	–	5	–	ns
t17	WbFull* active from Clock rising	–	35	–	32	ns
t18	WbFull* inactive from Clock rising	–	35	–	32	ns
t19	OutEn to AddrOut (7:0), DataOut (8:0) valid	5	20	2	15	ns
t20	OutEn to AddrOut (7:0), DataOut (8:0) tri-state	5	20	2	15	ns
t21	MatchOut (ABCD) from Clock rising	–	35	–	25	ns
t22	MatchIn (ABCD) from Clock rising set-up	15	–	10	–	ns
t23	MatchIn (ABCD) from Clock rising hold	4	–	3	–	ns
t24	EnErrAdr* to Data (error latch) valid	5	20	2	15	ns
t25	EnErrAdr* to Data (error latch) tri-state	5	20	2	15	ns
t26	Address/Data out from Clock rising	–	35	–	32	ns
t27	Reset* to Clock rising, set-up	9	–	8	–	ns
t28	Reset* from Clock rising, hold	4	–	3	–	ns
t29	Reset* low pulse width	12	–	10	–	ns
t30	WbFull* High from Clock rising (after Reset*)	3	24	3	22	ns
t31	Request* High from Reset* low	3	22	3	20	ns
t32	Access Type 1:0 low from Reset* low	3	28	3	28	ns
t33	Match Out (ABCD) low from Reset* low	3	23	3	21	ns

AC ELECTRICAL CHARACTERISTICS – MILITARY TEMPERATURE RANGE (T_A = -55°C to + 125°C, V_{CC} = +5V ± 10%)

SYMBOL	PARAMETER	12.5 MHz MIN.	12.5 MHz MAX.	16.67 MHz MIN.	16.67 MHz MAX.	UNIT
t1	AddrIn (3:0) to Clock falling setup	12	–	8	–	ns
t2	AddrIn (3:0) to Clock falling hold	4	–	4	–	ns
t3	Address 1:0 to Clock falling setup	12	–	8	–	ns
t4	Address 1:0 to Clock falling hold	4	–	4	–	ns
t5	Access Type 1:0 to Clock rising setup	10	–	7	–	ns
t6	Access Type 1:0 to Clock rising hold	4	–	3	–	ns
t7	AddrIn (7:4) to Clock rising setup	10	–	7	–	ns
t8	AddrIn (7:4) to Clock rising hold	4	–	3	–	ns
t9	DataIn (8:0) to Clock rising setup	10	–	7	–	ns
t10	DataIn (8:0) to Clock rising hold	4	–	3	–	ns
t11	WrtMem to Clock rising setup	14	–	10	–	ns
t12	WrtMem to Clock rising hold	8	–	6	–	ns
t13	Request from Clock rising	–	35	–	32	ns
t14	Acknowledge to Clock rising setup	15	–	12	–	ns
t15	Acknowledge to Clock rising hold	7	–	7	–	ns
t16	LatchErrAdr rising to Acknowledge	5	–	5	–	ns
t17	WbFull active from Clock rising	–	35	–	32	ns
t18	WbFull inactive from Clock rising	–	35	–	32	ns
t19	OutEn to AddrOut (7:0), DataOut (8:0) valid	5	20	2	15	ns
t20	OutEn to AddrOut (7:0), DataOut (8:0) tri-state	5	20	2	15	ns
t21	MatchOut (ABCD) from Clock rising	–	35	–	25	ns
t22	MatchIn (ABCD) from Clock rising setup	15	–	10	–	ns
t23	MatchIn (ABCD) from Clock rising hold	4	–	3	–	ns
t24	EnErrAdr to Data (error latch) valid	5	20	2	15	ns
t25	EnErrAdr to Data (error latch) tri-state	5	20	2	15	ns
t26	Address/Data out from Clock rising	–	35	–	32	ns
t27	Reset* to Clock rising, set-up	9	–	8	–	ns
t28	Reset* from Clock rising, hold	4	–	3	–	ns
t29	Reset* low pulse width	12	–	10	–	ns
t30	WbFull* High from Clock rising (after Reset*)	3	24	10	22	ns
t31	Request* High from Reset* low	3	22	10	20	ns
t32	Access Type 1:0 low from Reset* low	3	28	12	28	ns
t33	Match Out (ABCD) low from Reset* low	3	23	10	21	ns

ORDERING INFORMATION



9