NEC

MOS INTEGRATED CIRCUIT

μPD78052Y, 78053Y, 78054Y, 78055Y, 78056Y, 78058Y

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78052Y, 78053Y, 78054Y, 78055Y, 78056Y, and 78058Y are the μPD78054Y subseries products of the 78K/0 series.

Various peripheral hardware such as 8-bit resolution D/A converter, timer, serial interface (I^2C bus mode compatible), real-time output port and interrupt functions are incorporated.

The μPD78P054Y, 78P058Y, a one-time PROM or EPROM version which can be operated in the same supply voltage range as for the mask ROM version, and various development tools are also available.

Detailed function descriptions, etc., are provided in the following User's Manual. Be sure to read it when designing.

μPD78054, 78054Y Subseries User's Manual : IEU-1356
78K/0 Series User's Manual Instructions : IEU-1372

FEATURES

- Internal high-capacity ROM and RAM

Item / Part number	Program memory (ROM)	Data memory		
		Internal High-Speed RAM	Buffer RAM	Internal Expanded RAM
μPD78052Y	16 Kbytes	512 bytes	32 bytes	No
μPD78053Y	24 Kbytes	1024 bytes		
μPD78054Y	32 Kbytes			
μPD78055Y	40 Kbytes			
μPD78056Y	48 Kbytes			
μPD78058Y	60 Kbytes			1024 bytes

- External memory expansion space : 64 Kbytes
- Instruction execution time can be varied from high-speed (0.4 μs) to ultra-low-speed (122 μs)
- I/O ports : 69 (N-ch open-drain : 4)
- 8-bit resolution A/D converter: 8 channels
- 8-bit resolution D/A converter: 2 channels
- Serial interface : 3 channels (I^2C bus mode : 1 channel)
- Timer : 5 channels
- Supply voltage : V_{DD} = 2.0 to 6.0 V

APPLICATIONS

Cellular phones, pagers, printers, AV equipment, airconditioners, cameras, PPC, fuzzy home applicances, vending machines, etc.

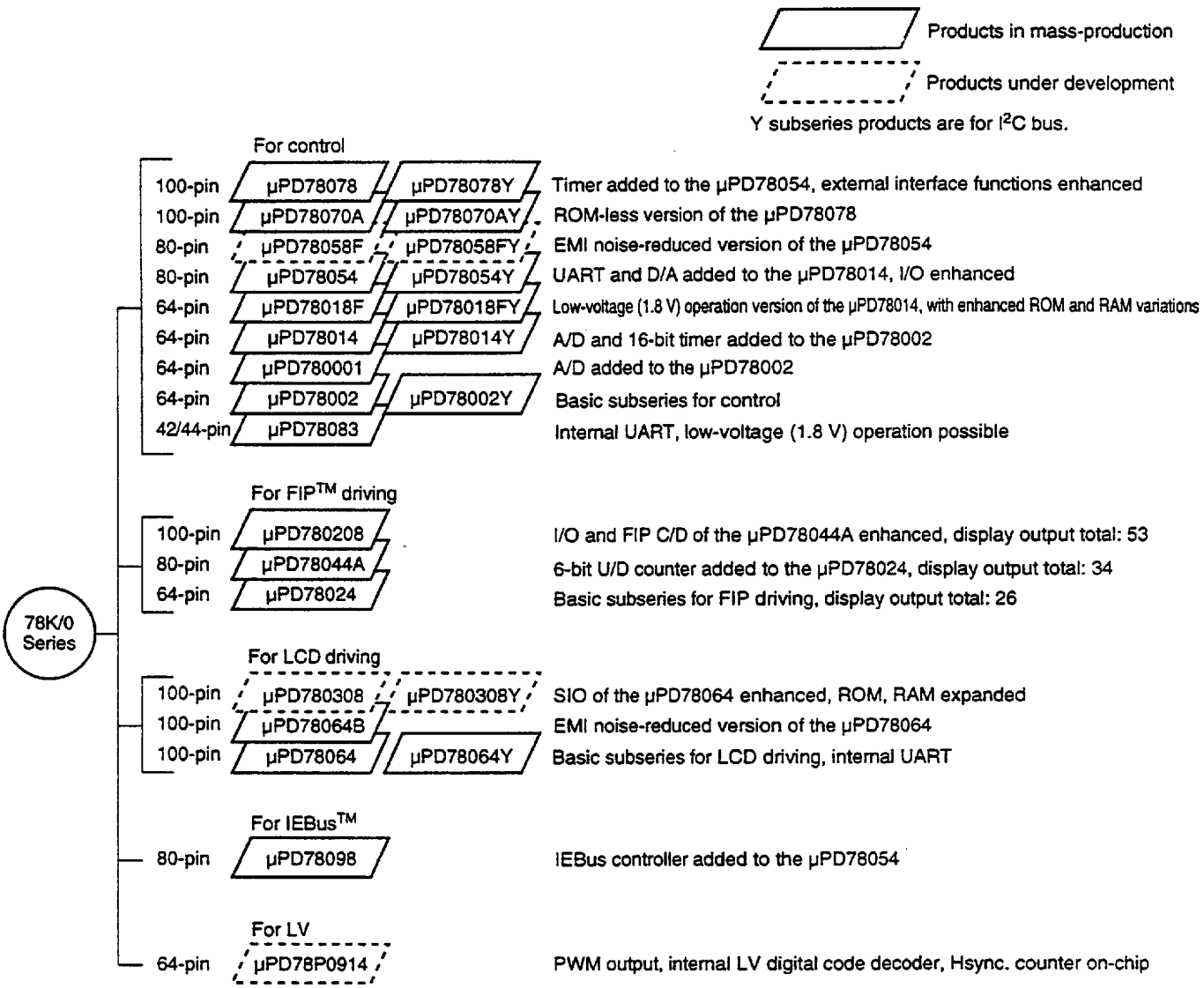
ORDERING INFORMATION

Part Number	Package
μPD78052YGC-xxx-3B9	80-pin plastic QFP (14 x 14 mm)
μPD78053YGC-xxx-3B9	80-pin plastic QFP (14 x 14 mm)
μPD78054YGC-xxx-3B9	80-pin plastic QFP (14 x 14 mm)
μPD78055YGC-xxx-3B9	80-pin plastic QFP (14 x 14 mm)
μPD78056YGC-xxx-3B9	80-pin plastic QFP (14 x 14 mm)
μPD78058YGC-xxx-3B9	80-pin plastic QFP (14 x 14 mm)

Remark xxx indicates the ROM code suffix.

78K/0 SERIES PRODUCT DEVELOPMENT

The following shows the products of the 78K/0 Series. The designations appearing inside the boxes are subseries names.



The major functional differences among the subseries are shown below.

Name \ Function		ROM	Timer				8-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT						
For control	μPD78078	32 K to 60 K	4 ch	1 ch	1 ch	1 ch	8 ch	2 ch	3 ch (UART : 1 ch)	88	1.8 V	√
	μPD78070A	–								61	2.7 V	
	μPD78058F	48 K to 60 K	2 ch							69		
	μPD78054	16 K to 60 K									2.0 V	
	μPD78018F	8 K to 60 K						–	2 ch	53	1.8 V	
	μPD78014	8 K to 32 K									2.7 V	
	μPD780001	8 K		–	–				1 ch	39		–
	μPD78002	8 K to 16 K			1 ch		–			53		√
	μPD78083				–		8 ch		1 ch (UART : 1 ch)	33	1.8 V	–
For FIP driving	μPD780208	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	74	2.7 V	–
	μPD78044A	16 K to 40 K								68		
	μPD78024	24 K to 32 K								54		
For LCD driving	μPD780308	48 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	3 ch (UART : 1 ch)	57	1.8 V	–
	μPD78064B	32 K							2 ch (UART : 1 ch)		2.0 V	
	μPD78064	16 K to 32 K										
For IEBus	μPD78098	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	2 ch	3 ch (UART : 1 ch)	69	2.7 V	√
For LV	μPD78P0914	32 K	6 ch	–	–	1 ch	8 ch	–	2 ch	54	4.5 V	√

FUNCTIONAL OVERVIEW

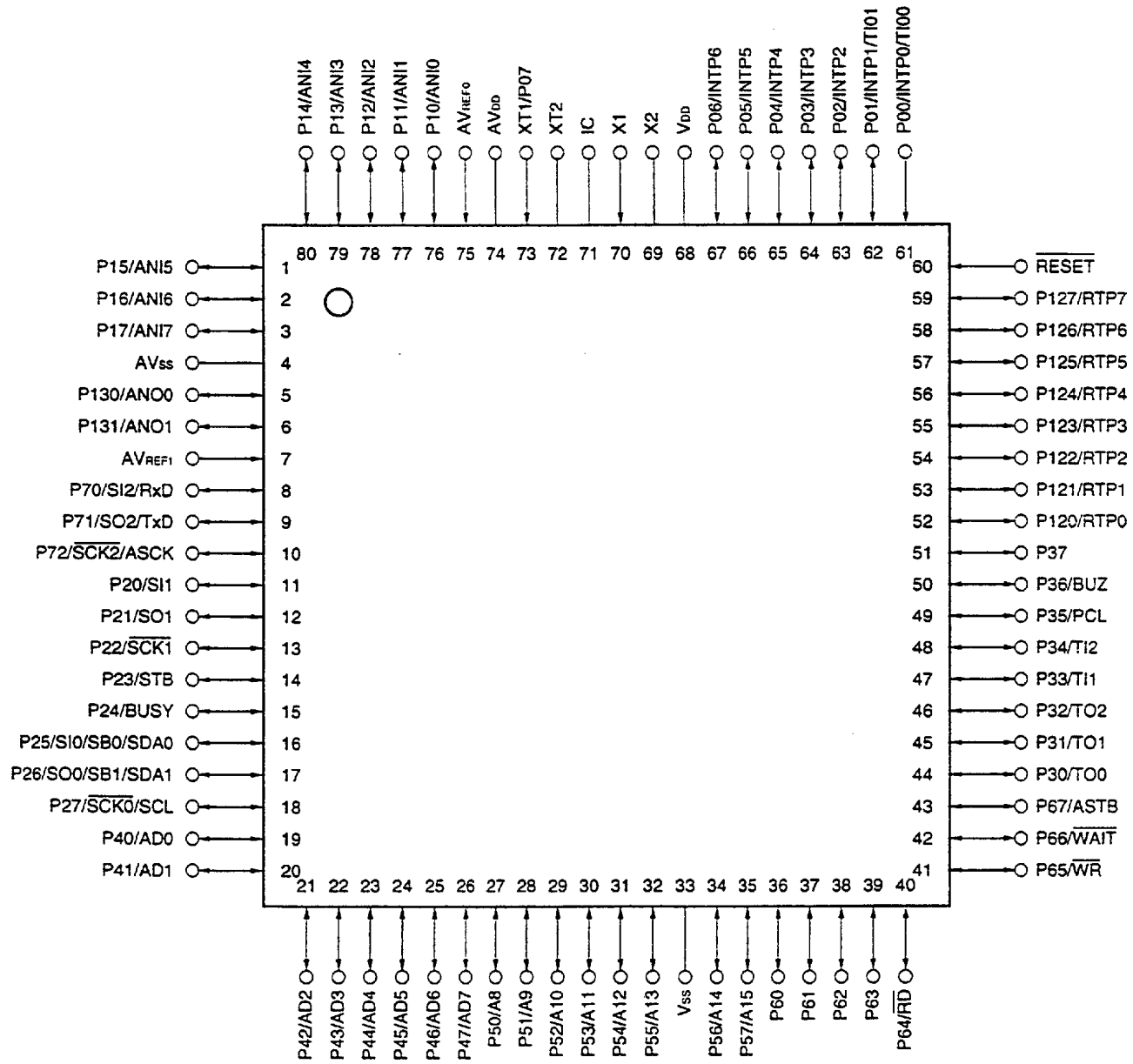
Item \ Product Name		μPD78052Y	μPD78053Y	μPD78054Y	μPD78055Y	μPD78056Y	μPD78058Y
Internal memory	ROM	16 Kbytes	24 Kbytes	32 Kbytes	40 Kbytes	48 Kbytes	60 Kbytes
	Internal high-speed RAM	512 bytes	1024 bytes				
	Buffer RAM	32 bytes					
	Internal expanded RAM	None					1024 bytes
Memory space		64 Kbytes					
General registers		8 bits x 32 registers (8 bits x 8 registers x 4 banks)					
Instruction cycle		On-chip instruction execution time cycle modification function					
	When main system clock selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@ 5.0-MHz operation)					
	When subsystem clock selected	122 μs (@ 32.768-kHz operation)					
Instruction set		• 16-bit operation • Multiply/divide (8 bits x 8 bits, 16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, boolean operation) • BCD adjust, etc.					
I/O ports		Total : 69 • CMOS input : 2 • CMOS I/O : 63 • N-ch open-drain I/O : 4					
A/D converter		• 8-bit resolution x 8 channels					
D/A converter		• 8-bit resolution x 2 channels					
Serial interface		• 3-wire/2-wire/I²C bus mode selectable: 1 channel • 3-wire mode (on-chip max. 32 bytes automatic data transmit/receive function): 1 channel • 3-wire/UART mode selectable : 1 channel					
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel					
Timer output		3 (14-bit PWM output x 1)					
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (@5.0-MHz operation with main system clock) 32.768 kHz (@32.768-kHz operation with subsystem clock)					
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (@5.0-MHz operation with main system clock)					
Vectored interrupts	Maskable interrupts	Internal interrupt : 13, external interrupt : 7					
	Non-maskable interrupts	Internal interrupt : 1					
	Software interrupts	Internal interrupt : 1					
Test input		Internal : 1, external : 1					
Power supply voltage		V_{DD} = 2.0 to 6.0 V					
Operating ambient temperature		T_A = −40 to +85 °C					
Package		80-pin plastic QFP (14 x 14 mm)					

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- **80-pin plastic QFP (14 x 14 mm)**

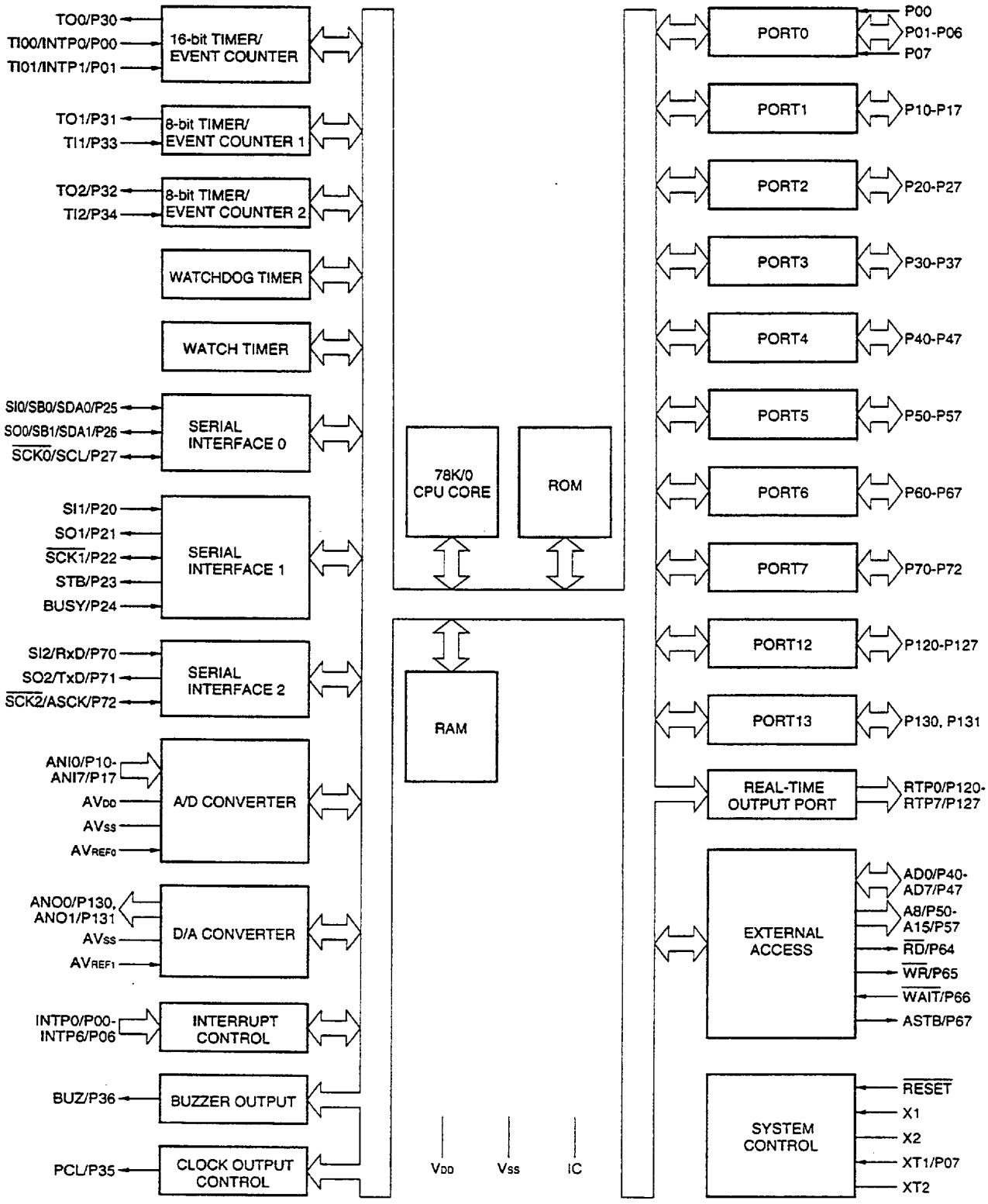
μPD78052YGC-xxx-3B9
μPD78053YGC-xxx-3B9
μPD78054YGC-xxx-3B9
μPD78055YGC-xxx-3B9
μPD78056YGC-xxx-3B9
μPD78058YGC-xxx-3B9



Cautions
1. **IC (Internally Connected) pin should be connected directly to Vss.**
2. **AVDD pin should be connected to VDD pin.**
3. **AVss pin should be connected to Vss pin.**

P00 to P07	:	Port0
P10 to P17	:	Port1
P20 to P27	:	Port2
P30 to P37	:	Port3
P40 to P47	:	Port4
P50 to P57	:	Port5
P60 to P67	:	Port6
P70 to P72	:	Port7
P120 to P127	:	Port12
P130, P131	:	Port13
RTP0 to RTP7	:	Real-Time Output Port
INTP0 to INTP6	:	Interrupt from Peripherals
TI00, TI01	:	Timer Input
TI1, TI2	:	Timer Input
TO0 to TO2	:	Timer Output
SB0, SB1	:	Serial Bus
SI0 to SI2	:	Serial Input
SO0 to SO2	:	Serial Output
$\overline{SCK0}$ to $\overline{SCK2}$	:	Serial Clock
SCL	:	Serial Clock
SDA0, SDA1	:	Serial Data
RxD	:	Receive Data
TxD	:	Transmit Data
ASCK	:	Asynchronous Serial Clock
PCL	:	Programmable Clock
BUZ	:	Buzzer Clock
STB	:	Strobe
BUSY	:	Busy
AD0 to AD7	:	Address/Data Bus
A8 to A15	:	Address Bus
$\overline{RD}$	:	Read Strobe
$\overline{WR}$	:	Write Strobe
$\overline{WAIT}$	:	Wait
ASTB	:	Address Strobe
X1, X2	:	Crystal (Main System Clock)
XT1, XT2	:	Crystal (Subsystem Clock)
$\overline{RESET}$	:	Reset
ANI0 to ANI7	:	Analog Input
ANO0, ANO1	:	Analog Output
AV_{DD}	:	Analog Power Supply
AV_{SS}	:	Analog Ground
$AV_{REF0,1}$	:	Analog Reference Voltage
V_{DD}	:	Power Supply
V_{SS}	:	Ground
IC	:	Internally Connected

2. BLOCK DIAGRAM



Remark The internal ROM and RAM capacity depends on the product.

3. PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P00	Input	Port 0 8-bit I/O port	Input only	Input	INTP0/TI00
P01	Input/ output		Input/output can be specified bit-wise. When used as an input port, internal pull-up resistor can be connected by software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P06					INTP6
P07[Note 1]	Input		Input only	Input	XT1
P10 to P17	Input/ output	Port 1 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, internal pull-up resistor can be connected by software.[Note 2]		Input	ANI0 to ANI7
P20	Input/ output	Port 2 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, internal pull-up resistor can be connected by software.		Input	SI1
P21					SO1
P22					$\overline{SCK1}$
P23					STB
P24					BUSY
P25					SI0/SB0/SDA0
P26					SO0/SB1/SDA1
P27					$\overline{SCK0}$/SCL
P30	Input/ output	Port 3 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, internal pull-up resistor can be connected by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—
P40 to P47	Input/ output	Port 4 8-bit input/output port. Input/output can be specified in 8-bit units. When used as an input port, internal pull-up resistor can be connected by software. Test input flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7

Notes 1. When using the P07/XT1 pins as an input port, set 1 in bit 6 (FRC) of the processor clock control register (PCC). On-chip feedback resistor of the subsystem clock oscillator should not be used.

2. When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input pins, the pull-up resistor is disabled automatically.

3.1 PORT PINS (2/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P50 to P57	Input/ output	Port 5 8-bit input/output port. LEDs can be driven directly. Input/output can be specified bit-wise. When used as an input port, internal pull-up resistor can be connected by software.		Input	A8 to A15
P60	Input/ output	Port 6 8-bit input/outport port. Input/output can be specified bit-wise.	N-ch open-drain input/output port. On-chip pull-up resistor can be specified by mask option. LEDs can be driven directly.	Input	—
P61					
P62					
P63					
P64			When used as an input port, internal pull-up resistor can be connected by software.	Input	$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB
P70	Input/ output	Port 7 3-bit input/output port. Input/output can be specified bit-wise. When used as an input port, internal pull-up resistor can be connected by software.		Input	SI2/RxD
P71					SO2/TxD
P72					$\overline{SCK2}$/ASCK
P120 to P127	Input/ output	Port 12 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, internal pull-up resistor can be connected by software.		Input	RTP0 to RTP7
P130, P131	Input/ output	Port 13 2-bit input/output port. Input/output can be specified bit-wise. When used as an input port, internal pull-up resistor can be connected by software.		Input	ANO0, ANO1

3.2 NON-PORT PINS (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input by which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
INTP6				P06
SI0	Input	Serial interface serial data input.	Input	P25/SB0/SDA0
SI1				P20
SI2				P70/RxD
SO0	Output	Serial interface serial data output.	Input	P26/SB1/SDA1
SO1				P21
SO2				P71/TxD
SB0	Input /output	Serial interface serial data input/output.	Input	P25/SI0/SDA0
SB1				P26/SO0/SDA1
SDA0				P25/SI0/SB0
SDA1				P26/SO0/SB1
$\overline{SCK0}$	Input /output	Serial interface serial clock input/output	Input	P27/SCL
$\overline{SCK1}$				P22
$\overline{SCK2}$				P72/ASCK
SCL				P27/$\overline{SCK0}$
STB	Output	Serial interface automatic transmit/receive strobe output.	Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input.	Input	P24
RxD	Input	Asynchronous serial interface serial data input.	Input	P70/SI2
TxD	Output	Asynchronous serial interface serial data output.	Input	P71/SO2
ASCK	Input	Asynchronous serial interface serial clock input.	Input	P72/$\overline{SCK2}$
TI00	Input	External count clock input to the 16-bit timer (TM0)	Input	P00/INTP0
TI01		Capture trigger signal input to the capture register (CR00)		P01/INTP1
TI1		External count clock input to the 8-bit timer (TM1)		P33
TI2		External count clock input to the 8-bit timer (TM2)		P34
TO0	Output	16-bit timer output (dual-function as 14-bit PWM output)	Input	P30
TO1		8-bit timer output		P31
TO2				P32
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
RTP0 to RTP7	Output	Real-time output port by which data is output in synchronization with a trigger.	Input	P120 to P127
AD0 to AD7	Input /output	Low-order address/data bus at external memory expansion.	Input	P40 to P47

3.2 NON-PORT PINS (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
A8 to A15	Output	High-order address bus at external memory expansion.	Input	P50 to P57
$\overline{RD}$	Output	External memory read operation strobe signal output.	Input	P64
$\overline{WR}$		External memory write operation strobe signal output.		P65
$\overline{WAIT}$	Input	Wait insertion at external memory access.	Input	P66
ASTB	Output	Strobe output which latches the address information output at port 4 and port 5 to access external memory.	Input	P67
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
ANO0, ANO1	Output	D/A converter analog output.	Input	P130, P131
AV_{REF0}	Input	A/D converter reference voltage input.	—	—
AV_{REF1}	Input	D/A converter reference voltage input.	—	—
AV_{DD}	—	A/D converter analog power supply. Connected to V_{DD}	—	—
AV_{SS}	—	A/D converter ground potential. Connected to V_{SS}	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection.	Input	P07
XT2	—		—	—
V_{DD}	—	Positive power supply.	—	—
V_{SS}	—	Ground potential.	—	—
IC	—	Internal connection. Connect to Vss directly.	—	—

★ 3.3 PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, see Figure 3-1.

Table 3-1. Input/Output Circuit Type of Each Pin (1/2)

Pin Name	Input/output Circuit Type	I/O	Recommended Connection when Not Used
P00/INTP0/TI00	2	Input	Connected to Vss.
P01/INTP1/TI01	8-A	Input/output	Independently connected to Vss through resistor.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P06/INTP6			
P07/XT1	16	Input	Connected to VDD.
P10/ANI0 to P17/ANI7	11	Input/output	Independently connected to VDD or Vss through resistor.
P20/SI1	8-A		
P21/SO1	5-A		
P22/$\overline{SCK1}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0/SDA0	10-A		
P26/SO0/SB1/SDA1			
P27/$\overline{SCK0}$/SCL			
P30/TO0	5-A		
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0 to P47/AD7	5-E		Independently connected to VDD through resistor.
P50/A8 to P57/A15	5-A		Independently connected to VDD or Vss through resistor.
P60 to P63	13-B		Independently connected to VDD through resistor.
P64/$\overline{RD}$	5-A		Independently connected to VDD or Vss through resistor.
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			

Table 3-1. Input/Output Circuit Type of Each Pin (2/2)

Pin Name	Input/output Circuit Type	I/O	Recommended Connection when Not Used
P70/SI2/RxD	8-A	Input/output	Independently connected to V_{DD} or Vss through resistor.
P71/SO2/TxD	5-A		
P72/$\overline{SCK2}$/ASCK	8-A		
P120/RTP0 to P127/RTP7	5-A		
P130/ANO0, P131/ANO1	12-A		Independently connected to Vss through resistor.
$\overline{RESET}$	2	Input	—
XT2	16	—	Leave open.
AV_{REF0}	—		Connected to Vss.
AV_{REF1}			Connected to V_{DD}.
AV_{DD}			
AVss			Connected to Vss.
IC			Connected to Vss directly.

Figure 3-1. Pin Input/Output Circuits (1/2)

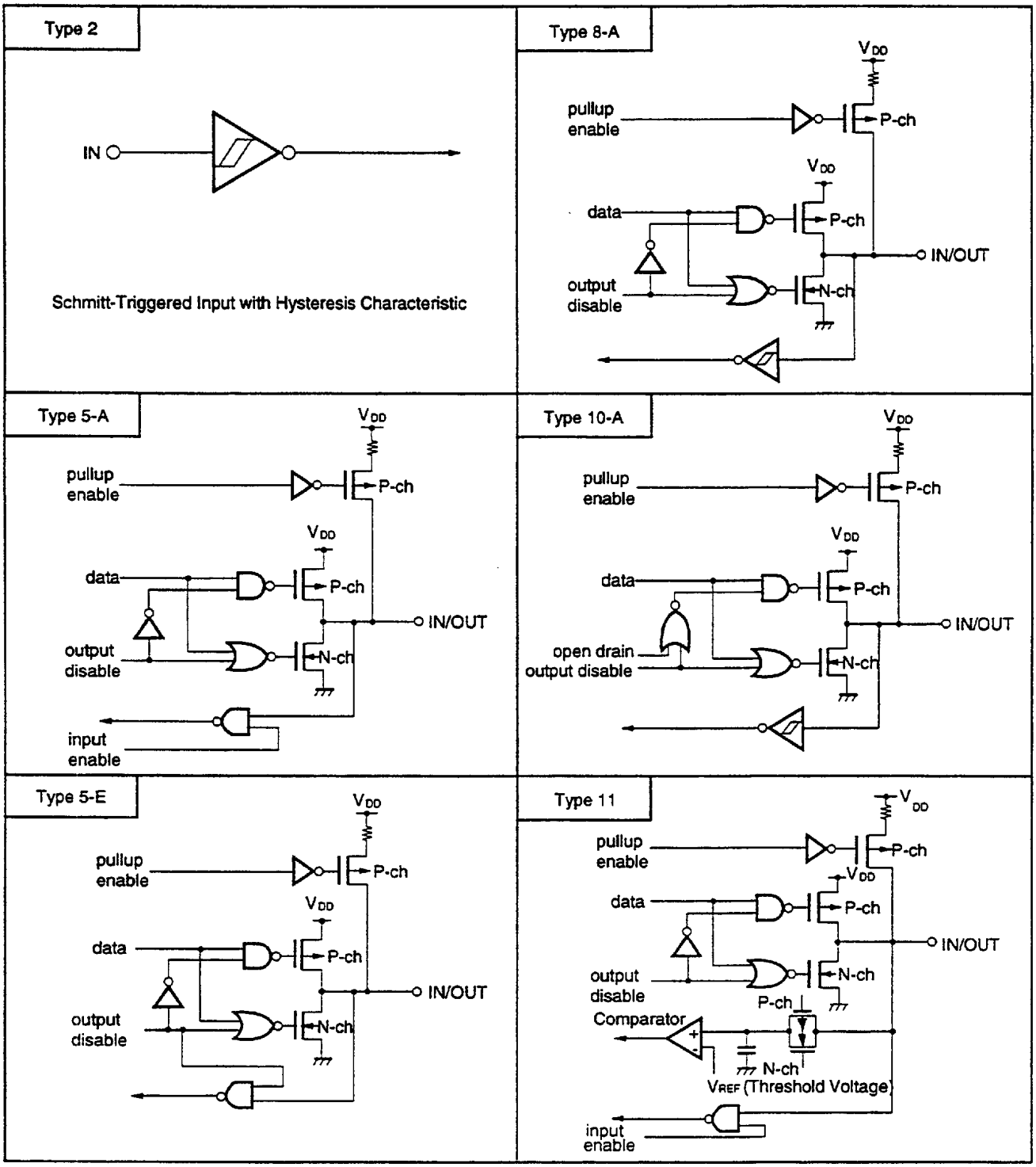
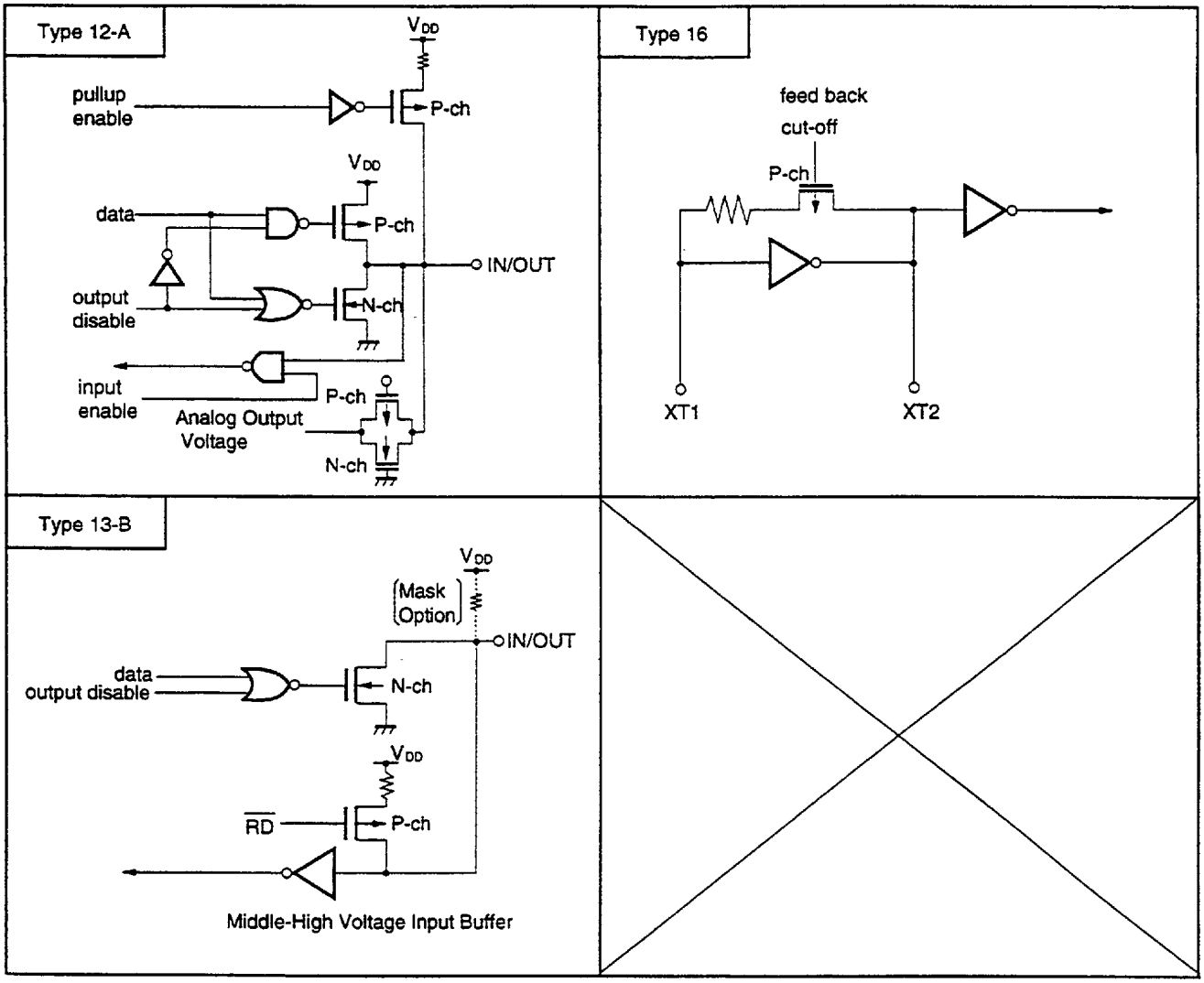


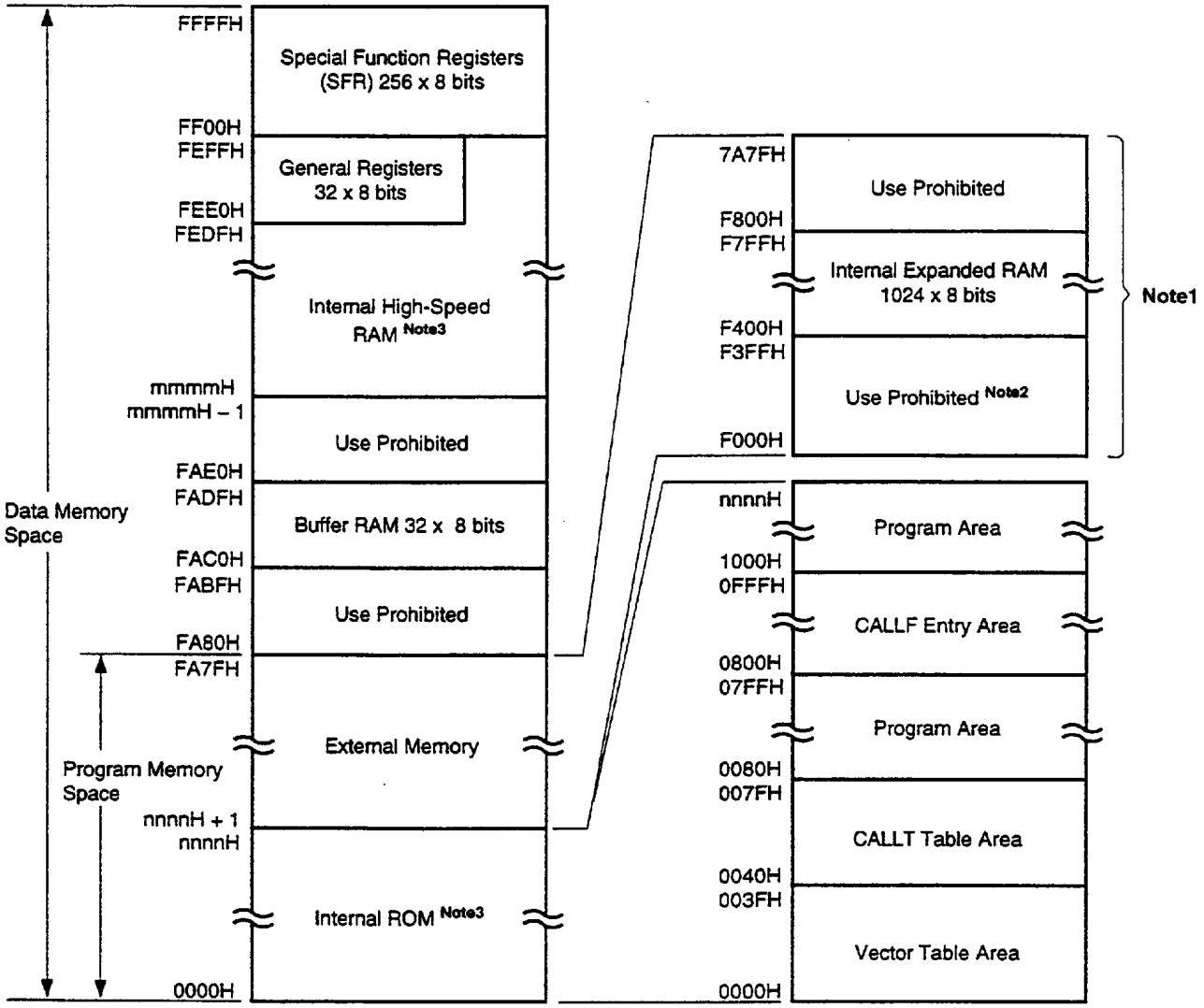
Figure 3-1. Pin Input/Output Circuits (2/2)



4. MEMORY SPACE

Figure 4-1 shows the μPD78052Y/78053Y/78054Y/78055Y/78056Y/78058Y memory map.

Figure 4-1. Memory Map



Notes 1. Provided in the μPD78058Y only

2. When the external device expansion function is used with the μPD78058Y, set the internal ROM capacity to 56 Kbytes or less using the internal memory size switching register (IMS).
3. The internal ROM capacity and internal high-speed RAM capacity depend on the products (see the next table).

Relevant Product Name	Internal ROM Last Address nnnnH	Internal High-Speed RAM First Address mmmmH
μPD78052Y	3FFFH	FD00H
μPD78053Y	5FFFH	FB00H
μPD78054Y	7FFFH	
μPD78055Y	9FFFH	
μPD78056Y	BFFFH	
μPD78058Y	EFFFH	

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 PORTS

The following 3 types of I/O ports are available.

- CMOS input (P00, P07) : 2
- CMOS input/output (P01 to P06, port 1 to port 5, P64 to P67, port 7, port 12, port 13) : 63
- N-channel open-drain input/output (P60 to P63) : 4

Total : 69

Table 5-1. Port Functions

Name	Pin Name	Function
Port 0	P00, P07	Dedicated input port pins
	P01 to P06	Input/output port pins. Input/output specifiable bit-wise. When used as input/output port pins, on-chip pull-up resistor can be connected by software.
Port 1	P10 to P17	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be connected by software.
Port 2	P20 to P27	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be connected by software.
Port 3	P30 to P37	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be connected by software.
Port 4	P40 to P47	Input/output port pins. Input/output specifiable in 8-bit units. When used as input port pins, on-chip pull-up resistor can be connected by software. Test input flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be connected by software. LEDs direct drive capability.
Port 6	P60 to P63	N-channel open-drain input/output port pins. Input/output specifiable bit-wise. On-chip pull-up resistor can be connected by mask option. LEDs direct drive capability.
	P64 to P67	Input/output port pins. Input/output specifiable bit-wise. When used as input/output port pins, on-chip pull-up resistor can be connected by software.
Port 7	P70 to P72	Input/output port pins. Input/output specifiable bit-wise. When used as input/output port pins, on-chip pull-up resistor can be connected by software.
Port 12	P120 to P127	Input/output port pins. Input/output specifiable bit-wise. When used as input/output port pins, on-chip pull-up resistor can be connected by software.
Port 13	P130, P131	Input/output port pins. Input/output specifiable bit-wise. When used as input/output port pins, on-chip pull-up resistor can be connected by software.

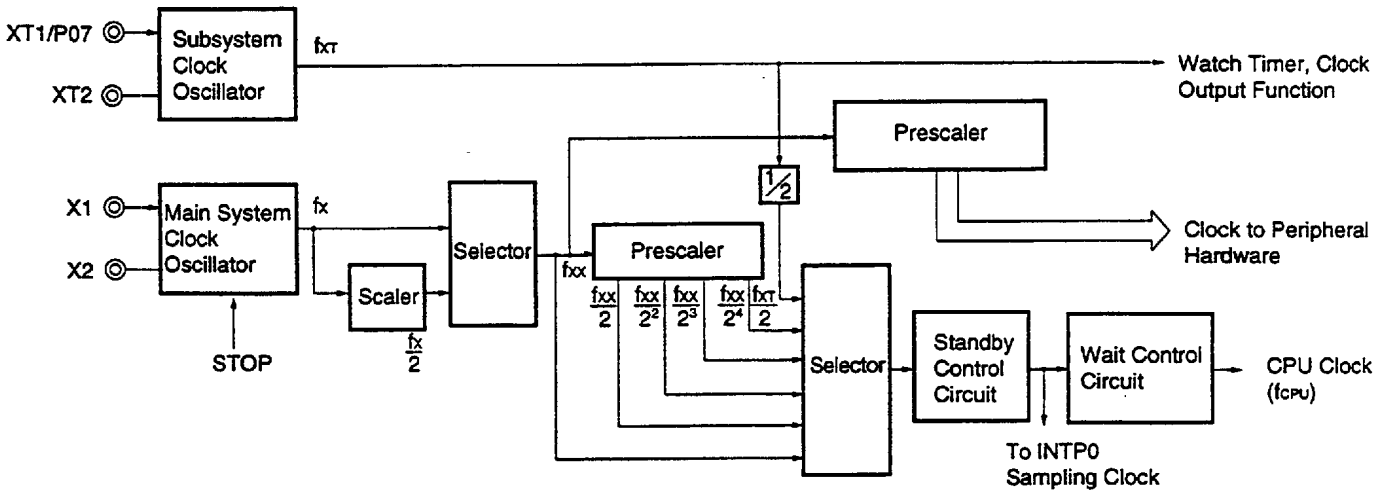
5.2 CLOCK GENERATOR

Two types of generators, a main system clock generator and a subsystem clock generator, are avaibable.

The instruction execution time can also be changed.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@5.0-MHz operation with main system clock)
- 122 μs (@32.768-kHz operation with subsystem clock)

* **Figure 5-1. Clock Generator Block Diagram**



5.3 TIMER/EVENT COUNTER

5 timer/event counter channels are incorporated.

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2. Types and Functions of Timer/Event Counter

	16-Bit Timer/Event Counter	8-Bit Timer/Event Counter	Watch Timer	Watchdog Timer
Type				
Interval timer	1 channel	2 channels	1 channel	1 channel
External event counter	1 channel	2 channels	—	—
Function				
Timer output	1 output	2 outputs	—	—
PWM output	1 output	—	—	—
Pulse width measurement	2 inputs	—	—	—
Square wave output	1 output	2 outputs	—	—
One-shot pulse output	1 output	—	—	—
Interrupt request	2	2	1	1
Test input	—	—	1	—

Figure 5-2. 16-Bit Timer/Event Counter Block Diagram

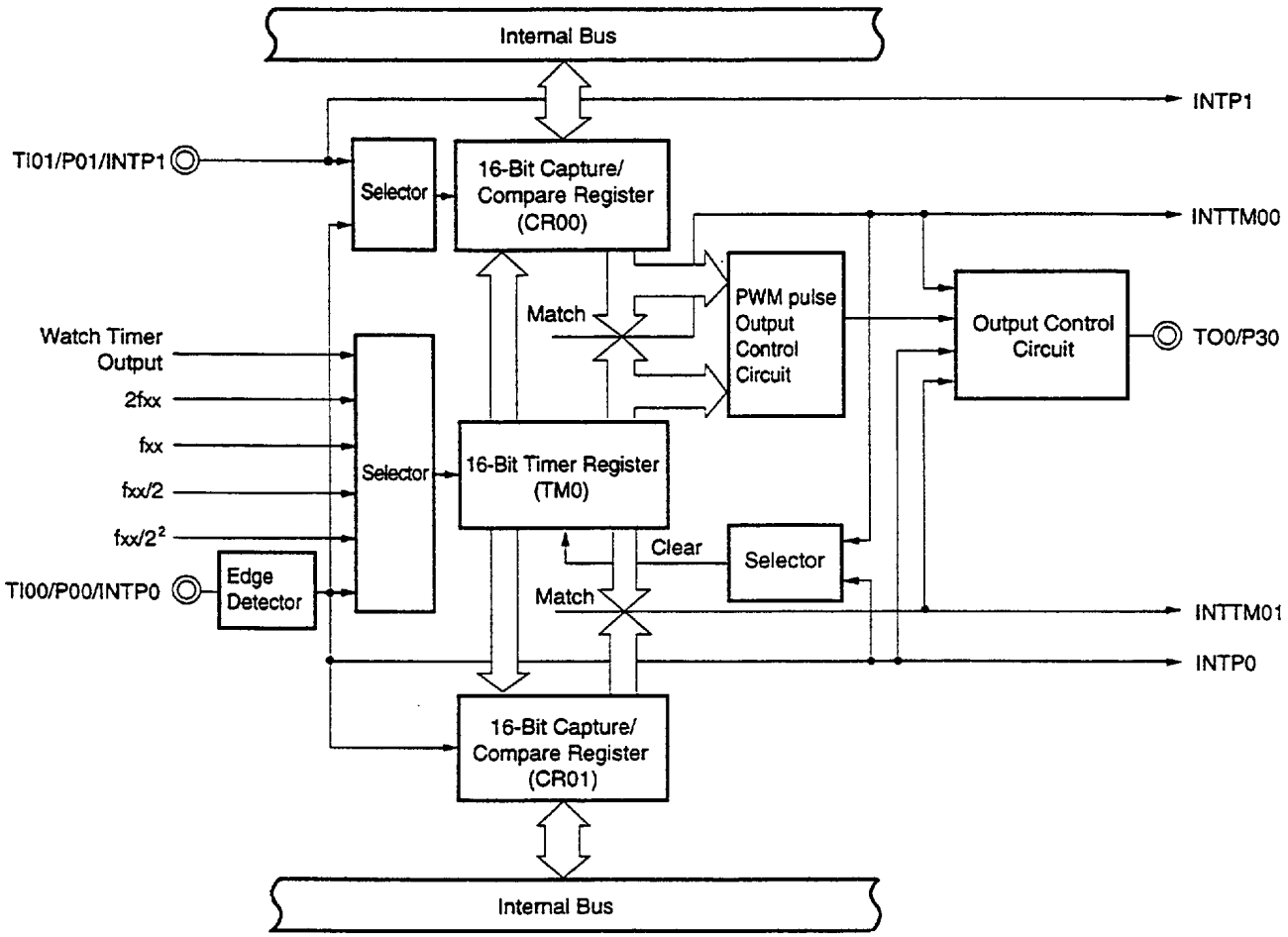


Figure 5-3. 8-Bit Timer/Event Counter Block Diagram

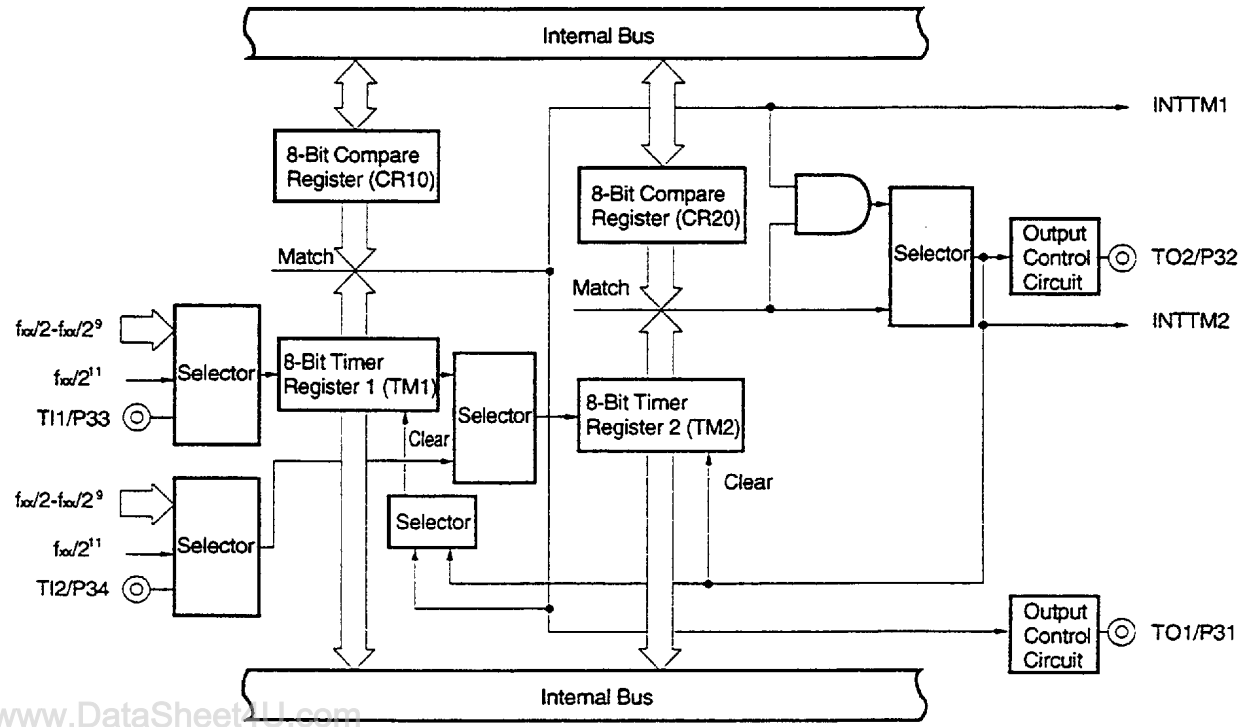


Figure 5-4. Watch Timer Block Diagram

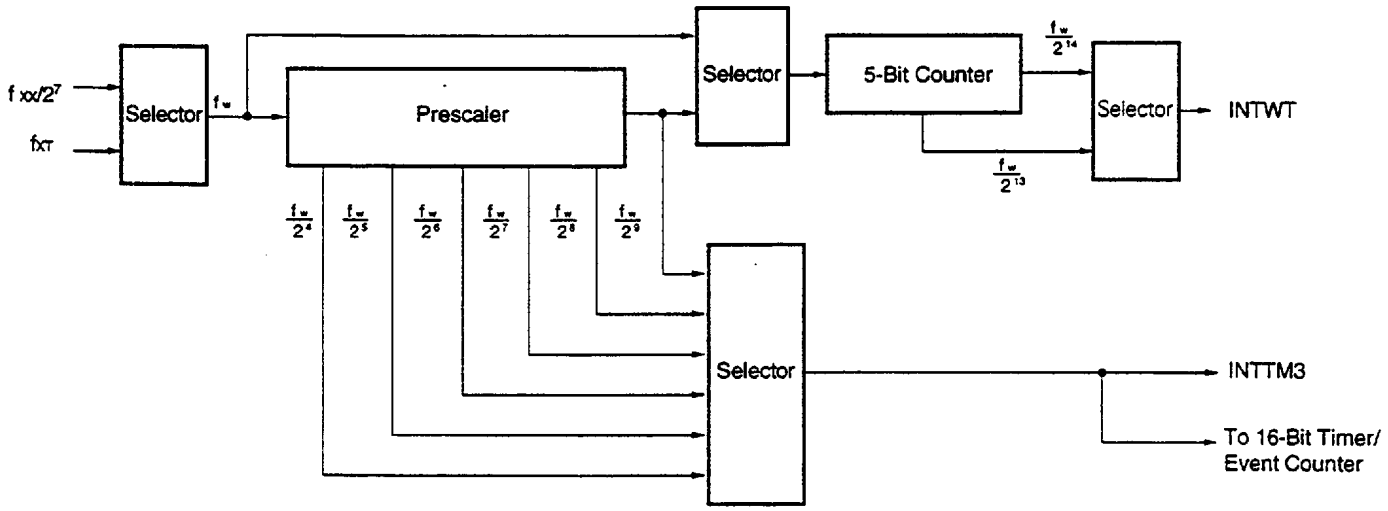
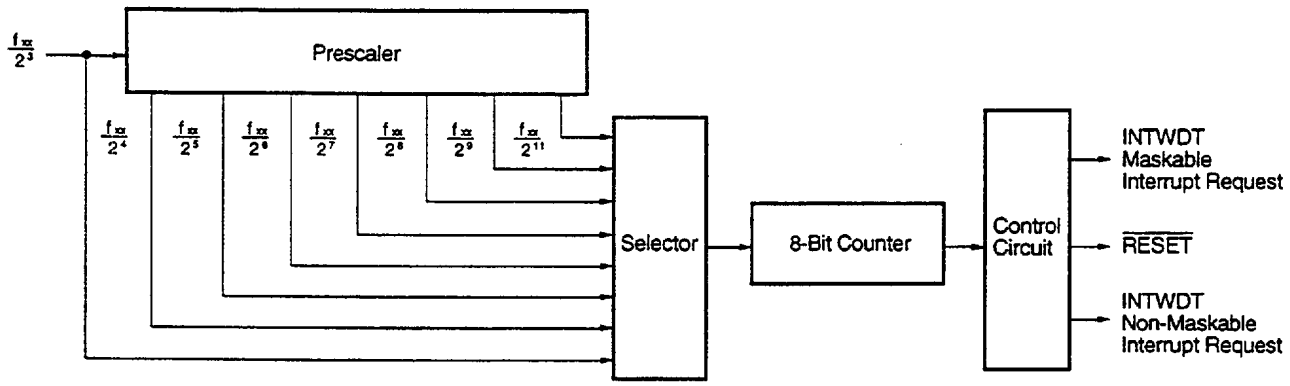


Figure 5-5. Watchdog Timer Block Diagram

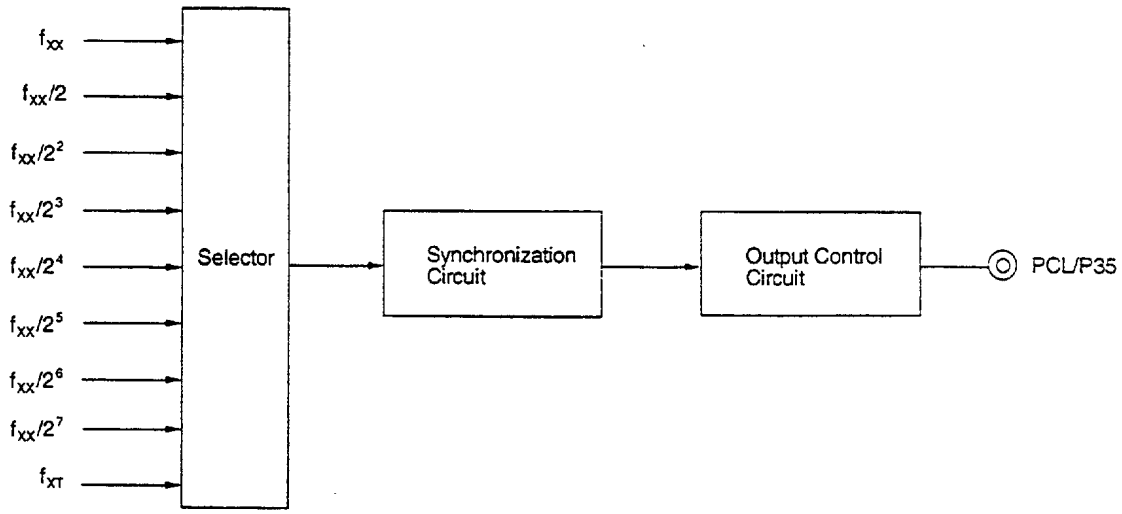


5.4 CLOCK OUTPUT CONTROL CIRCUIT

A clock with the following frequencies can be output as the clock output.

- 19.5 kHz/39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz/2.5 MHz/5.0 MHz (@5.0-MHz operation with main system clock)
- 32.768 kHz (@32.768-kHz operation with subsystem clock)

Figure 5-6. Clock Output Control Circuit Block Diagram

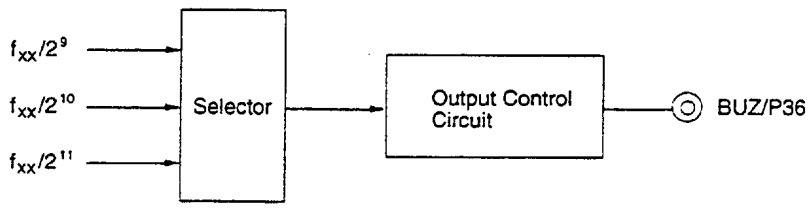


5.5 BUZZER OUTPUT CONTROL CIRCUIT

A clock with the following frequencies can be output as the buzzer output.

- 1.2 kHz/2.4 kHz/4.9 kHz/9.8 kHz (@5.0-MHz operation with main system clock)

Figure 5-7. Buzzer Output Control Circuit Block Diagram



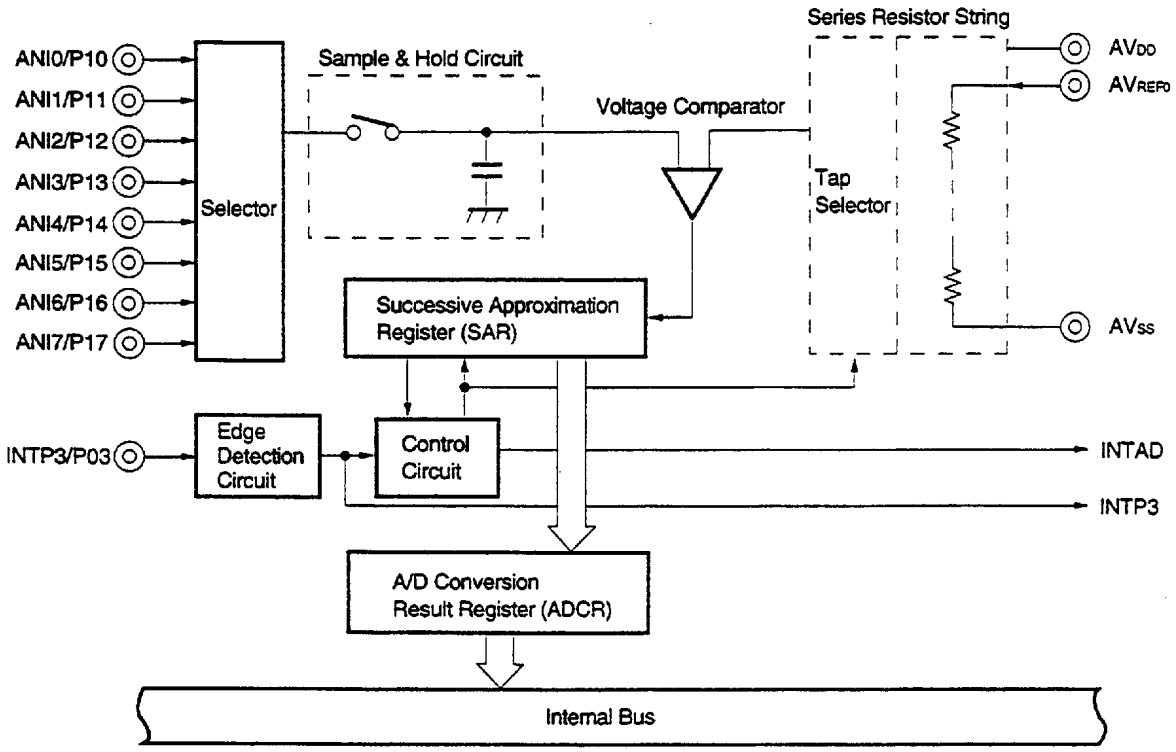
5.6 A/D CONVERTER

An A/D converter of 8-bit resolution x 8 channels is incorporated.

The following two A/D conversion operation start-up methods are available.

- Hardware start
- Software start

Figure 5-8. A/D Converter Block Diagram

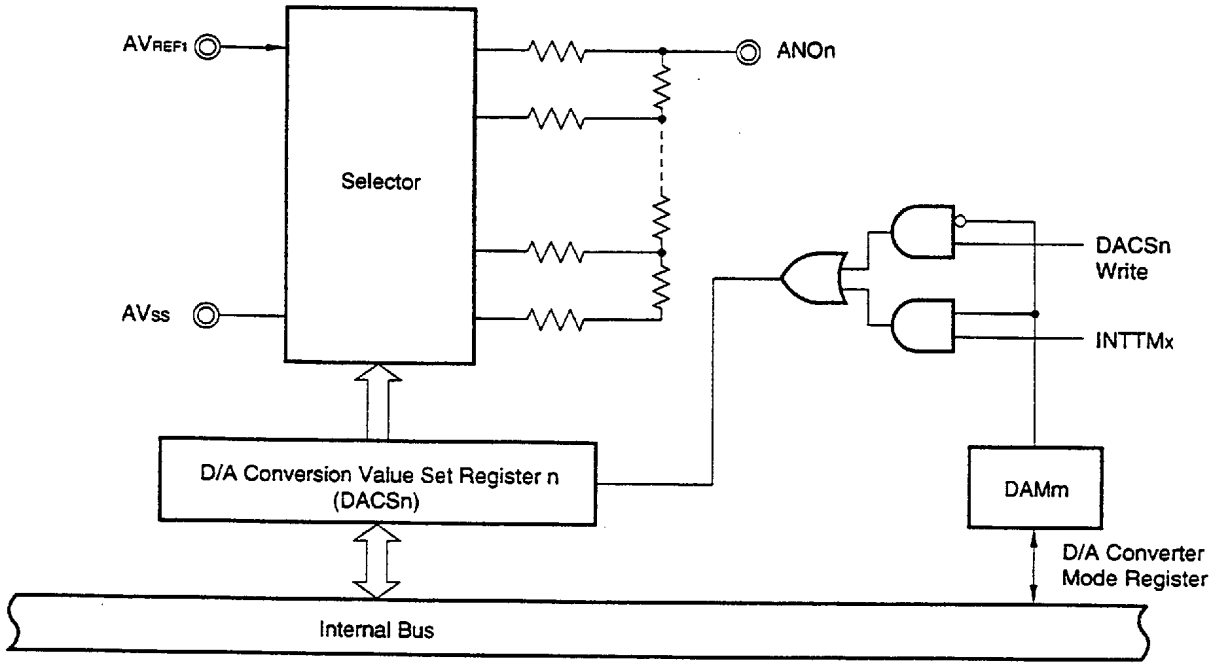


5.7 D/A CONVERTER

A D/A converter of 8-bit resolution x 2 channels is available.

Conversion method is R-2R resistor ladder method.

Figure 5-9. D/A Converter Block Diagram



n = 0, 1
m = 4, 5
x = 1, 2

5.8 SERIAL INTERFACES

3 channels of the clocked serial interface are incorporated.

- Serial interface channel 0
- Serial interface channel 1
- Serial interface channel 2

Table 5-3. Types and Functions of Serial Interface

Function	Serial Interface Channel 0	Serial Interface Channel 1	Serial Interface Channel 2
3-wire serial I/O mode	O (MSB/LSB first switchable)	O(MSB/LSB first switchable)	O(MSB/LSB first switchable)
3-wire serial I/O mode with automatic transmit/receive function	—	O(MSB/LSB first switchable)	—
2-wire serial I/O mode	O (MSB first)	—	—
I²C bus mode	O (MSB first)	—	—
Asynchronous serial interface (UART) mode	—	—	O(Dedicated baud rate generator incorporated)

Figure 5-10. Serial Interface Channel 0 Block Diagram

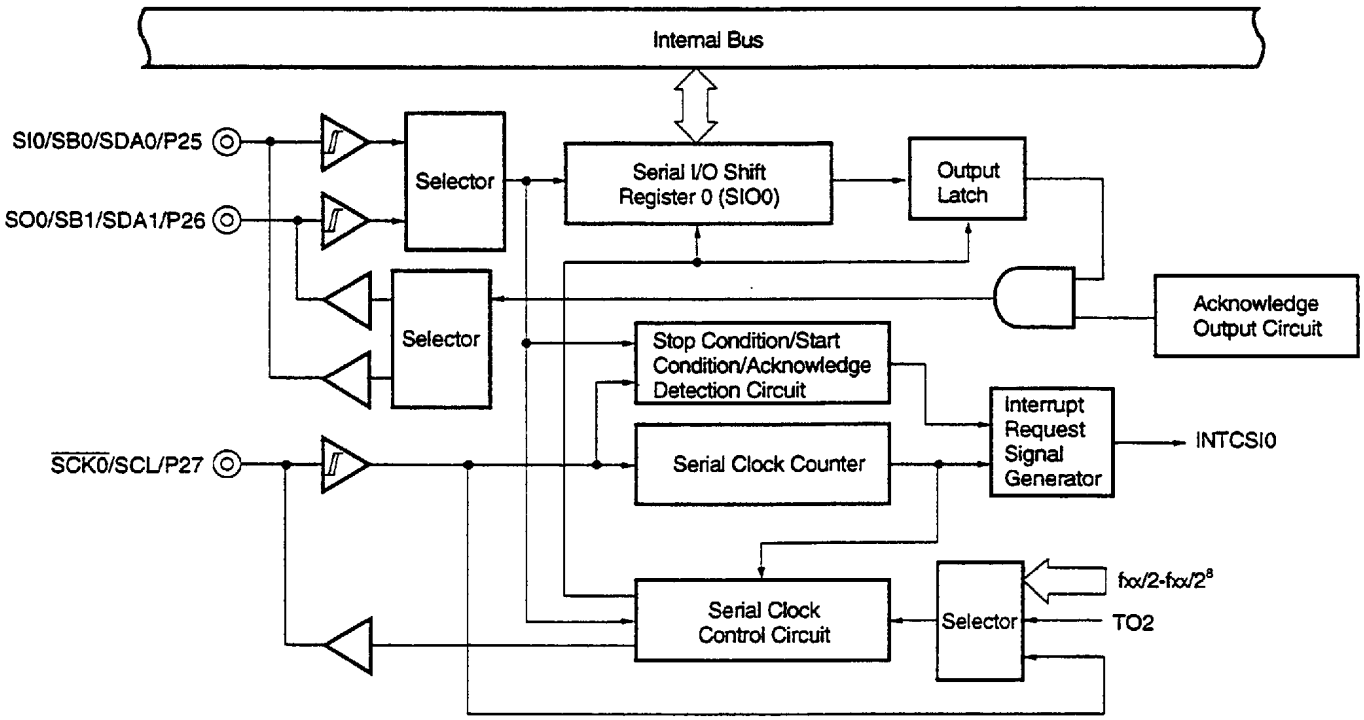


Figure 5-11. Serial Interface Channel 1 Block Diagram

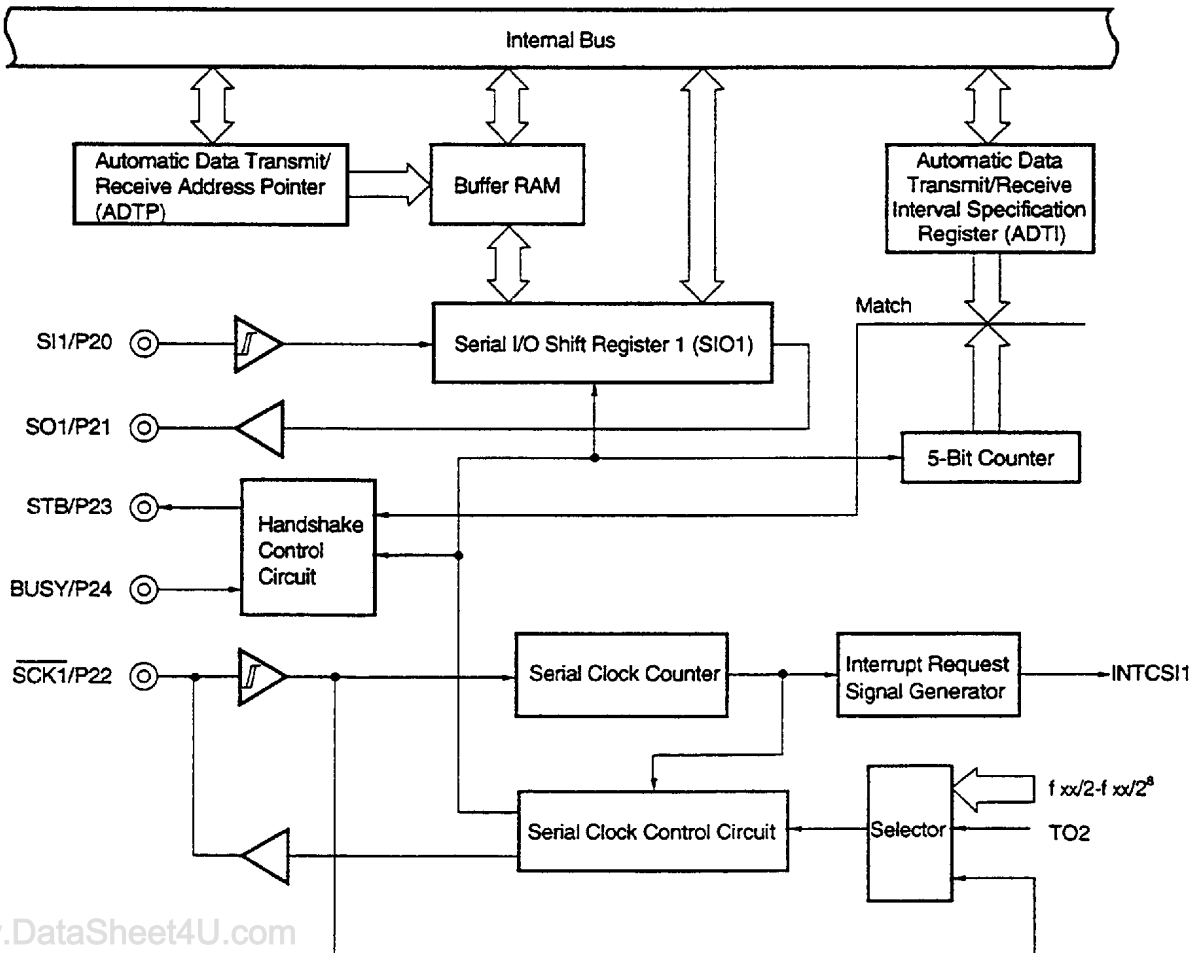
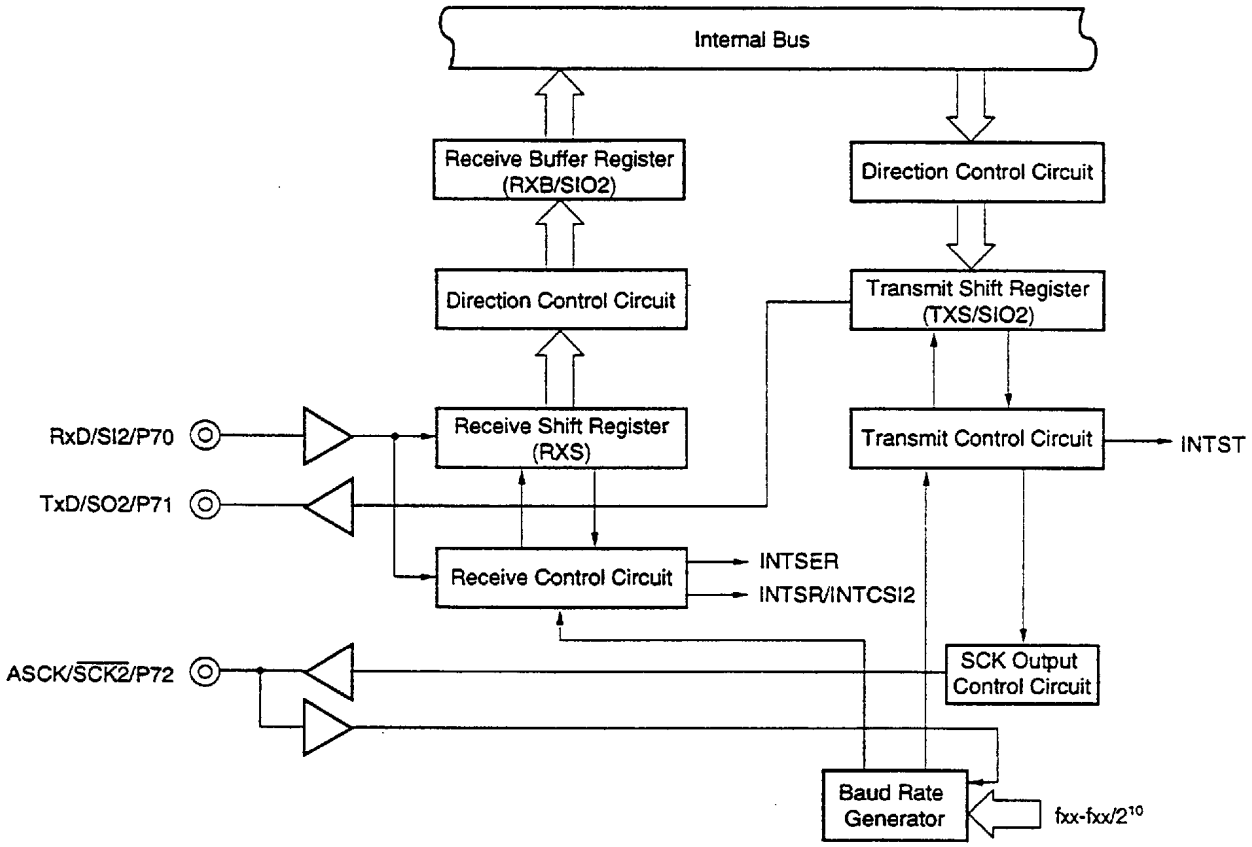


Figure 5-12. Serial Interface Channel 2 Block Diagram

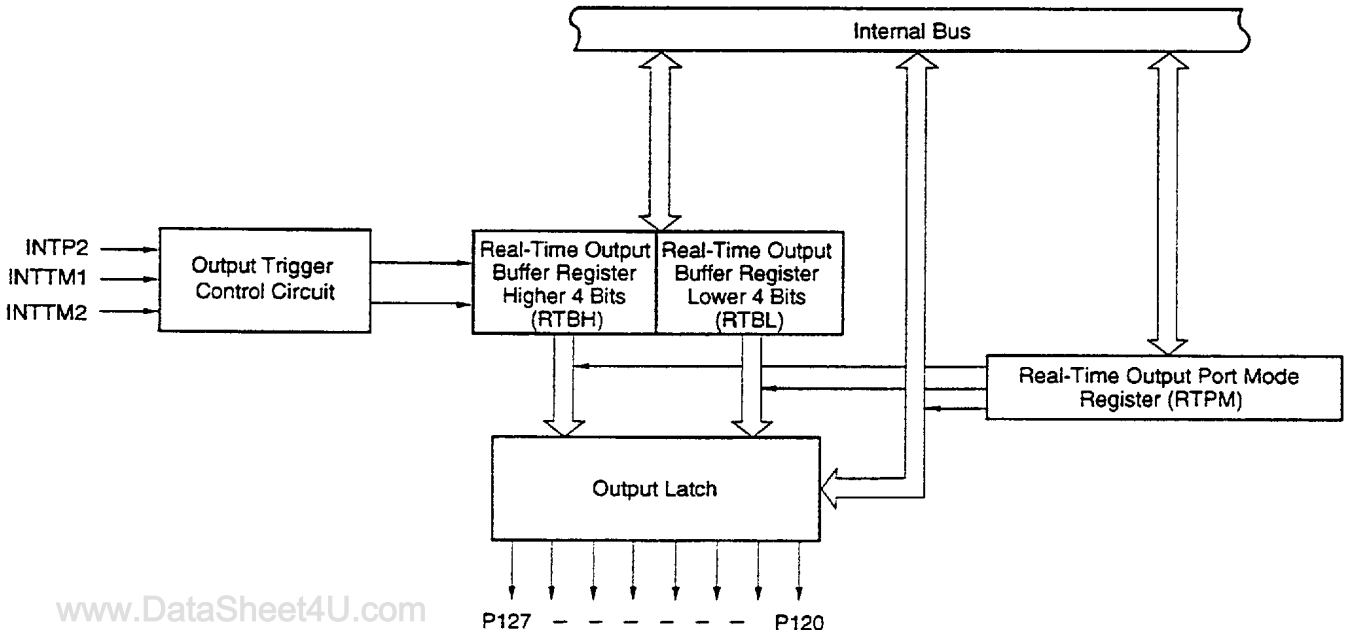


5.9 REAL-TIME OUTPUT PORT FUNCTIONS

Data set previously in the real-time output buffer register is transferred to the output latch by hardware concurrently with timer interrupt or external interrupt generation in order to output to off-chip. This is a real-time output function. Pins used to output data to off-chip are called real-time output ports.

By using a real-time output port, a signal which has no jitter can be output. This is most applicable to control stepping motors, etc.

Figure 5-13. Real-Time Output Port Block Diagram



6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

6.1 INTERRUPT FUNCTIONS

There are 22 interrupt functions of three different types, as shown below.

- Non-maskable interrupt: 1
- Maskable interrupts: 20
- Software interrupt: 1

Table 6-1. Interrupt Source List (1/2)

Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2
		Name	Trigger			
Non-maskable	—	INTWDT	Watchdog timer overflow (watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	(D)
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTP4			000EH	
	6	INTP5			0010H	
	7	INTP6			0012H	
	8	INTCSI0	End of serial interface channel 0 transfer	Internal	0014H	(B)
	9	INTCSI1	End of serial interface channel 1 transfer		0016H	
	10	INTSER	Generation of serial interface channel 2 UART receive error		0018H	
	11	INTSR	End of serial interface channel 2 UART reception		001AH	
		INTCSI2	End of serial interface channel 2 3-wire transfer			
	12	INTST	End of serial interface channel 2 UART transmission		001CH	

Notes 1. The default priority is a priority order when two or more maskable interrupts are generated simultaneously. 0 is the highest order and 18, the lowest.

2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1, respectively.

Table 6-1. Interrupt Source List (2/2)

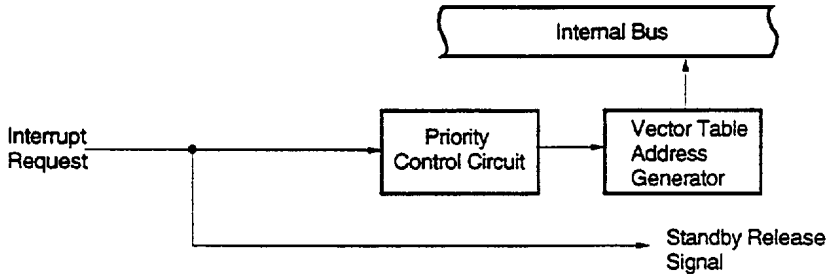
Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2
		Name	Trigger			
Maskable	13	INTTM3	Reference time interval signal from watch timer	Internal	001EH	(B)
	14	INTTM00	Generation of match signal of 16-bit timer register and capture/compare register (CR00)		0020H	
	15	INTTM01	Generation of match signal of 16-bit timer register and capture/compare register (CR01)		0022H	
	16	INTTM1	Generation of match signal of 8-bit timer/event counter 1		0024H	
	17	INTTM2	Generation of match signal of 8-bit timer/ event counter 2		0026H	
	18	INTAD	End of conversion by A/D converter		0028H	
Software	—	BRK	BRK instruction execution	Internal	003EH	(E)

Notes 1. The default priority is a priority order when two or more maskable interrupts are generated simultaneously. 0 is the highest order and 18, the lowest.

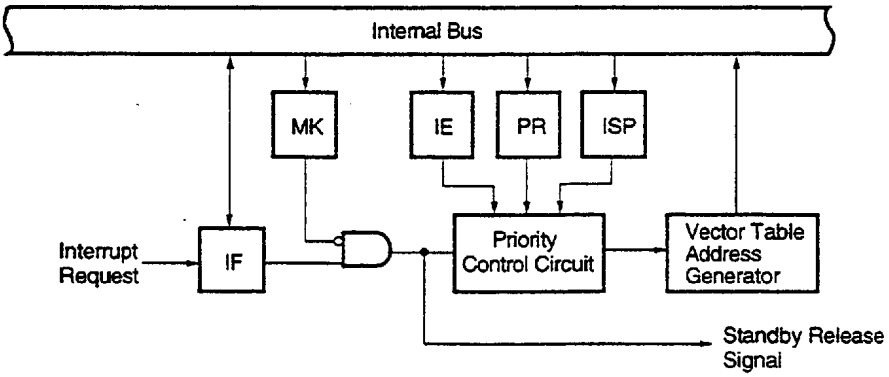
2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1, respectively.

Figure 6-1. Interrupt Function Basic Configuration(1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0)

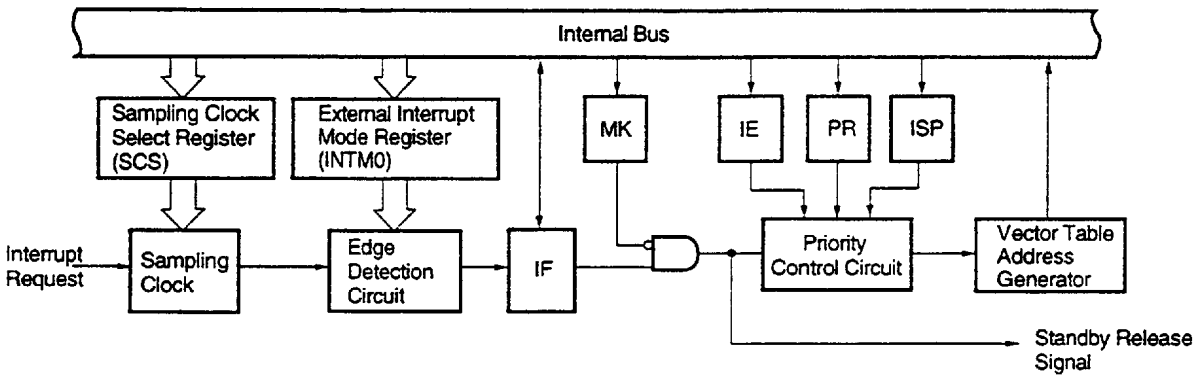
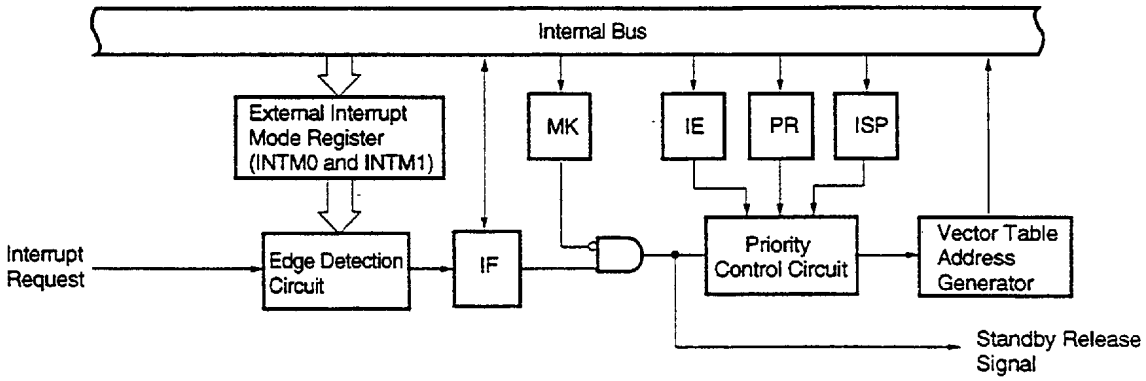
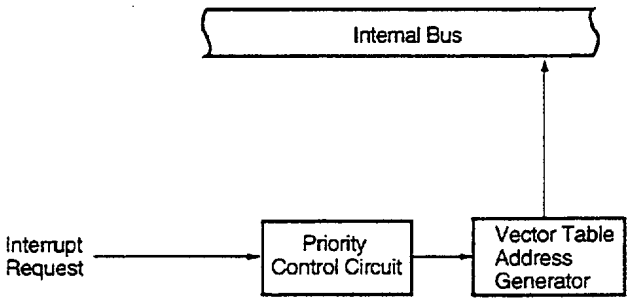


Figure 6-1. Interrupt Function Basic Configuration(2/2)

(D) External maskable interrupt (except INTP0)



(E) Software interrupt



IF : Interrupt request flag
IE : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority specification flag

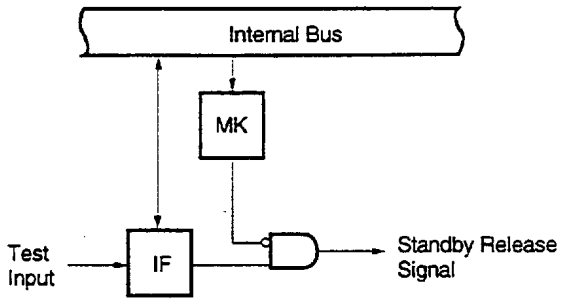
6.2 TEST FUNCTIONS

There are two test functions as shown in Table 6-2.

Table 6-2. Test Input Source List

Test Input Source		Internal/External
Name	Trigger	
INTWT	Watch timer overflow	Internal
INTPT4	Port 4 falling edge detection	External

Figure 6-2. Test Function Basic Configuration



IF : Test input flag
MK : Test mask flag

7. EXTERNAL DEVICE EXPANSION FUNCTIONS

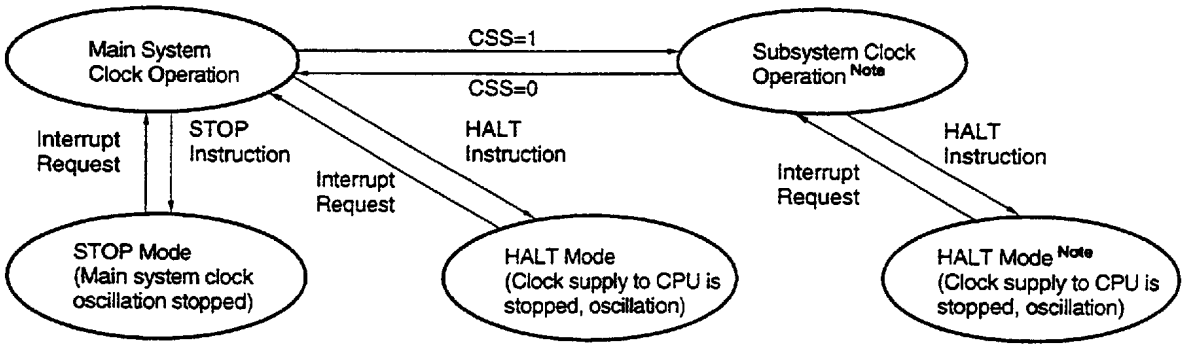
The external device expansion functions connect external devices to areas other than the internal ROM, RAM, and SFR. Ports 4 to 6 are used for external device connection.

8. STANDBY FUNCTION

There are the following two standby functions to reduce the system current consumption.

- HALT mode : The CPU operating clock is stopped.
  The average current consumption can be reduced by intermittent operation in combination with the normal operating mode.
- STOP mode : The main system clock oscillation is stopped. The whole operation by the main system clock is stopped, so that the system operates with ultra-low current consumption using only the subsystem clock.

Figure 8-1. Standby Function



Note The current consumption can be reduced by stopping the main system clock.
When the CPU is operating on the subsystem clock, set bit 7 (MCC) of processor clock control register (PCC) to stop the main system clock. The STOP instruction cannot be used.

Caution **When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.**

9. RESET FUNCTION

There are the following two reset methods.

- External reset input by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog time runaway time detection

10. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

Second Operand / First Operand	#byte	A	r Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + Byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]													
[HL]		MOV											ROR4 ROL4
[HL + Byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOV, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

First Operand \ Second Operand	#word	AX	rp [Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW [Note]						INCW DECW PUSH POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, or HL

(3) Bit manipulate instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

First Operand \ Second Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	Saddr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instruction/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

Second Operand / First Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR BC BNC BZ BNZ
Compound instruction					BT BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

11. ELECTRICAL SPECIFICATIONS ★

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

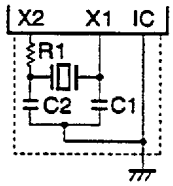
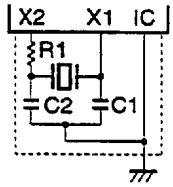
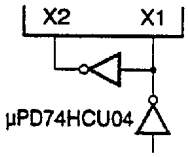
Parameter	Symbol	Test Conditions		Ratings	Unit
Supply voltage	V_{DD}			−0.3 to +7.0	V
	AV_{DD}			−0.3 to V_{DD} + 0.3	V
	AV_{REF0}			−0.3 to V_{DD} + 0.3	V
	AV_{REF1}			−0.3 to V_{DD} + 0.3	V
	AV_{SS}			−0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131, X1, X2, XT2, $\overline{RESET}$		−0.3 to V_{DD} + 0.3	V
	V_{I2}	P60 to P63	N-ch Open-drain	−0.3 to +16	V
Output voltage	V_O			−0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pin	AV_{SS} − 0.3 to AV_{REF0} + 0.3	V
Output current high	I_{OH}	1 pin		−10	mA
		P01 to P06, P30-P37, P56, P57, P60 to P67, P120 to P127 total		−15	mA
		P10 to P17, P20 to P27, P40 to P47, P50 to P55, P70 to P72, P130, P131 total		−15	mA
Output current low	I_{OL} Note	1 pin	Peak value	30	mA
			r.m.s.	15	mA
		P50 to P55 total	Peak value	100	mA
			r.m.s.	70	mA
		P56, P57, P60 to P63 total	Peak value	100	mA
			r.m.s.	70	mA
		P10 to P17, P20 to P27, P40 to P47, P70 to P72, P130, P131 total	Peak value	50	mA
			r.m.s.	20	mA
		P01 to P06, P30 to P37, P64 to P67, P120 to P127 total	Peak value	50	mA
			r.m.s.	20	mA
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

Note The r.m.s. should be calculated as follows: [r.m.s.] = [Peak value] x $\sqrt{duty}$

Caution **If any of the parameters exceed the absolute maximum ratings, even momentarily, device reliability may be impaired. The absolute maximum ratings are values that may physically damage the product. Be sure to use the product within the ratings.**

Remark The characteristics of dual-function pins and port pins are the same unless otherwise specified.

MAIN SYSTEM CLOCK OSCILLATION CIRCUIT CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X) Note1	V_{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time Note2	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X) Note1		1.0		5.0	MHz
		Oscillation stabilization time Note2	V_{DD} = 4.5 to 6.0 V			10	ms
						30	
External clock		X1 input frequency (f_X) Note1		1.0		5.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		85		500	ns

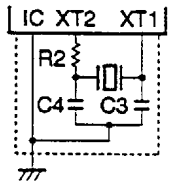
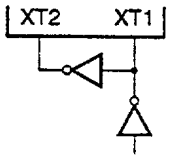
Notes 1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristics" for instruction execution time.
2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. **When using the main system clock oscillator, wiring in the area enclosed with the broken line should be carried out as follows to avoid adverse effects from wiring capacitance.**

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. **When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.**

SUBSYSTEM CLOCK OSCILLATION CIRCUIT CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT}) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 6.0 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT}) Note 1		32		100	kHz
		XT1 input high/low level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristics" for instruction execution time.

2. Time required to stabilize oscillation after applying power (V_{DD}).

Cautions 1. **When using the subsystem clock oscillator, wiring in the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.**

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as Vss.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. **The subsystem clock oscillation circuit is a circuit with a low amplification level, more prone to misoperation due to noise than the main system clock. When using the subsystem clock, pay special attention to wiring as described above.**

RECOMMENDED OSCILLATOR CONSTANT

(1) μPD78052Y, 78053Y, 78054Y, 78055Y, 78056Y

MAIN SYSTEM CLOCK: CERAMIC RESONATOR (T_A = −40 to +85 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillator Constant			Oscillation Voltage Range		Remarks
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)	
Murata Mfg. Co., Ltd.	CSA5.00MG	5.00	30	30	0	2.0	6.0	
	CST5.00MGW	5.00	On-chip	On-chip	0	2.0	6.0	Capacitor on chip
Kyocera	KBR-5.0MSA	5.00	33	33	0	2.0	6.0	Lead type
	KBR-5.0MKS	5.00	On-chip	On-chip	0	2.0	6.0	Capacitor on chip, lead type
	KBR-5.0MWS	5.00	On-chip	On-chip	0	2.0	6.0	Capacitor on chip, lead type
	PBRC 5.00A	5.00	33	33	0	2.0	6.0	Chip type
TDK Corp.	CCR4.0MC3	4.00	On-chip	On-chip	0	2.0	6.0	Capacitor on chip
	CCR5.0MC3	5.00	On-chip	On-chip	0	2.0	6.0	Capacitor on chip

MAIN SYSTEM CLOCK: CRYSTAL RESONATOR (T_A = −10 to +70 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillator Constant			Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)
Daishinku	SMD-49	3.579545	27	27	1.5	2.0	6.0

SUBSYSTEM CLOCK: CRYSTAL RESONATOR (T_A = −10 to +70 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillator Constant			Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)
Daishinku	DT-38 (1TA252E00)	32.768	27	20	330	2.0	6.0

Caution **The oscillator constant and oscillation voltage range indicated above are conditions for stable oscillation and do not guarantee oscillating frequency accuracy. If frequency accuracy is necessary for the user's circuit, the frequency of the resonator in the circuit must be adjusted. Therefore, it is recommended that the user directly consult the resonator manufacturer before designing.**

(2) μPD78058Y

MAIN SYSTEM CLOCK: CERAMIC RESONATOR (T_A = −40 to +85 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillator Constant			Oscillation Voltage Range		Remarks
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)	
Kyocera	PBRC4.19A	4.19	33	33	0	2.0	6.0	
	PBRC4.19B	4.19	On-chip	On-chip	0	2.0	6.0	Capacitor on chip
	KBR-4.19MSA	4.19	33	33	0	2.0	6.0	
	KBR-4.19MKS	4.19	On-chip	On-chip	0	2.0	6.0	Capacitor on chip
	PBRC4.91A	4.91	33	33	0	2.0	6.0	
	PBRC4.91B	4.91	On-chip	On-chip	0	2.0	6.0	Capacitor on chip
	KBR-4.91MSA	4.91	33	33	0	2.0	6.0	
	KBR-4.91MKS	4.91	On-chip	On-chip	0	2.0	6.0	Capacitor on chip

Caution **The oscillator constant and oscillation voltage range indicated above are conditions for stable oscillation and do not guarantee oscillating frequency accuracy. If frequency accuracy is necessary for the user's circuit, the frequency of the resonator in the circuit must be adjusted. Therefore, it is recommended that the user directly consult the resonator manufacturer before designing.**

CAPACITANCE (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
Input/Output capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V.	P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131			15	pF
			P60 to P63			20	pF

Remark The characteristics of the dual-function pins and port pins are the same unless otherwise specified.

DC CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131	V_{DD} = 2.7 to 6.0 V	0.7V_{DD}		V_{DD}	V
				0.8V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{RESET}$	V_{DD} = 2.7 to 6.0 V	0.8V_{DD}		V_{DD}	V
				0.85V_{DD}		V_{DD}	V
	V_{IH3}	P60 to P63 (N-ch Open-drain)	V_{DD} = 2.7 to 6.0 V	0.7V_{DD}		15	V
				0.8V_{DD}		15	V
	V_{IH4}	X1, X2	V_{DD} = 2.7 to 6.0 V	V_{DD}−0.5		V_{DD}	V
				V_{DD}−0.2		V_{DD}	V
	V_{IH5}	XT1/P07, XT2	4.5 V≤ V_{DD} ≤ 6.0 V	0.8V_{DD}		V_{DD}	V
			2.7 V≤ V_{DD} < 4.5 V	0.9V_{DD}		V_{DD}	V
			2.0 V≤ V_{DD} < 2.7 V[Note]	0.9V_{DD}		V_{DD}	V
Input voltage low	V_{IL1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131	V_{DD} = 2.7 to 6.0 V	0		0.3V_{DD}	V
				0		0.2V_{DD}	V
	V_{IL2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{RESET}$	V_{DD} = 2.7 to 6.0 V	0		0.2V_{DD}	V
				0		0.15V_{DD}	V
	V_{IL3}	P60 to P63	4.5 V≤ V_{DD} ≤ 6.0 V	0		0.3V_{DD}	V
			2.7 V≤ V_{DD} < 4.5 V	0		0.2V_{DD}	V
				0		0.1V_{DD}	V
	V_{IL4}	X1, X2	V_{DD} = 2.7 to 6.0 V	0		0.4	V
				0		0.2	V
	V_{IL5}	XT1/P07, XT2	4.5 V≤ V_{DD} ≤ 6.0 V	0		0.2V_{DD}	V
			2.7 V≤ V_{DD} < 4.5 V	0		0.1V_{DD}	V
			2.0 V≤ V_{DD} < 2.7 V[Note]	0		0.1V_{DD}	V
Output voltage high	V_{OH}	V_{DD} = 4.5 to 6.0 V, I_{OH} = −1 mA		V_{DD}−1.0			V
		I_{OH} = −100 μA		V_{DD}−0.5			V
Output voltage low	V_{OL1}	P50 to P57, P60 to P63	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA		0.4	2.0	V
		P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P70 to P72, P120 to P127, P130, P131	V_{DD} = 4.5 to 6.0 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{SCK0}$	V_{DD} = 4.5 to 6.0 V, open-drain pulled-up (R = 1 KΩ)			0.2V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V

Note For use as P07, use an inverter to input the reverse phase of P07 to the XT2 pin.

Remark The characteristics of dual-function pins and port pins are the same unless otherwise specified.

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P72, P120 to P127, P130, P131, $\overline{RESET}$			3	μA
	I_{LIH2}		X1, X2, XT1/P07, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P60 to P63			80	μA
Input leakage current low	I_{LIL1}	V_{IN} = 0 V	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131, $\overline{RESET}$			–3	μA
	I_{LIL2}		X1, X2, XT1/P07, XT2			–20	μA
	I_{LIL3}		P60 to P63			–3 Note1	μA
Output leakage current high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Mask option pull-up resistor	R_1	V_{IN} = 0 V, P60 to P63		20	40	90	kΩ
Software pull-up resistor Note2	R_2	V_{IN} = 0 V, P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131	4.5 V ≤ V_{DD} ≤ 6.0 V	15	40	90	kΩ
			2.7 V ≤ V_{DD} < 4.5 V	20		500	kΩ

Notes 1. If no pull-up resistor is connected in P60 to P63 (specified with mask option), a –200 μA (MAX.) low-level input leak current flows only during the 1.5-clock interval (no wait interval) during which a read instruction is executed for port 6 (P6) and port mode register (PM6).
The leak current is –3 μA (MAX.) at all times other than the 1.5-clock interval during which the read instruction is executed.

2. A software pull-up resistor can be used only in the range of V_{DD} = 2.7 to 6.0 V.

Remark The characteristics of dual-function pins and port pins are the same unless otherwise specified.

DC CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Power supply current Note1	I_{DD1}	5.0-MHz Crystal oscillation operating mode (f_{XX} = 2.5 MHz) Note2	V_{DD} = 5.0 V ± 10 % Note5		4	12	mA
			V_{DD} = 3.0 V ± 10 % Note6		0.6	1.8	mA
			V_{DD} = 2.2 V ± 10 % Note6		0.35	1.05	mA
		5.0-MHz Crystal oscillation operating mode (f_{XX} = 5.0 MHz) Note3	V_{DD} = 5.0 V ± 10 % Note5		6.5	19.5	mA
			V_{DD} = 3.0 V ± 10 % Note6		0.8	2.4	mA
	I_{DD2}	5.0-MHz Crystal oscillation HALT mode (f_{XX} = 2.5 MHz) Note2	V_{DD} = 5.0 V ± 10 %		1.4	4.2	mA
			V_{DD} = 3.0 V ± 10 %		0.5	1.5	mA
			V_{DD} = 2.2 V ± 10 %		280	840	μA
		5.0-MHz Crystal oscillation HALT mode (f_{XX} = 5.0 MHz) Note3	V_{DD} = 5.0 V ± 10 %		1.6	4.8	mA
			V_{DD} = 3.0 V ± 10 %		0.65	1.95	mA
	I_{DD3}	32.768-kHz Crystal oscillation operating mode Note4	V_{DD} = 5.0 V ± 10 %		60	120	μA
			V_{DD} = 3.0 V ± 10 %		32	64	μA
			V_{DD} = 2.2 V ± 10 %		24	48	μA
	I_{DD4}	32.768-kHz Crystal oscillation HALT mode Note4	V_{DD} = 5.0 V ± 10 %		25	55	μA
			V_{DD} = 3.0 V ± 10 %		5	15	μA
			V_{DD} = 2.2 V ± 10 %		2.5	12.5	μA
	I_{DD5}	XT1 = V_{DD} STOP mode When feedback resistor is used	V_{DD} = 5.0 V ± 10 %		1	30	μA
			V_{DD} = 3.0 V ± 10 %		0.5	10	μA
			V_{DD} = 2.2 V ± 10 %		0.3	10	μA
	I_{DD6}	XT1 = V_{DD} STOP mode When feedback resistor is unused	V_{DD} = 5.0 V ± 10 %		0.1	30	μA
			V_{DD} = 3.0 V ± 10 %		0.05	10	μA
			V_{DD} = 2.2 V ± 10 %		0.05	10	μA

Notes 1. The AV_{REF0}, AV_{REF1}, AV_{DD} current, and port current (including the current flowing in the on-chip pull-up resistor) are not included.

2. Operation with f_{XX} = f_X/2 (when oscillation mode selection register (OSMS) is set to 00H)

3. Operation with f_{XX} = f_X (when OSMS is set to 01H)

4. When the main system clock is halted.

5. Operating in high-speed mode (when the processor clock control register (PCC) is set to 00H.)

6. Operating in low-speed mode (when PCC is set to 04H)

f_{XX} : Main system clock frequency (f_X or f_X/2)

f_X : Main system clock oscillation frequency

AC CHARACTERISTICS

(1) BASIC OPERATION (T_A = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions			MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating on main system clock	$f_{XX} = f_X/2$ Note1	V_{DD} = 2.7 to 6.0 V	0.8		64	μs
					2.2		64	μs
			$f_{XX} = f_X$ Note2	4.5 V≤ V_{DD} ≤ 6.0 V	0.4		32	μs
				2.7 V≤ V_{DD} < 4.5 V	0.8		32	μs
		Operating on sub system clock			40	122	125	μs
TI00 input high-/low-level width	t_{TIH00}, t_{TIL00}	3.5 V ≤ V_{DD} ≤ 6.0 V			$2/f_{sam}+0.1$ Note3			μs
		2.7 V ≤ V_{DD} < 3.5 V			$2/f_{sam}+0.2$ Note3			μs
					$2/f_{sam}+0.5$ Note3			μs
TI01 input high-/low-level width	t_{TIH01}, t_{TIL01}	V_{DD} = 2.7 to 6.0 V			10			μs
					20			μs
TI1, TI2 input frequency	f_{TI1}	V_{DD} = 4.5 to 6.0 V			0		4	MHz
					0		275	kHz
TI1, TI2 input high-/low-level width	t_{TIH1}, t_{TIL1}	V_{DD} = 4.5 to 6.0 V			100			ns
					1.8			μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0		3.5 V ≤ V_{DD} ≤ 6.0 V	$2/f_{sam}+0.1$ Note3			μs
				2.7 V ≤ V_{DD} < 3.5 V	$2/f_{sam}+0.2$ Note3			μs
					$2/f_{sam}+0.5$ Note3			μs
		INTP1 to INTP6, KR0 to KR7		V_{DD} = 2.7 to 6.0 V	10			μs
					20			μs
$\overline{RESET}$ low level width	t_{RSL}	V_{DD} = 2.7 to 6.0 V			10			μs
					20			μs

Notes 1. When oscillation mode selection register (OSMS) is set to 00H

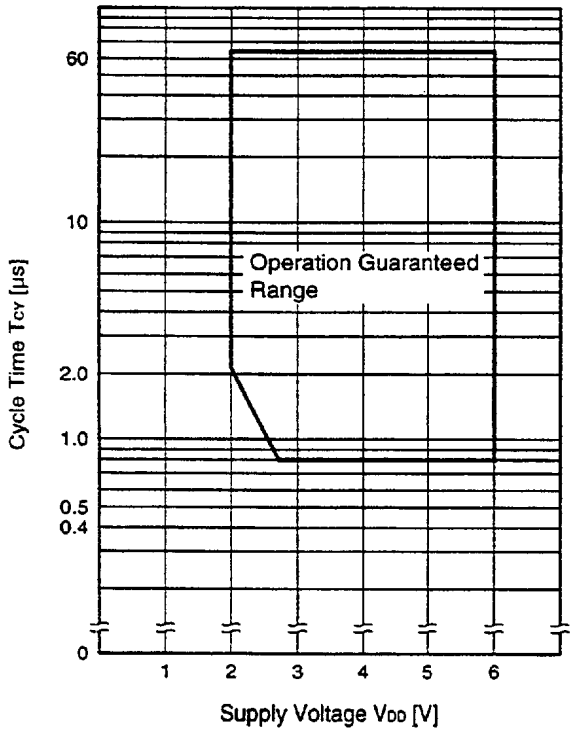
2. When OSMS is set to 01H

3. In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock selection register, f_{sam} is selectable between $f_{XX}/2^N$, $f_{XX}/32$, $f_{XX}/64$, and $f_{XX}/128$ (when N= 0 to 4).

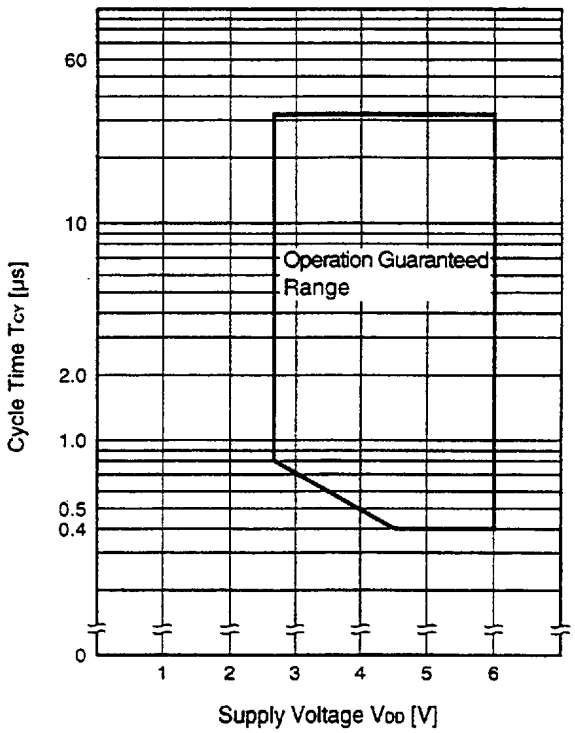
f_{XX} : Main system clock frequency (f_X or $f_X/2$)

f_X : Main system clock oscillation frequency

T_{CY} vs V_{DD} (At $f_{XX} = f_X/2$ main system clock operation)



T_{CY} vs V_{DD} (At $f_{XX} = f_X$ main system clock operation)



(2) READ/WRITE OPERATION

(a) When MCS = 1, PCC2 to PCC0 = 000B (T_A = −40 to +85 °C, V_{DD} = 4.5 to 6.0 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		0.85t_{CY} − 50		ns
Address setup time	t_{ADS}		0.85t_{CY} − 50		ns
Address hold time	t_{ADH}		50		ns
Data input time from address	t_{ADD1}			(2.85 + 2n)t_{CY} − 80	ns
	t_{ADD2}			(4 + 2n)t_{CY} − 100	ns
Data input time from $\overline{RD}$↓	t_{RDD1}			(2 + 2n)t_{CY} − 100	ns
	t_{RDD2}			(2.85 + 2n)t_{CY} − 100	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(2 + 2n)t_{CY} − 60		ns
	t_{RDL2}		(2.85 + 2n)t_{CY} − 60		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{RDWT1}			0.85t_{CY} − 50	ns
	t_{RDWT2}			2t_{CY} − 60	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{WRWT}			2t_{CY} − 60	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(1.15 + 2n)t_{CY}	(2 + 2n)t_{CY}	ns
Write data setup time	t_{WDS}		(2.85 + 2n)t_{CY} − 100		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL}		(2.85 + 2n)t_{CY} − 60		ns
$\overline{RD}$↓ delay time from ASTB↓	t_{ASTRD}		25		ns
$\overline{WR}$↓ delay time from ASTB↓	t_{ASTWR}		0.85t_{CY} + 20		ns
ASTB↑ delay time from $\overline{RD}$↑ in external fetch	t_{RDAST}		0.85t_{CY} − 10	1.15t_{CY} + 20	ns
Address hold time from $\overline{RD}$↑ in external fetch	t_{RDADH}		0.85t_{CY} − 50	1.15t_{CY} + 50	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}		40		ns
Write data output time from $\overline{WR}$↓	t_{RDWD}		0	50	ns
Address hold time from $\overline{WR}$↑	t_{WRADH}		0.85t_{CY}	1.15t_{CY} + 40	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t_{WTRD}		1.15t_{CY} + 40	3.15t_{CY} + 40	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t_{WTWR}		1.15t_{CY} + 30	3.15t_{CY} + 30	ns

Remarks
1. MCS: Oscillation mode selection register (OSMS) bit 0
2. PCC2 to PCC0: Processor clock control register (PCC) bit 2 to bit 0
3. $t_{CY} = T_{CY}/4$
4. n indicates number of waits.

(b) Except when MCS = 1, PCC2 to PCC0 = 000B (T_A = −40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

(1/2)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}	V_{DD} = 2.7 to 6.0 V	t_{CY} − 80		ns
			t_{CY} − 150		ns
Address setup time	t_{ADS}	V_{DD} = 2.7 to 6.0 V	t_{CY} − 80		ns
			t_{CY} − 150		ns
Address hold time	t_{ADH}	V_{DD} = 2.7 to 6.0 V	0.4t_{CY} − 10		ns
			0.37t_{CY} − 40		ns
Data input time from address	t_{ADD1}	V_{DD} = 2.7 to 6.0 V		(3 + 2n)t_{CY} − 160	ns
				(3 + 2n)t_{CY} − 320	ns
	t_{ADD2}	V_{DD} = 2.7 to 6.0 V		(4 + 2n)t_{CY} − 200	ns
				(4 + 2n)t_{CY} − 300	ns
Data input time from $\overline{RD}$↓	t_{RDD1}	V_{DD} = 2.7 to 6.0 V		(1.4 + 2n)t_{CY} − 70	ns
				(1.37 + 2n)t_{CY} − 120	ns
	t_{RDD2}	V_{DD} = 2.7 to 6.0 V		(2.4 + 2n)t_{CY} − 70	ns
				(2.37 + 2n)t_{CY} − 120	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}	V_{DD} = 2.7 to 6.0 V	(1.4 + 2n)t_{CY} − 20		ns
			(1.37 + 2n)t_{CY} − 20		ns
	t_{RDL2}	V_{DD} = 2.7 to 6.0 V	(2.4 + 2n)t_{CY} − 20		ns
			(2.37 + 2n)t_{CY} − 20		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{RDWT1}	V_{DD} = 2.7 to 6.0 V		t_{CY} − 100	ns
				t_{CY} − 200	ns
	t_{RDWT2}	V_{DD} = 2.7 to 6.0 V		2t_{CY} − 100	ns
				2t_{CY} − 200	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{WRWT}	V_{DD} = 2.7 to 6.0 V		2t_{CY} − 100	ns
				2t_{CY} − 200	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(1 + 2n)t_{CY}	(2 + 2n)t_{CY}	ns
Write data setup time	t_{WDS}	V_{DD} = 2.7 to 6.0 V	(2.4 + 2n)t_{CY} − 60		ns
			(2.37 + 2n)t_{CY} − 100		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL}	V_{DD} = 2.7 to 6.0 V	(2.4 + 2n)t_{CY} − 20		ns
			(2.37 + 2n)t_{CY} − 20		ns
$\overline{RD}$↓ delay time from ASTB↓	t_{ASTRD}	V_{DD} = 2.7 to 6.0 V	0.4t_{CY} − 30		ns
			0.37t_{CY} − 50		ns
$\overline{WR}$↓ delay time from ASTB↓	t_{ASTWR}	V_{DD} = 2.7 to 6.0 V	1.4t_{CY} − 30		ns
			1.37t_{CY} − 50		ns

Remarks
1. MCS: Oscillation mode selection register (OSMS) bit 0
2. PCC2 to PCC0: Processor clock control register (PCC) bit 2 to bit 0
3. $t_{CY} = T_{CY}/4$
4. n indicates the number of waits.

(b) Except when MCS = 1, PCC2 to PCC0 = 000B (T_A = −40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB↑ delay time from $\overline{RD}$↑ in external fetch	t_{RDAST}		t_{CY} − 10	t_{CY} + 20	ns
Address hold time from $\overline{RD}$↑ in external fetch	t_{RDADH}		t_{CY} − 50	t_{CY} + 50	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}	V_{DD} = 2.7 to 6.0 V	0.4t_{CY} − 20		ns
			0.37t_{CY} − 40		ns
Write data output time from $\overline{WR}$↓	t_{WRWD}	V_{DD} = 2.7 to 6.0 V	0	60	ns
			0	120	ns
Address hold time from $\overline{WR}$↑	t_{WRADH}	V_{DD} = 2.7 to 6.0 V	t_{CY}	t_{CY} + 60	ns
			t_{CY}	t_{CY} + 120	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t_{WTRD}	V_{DD} = 2.7 to 6.0 V	0.6t_{CY} + 180	2.6t_{CY} + 180	ns
			0.63t_{CY} + 350	2.63t_{CY} + 350	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t_{WTWR}	V_{DD} = 2.7 to 6.0 V	0.6t_{CY} + 120	2.6t_{CY} + 120	ns
			0.63t_{CY} + 240	2.63t_{CY} + 240	ns

Remarks
1. MCS: Oscillation mode selection register (OSMS) bit 0
2. PCC2 to PCC0: Processor clock control register (PCC) bit 2 to bit 0
3. $t_{CY} = T_{CY}/4$
4. n indicates number of waits.

(3) SERIAL INTERFACE (T_A = −40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 6.0 V	$t_{KCY1}/2 - 50$			ns
			$t_{KCY1}/2 - 100$			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	C = 100 pF [Note]			300	ns

Note C is the load capacitance of $\overline{SCK0}$, SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH2}, t_{KL2}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}		100			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO2}	C = 100 pF [Note]			300	ns
$\overline{SCK0}$ rise, fall time	t_{R2}, t_{F2}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the load capacitance of SO0 output line.

(iii) 2-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	R = 1 kΩ, C = 100 pF Note	V_{DD} = 2.7 to 6.0 V	1600			ns
				3200			ns
$\overline{SCK0}$ high-level width	t_{KH3}		V_{DD} = 2.7 to 6.0 V	$t_{KCY3}/2 - 160$			ns
				$t_{KCY3}/2 - 190$			ns
$\overline{SCK0}$ low-level width	t_{KL3}		V_{DD} = 4.5 to 6.0 V	$t_{KCY3}/2 - 50$			ns
				$t_{KCY3}/2 - 100$			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK3}		4.5 V ≤ V_{DD} ≤ 6.0 V	300			ns
			2.7 V ≤ V_{DD} < 4.5 V	350			ns
				400			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI3}			600			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO3}			0		300	ns

Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$, SB0, and SB1 output line.

(iv) 2-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	V_{DD} = 2.7 to 6.0 V		1600			ns
				3200			ns
$\overline{SCK0}$ high-level width	t_{KH4}	V_{DD} = 2.7 to 6.0 V		650			ns
				1300			ns
$\overline{SCK0}$ low-level width	t_{KL4}	V_{DD} = 2.7 to 6.0 V		800			ns
				1600			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK4}			100			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI4}			$t_{KCY4}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO4}	R = 1 kΩ, C = 100 pF Note	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		500	ns
$\overline{SCK0}$ rise, fall time	t_{R4}, t_{F4}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$, SB0, and SB1 output line.

(v) I²C Bus mode (SCL...Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY5}	R = 1 kΩ	V_{DD} = 2.7 to 6.0 V	10			μs
		C = 100pF Note		20			μs
SCL high-level width	t_{KH5}		V_{DD} = 2.7 to 6.0 V	t_{KCY5} – 160			ns
				t_{KCY5} – 190			ns
SCL low-level width	t_{KL5}		V_{DD} = 4.5 to 6.0 V	t_{KCY5} – 50			ns
				t_{KCY5} – 100			ns
SDA0, SDA1 setup time (to SCL↑)	t_{SIK5}		V_{DD} = 2.7 to 6.0 V	200			ns
				300			ns
SDA0, SDA1 hold time (to SCL↓)	t_{KSI5}			0			ns
SDA0, SDA1 output delay time from SCL↓	t_{KSO5}		V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		500	ns
SCL↑→SDA0, SDA1↓ or SCL↑→SDA0, SDA1↑	t_{KSB}			200			ns
SDA0, SDA1↓→SCL↓	t_{SBK}			400			ns
SDA0, SDA1 high-level width	t_{SBH}			500			ns

Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$, SB0, and SB1 output line.

(vi) I²C Bus mode (SCL...External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY6}			1000			ns
SCL high-/low-level width	t_{KH6}, t_{KL6}			400			ns
SDA0, SDA1 setup time (to SCL↑)	t_{SIK6}			200			ns
SDA0, SDA1 hold time (to SCL↓)	t_{KSI6}			0			ns
SCL↓→ SDA0, SDA1 output delay time	t_{KSO6}	R = 1 kΩ,	V_{DD} = 4.5 to 6.0 V	0		300	ns
		C = 100 pF Note		0		500	ns
SCL↑→SDA0, SDA1↓ or SCL↑→SDA0, SDA1↑	t_{KSB}			200			ns
SDA0, SDA1↓ → SCL↓	t_{SBK}			400			ns
SDA0, SDA1 high-level width	t_{SBH}			500			ns
SCL rise, fall time	t_{R6}, t_{F6}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note R and C are the load resistance and load capacitance of the SDA0, SDA1 output line.

(b) Serial interface channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY7}	4.5 V ≤ V_{DD} ≤ 6.0 V		800		ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK1}$ high-/low-level width	t_{KH7}, t_{KL7}	V_{DD} = 4.5 to 6.0 V	$t_{KCY7}/2 - 50$			ns
			$t_{KCY7}/2 - 100$			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK7}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI7}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO7}	C = 100 pF [Note]			300	ns

Note C is the load capacitance of the $\overline{SCK1}$ and SO1 output lines.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$... External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY8}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK1}$ high-/low-level width	t_{KH8}, t_{KL8}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK8}		100			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI8}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO8}	C = 100 pF [Note]			300	ns
$\overline{SCK1}$ rise, fall time	t_{R8}, t_{F8}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the load capacitance of the SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$...Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK1}$ high-/low-level width	t_{KH9}, t_{KL9}	V_{DD} = 4.5 to 6.0 V	$t_{KCY9}/2 - 50$			ns
			$t_{KCY9}/2 - 100$			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK9}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI9}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO9}	C = 100 pF [Note]			300	ns
STB↑ from $\overline{SCK1}$↑	t_{SBD}		$t_{KCY9}/2 - 100$		$t_{KCY9}/2 + 100$	ns
Strobe signal high-level width	t_{SBW}	V_{DD} = 2.7 to 6.0V	$t_{KCY9} - 30$		$t_{KCY9} + 30$	ns
			$t_{KCY9} - 60$		$t_{KCY9} + 60$	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			200			ns
$\overline{SCK1}$↓ from busy inactive	t_{SPS}				$2t_{KCY9}$	ns

Note C is the load capacitance of the $\overline{SCK1}$, SO1 output line.

(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$...External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK1}$ high-/low-level width	t_{KH10}, t_{KL10}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK10}		100			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KIS10}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO10}	C = 100 pF [Note]			300	ns
$\overline{SCK1}$ rise, fall time	t_{R10}, t_{F10}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the load capacitance of the SO1 output line.

(c) Serial interface channel 2

(i) 3-wire serial I/O mode ($\overline{SCK2}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY11}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK2}$ high-/low-level width	t_{KH11}, t_{KL11}	V_{DD} = 4.5 to 6.0 V	$t_{KCY11}/2 - 50$			ns
			$t_{KCY11}/2 - 100$			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK11}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI2 hold time (to $\overline{SCK2}$↑)	t_{KSI11}		400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO11}	C = 100 pF Note			300	ns

Note C is the load capacitance of the $\overline{SCK2}$, SO2 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK2}$... External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY12}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK2}$ high-/low-level width	t_{KH12}, t_{KL12}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK12}		100			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI12}		400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO12}	C = 100 pF Note			300	ns
$\overline{SCK2}$ rise, fall time	t_{R12}, t_{F12}	V_{DD} = 4.5 to 6.0 V, When not using external device expansion function			1000	ns
					160	ns

Note C is the load capacitance of the SO2 output line.

(iii) UART mode (Dedicated baud rate generator output)

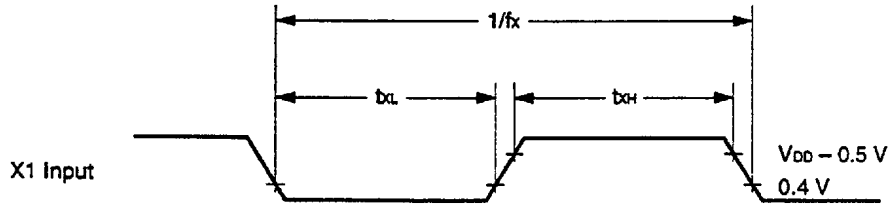
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.5 V ≤ V_{DD} ≤ 6.0 V			78125	bps
		2.7 V ≤ V_{DD} < 4.5 V			39063	bps
					19531	bps

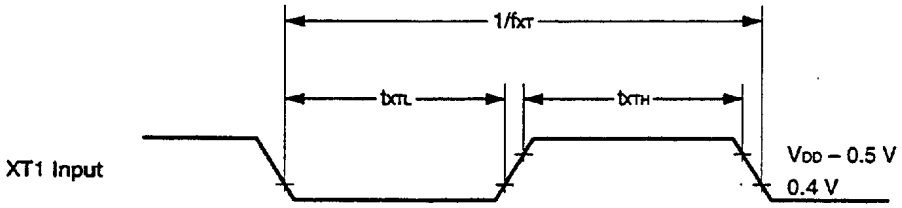
(iv) UART mode (External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY13}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
ASCK high-/low-level width	t_{KH13}, t_{KL13}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
Transfer rate		4.5 V ≤ V_{DD} ≤ 6.0 V			39063	bps
		2.7 V ≤ V_{DD} < 4.5 V			19531	bps
					9766	bps
ASCK rise, fall time	t_{R13}, t_{F13}	V_{DD} = 4.5 to 6.0 V, when not using external device expansion function.			1000	ns
					160	ns

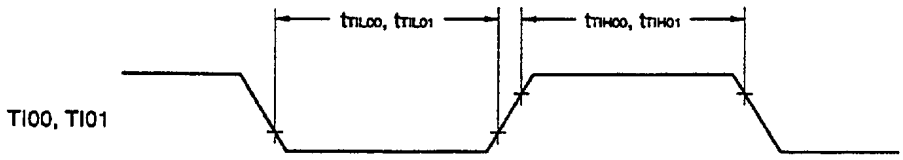
AC Timing Test Point (Excluding X1, XT1 Input)

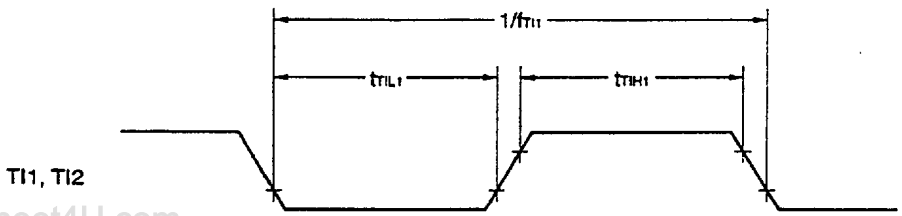
Clock Timing





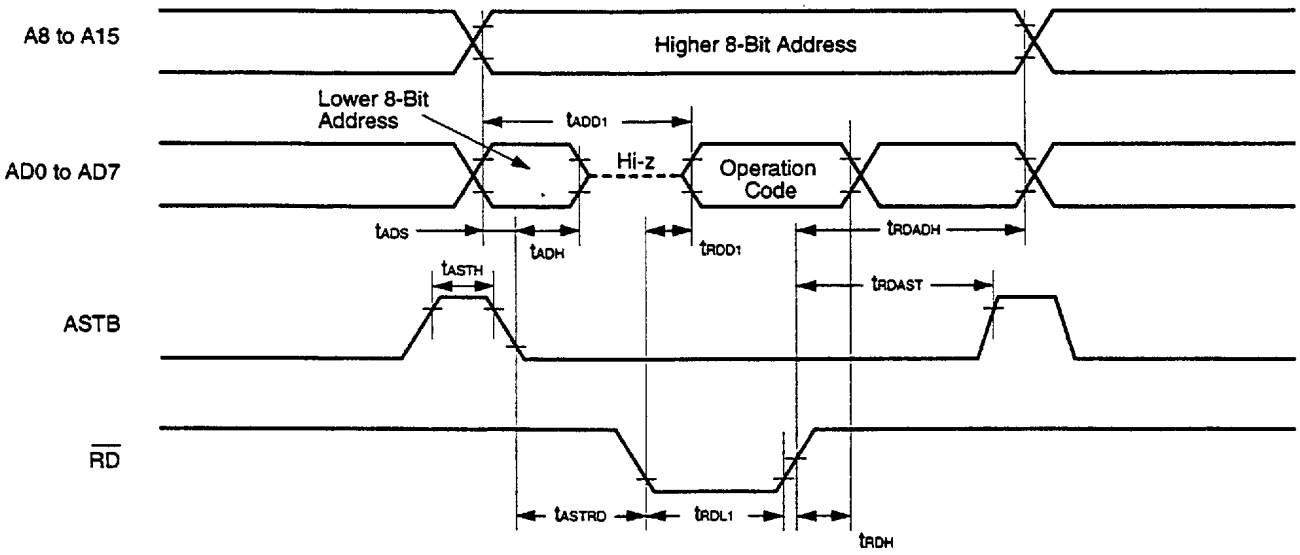
TI Timing



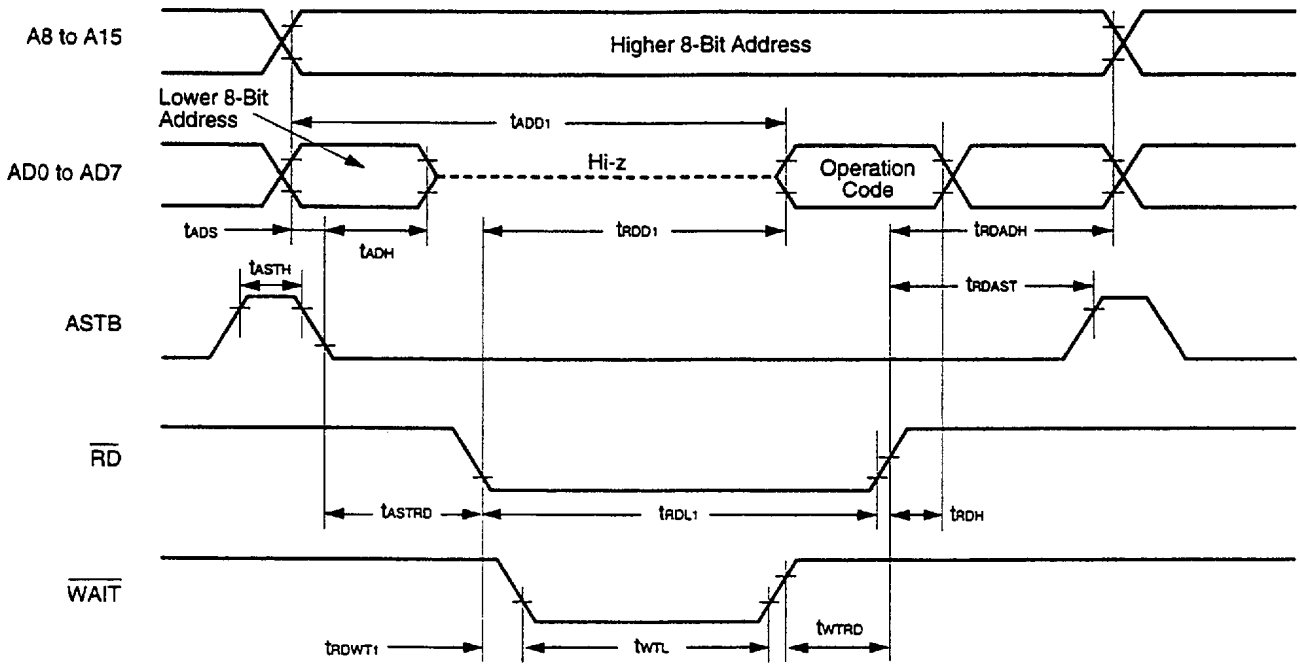


Read/Write Operation

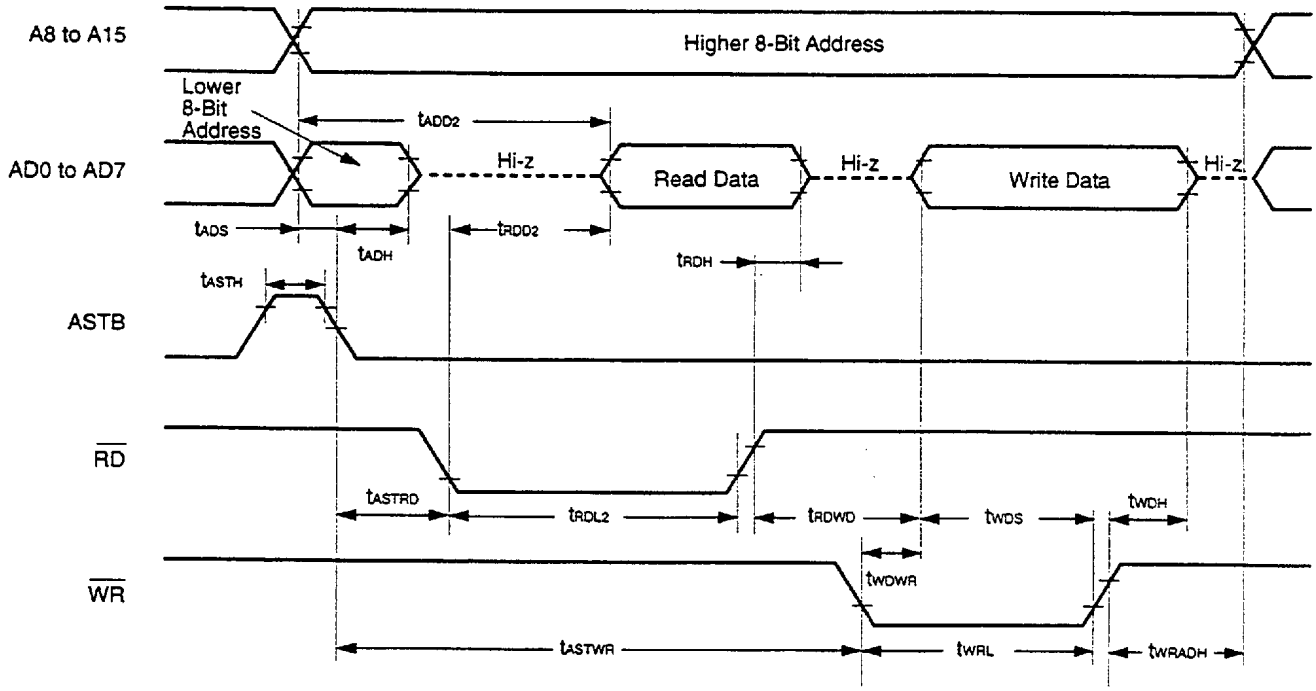
External Fetch (No Wait) :



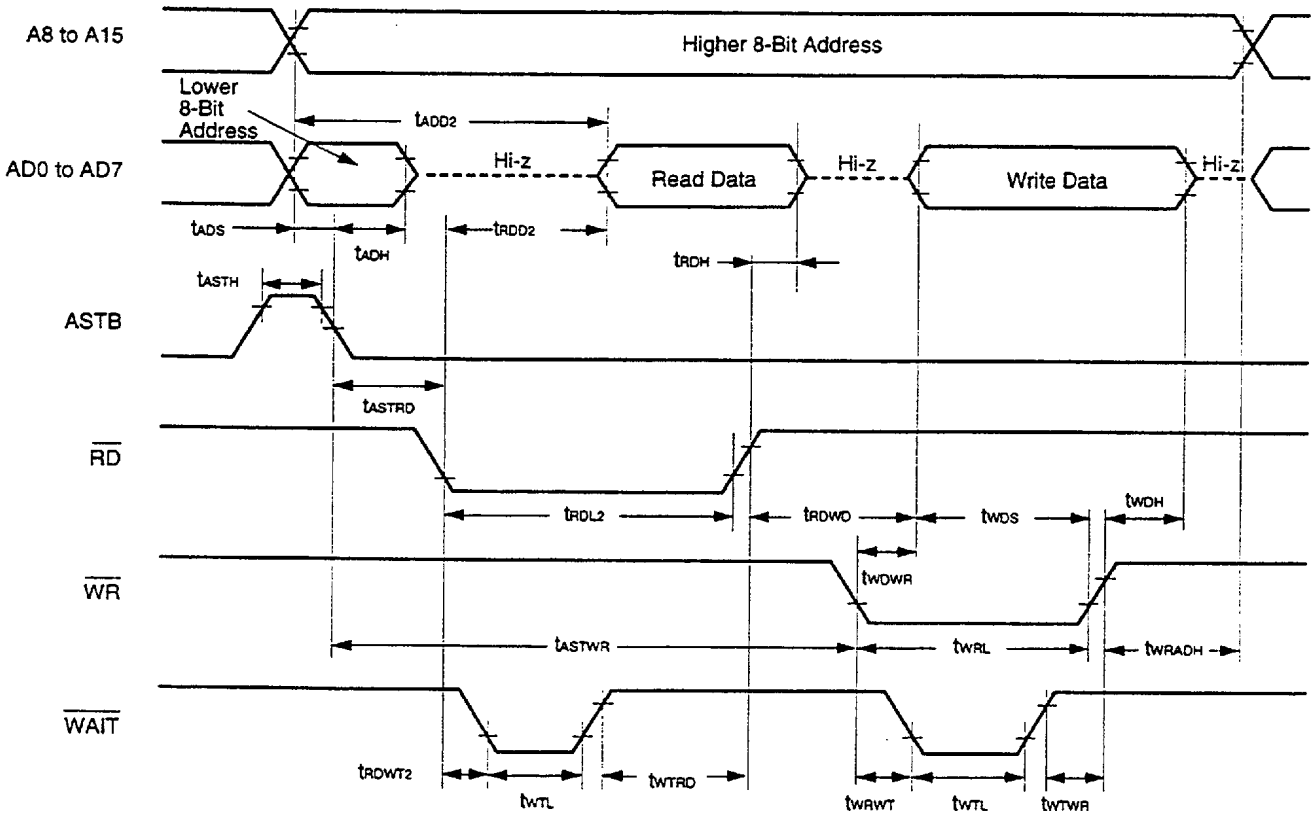
External Fetch (Wait Insertion) :



External Data Access (No Wait) :

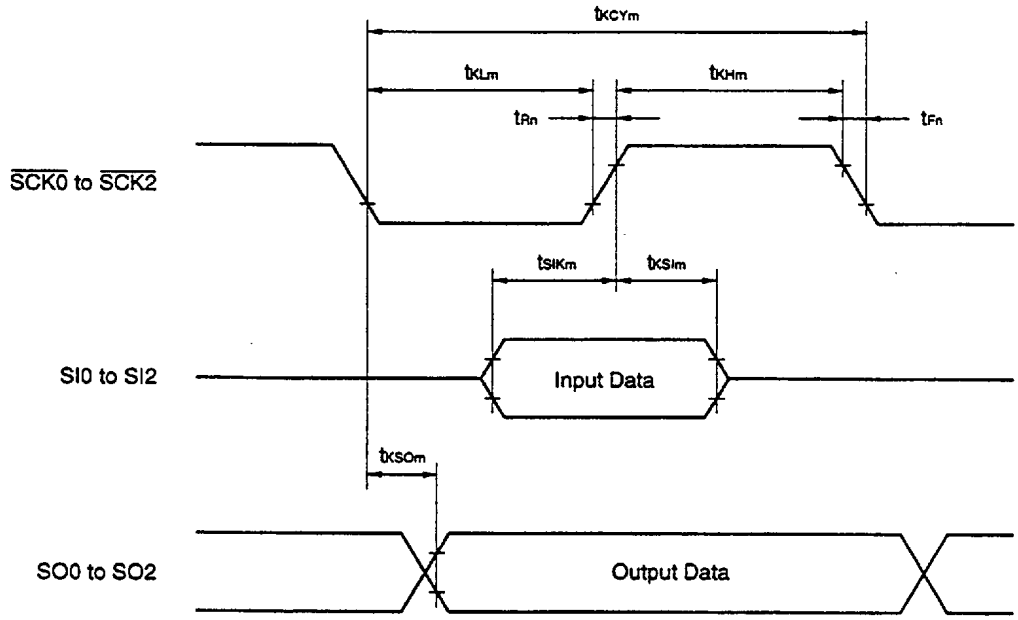


External Data Access (Wait Insertion) :



Serial Transfer Timing

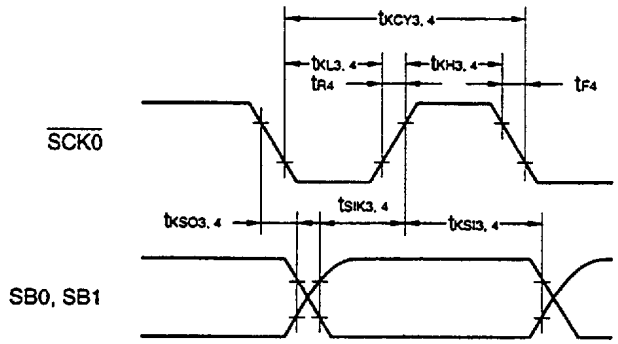
3-wire Serial I/O Mode :



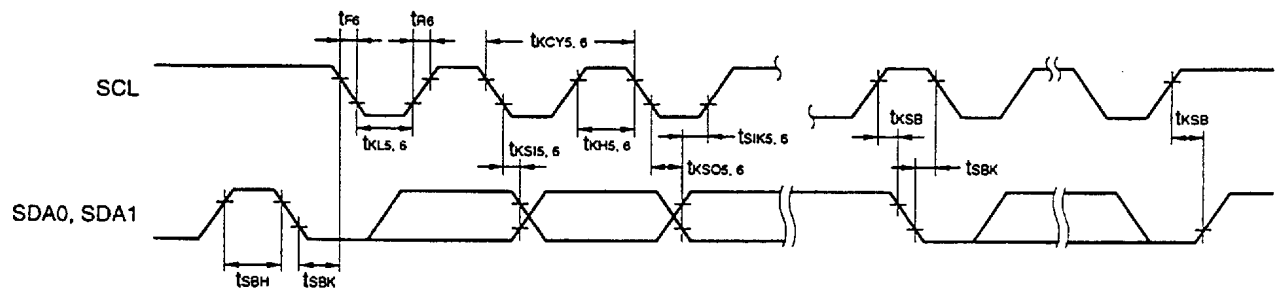
m = 1, 2, 7, 8, 11, 12

n = 2, 8, 12

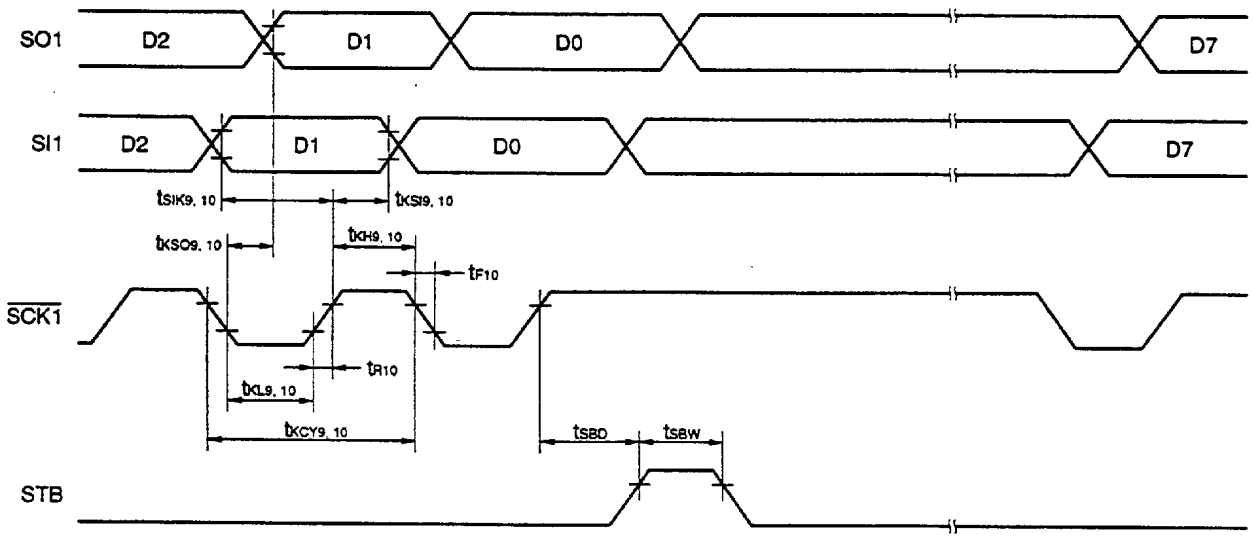
2-wire Serial I/O Mode :



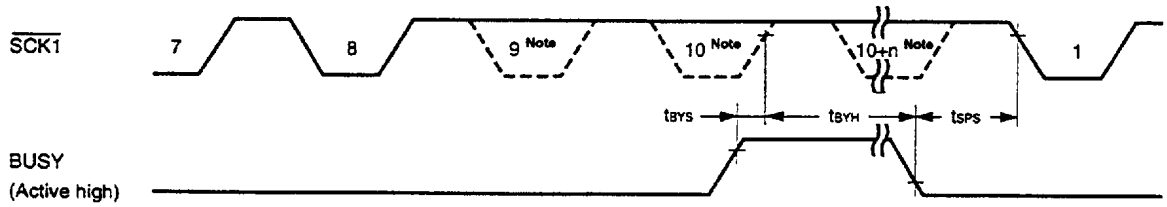
I²C Bus Mode:



3-wire Serial I/O Mode with Automatic Transmit/Receive Function :

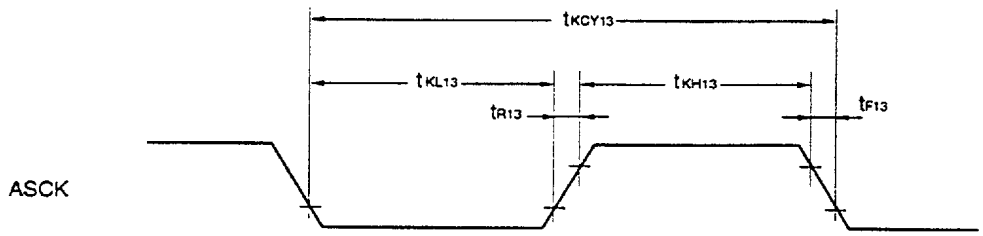


3-wire Serial I/O Mode with Automatic Transmit/Receive Function (Busy Processing) :



Note The signal is not actually driven low here; it is shown as such to indicate the timing.

UART Mode (External Clock Input) :



A/D CONVERTER CHARACTERISTICS (T_A = –40 to +85 °C, AV_{DD} = V_{DD} = 2.0 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error Note		2.7 V ≤ AV_{REF0} ≤ AV_{DD}			0.6	%
		2.0 V ≤ AV_{REF0} < 2.7 V			1.4	%
Conversion time	t_{CONV}		19.1		200	μs
Sampling time	t_{SAMP}		12/fxx			μs
Analog input voltage	V_{IAN}		AVss		AV_{REF0}	V
Reference voltage	AV_{REF0}		2.0		AV_{DD}	V
Resistance between AV_{REF0} and AVss	R_{AIREF0}		4	14		kΩ

Note Overall error excluding quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.

fxx : Main system clock frequency (fx or fx/2)
f_x : Main system clock oscillation frequency

D/A CONVERTER CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Resolution						8	bit
Overall error		R = 2 MΩ Note1				1.2	%
		R = 4 MΩ Note1				0.8	%
		R = 10 MΩ Note1				0.6	%
Settling time		C=30pF Note1	4.5 V ≤ AV_{REF1} ≤ 6.0 V			10	μs
			2.7 V ≤ AV_{REF1} < 4.5 V			15	μs
			2.0 V ≤ AV_{REF1} < 2.7 V			20	μs
Output resistance	R_O	DACS0, DACS1 = 55H Note 2			10		kΩ
Analog reference voltage	AV_{REF1}			2.0		V_{DD}	V
AV_{REF1} current	I_{REF1}	Note2				1.5	mA

Notes 1. R and C denote D/A converter output pin load resistance and load capacitance, respectively.
2. Value for one D/A converter channel

DACS0, DACS1: D/A conversion value setting register.

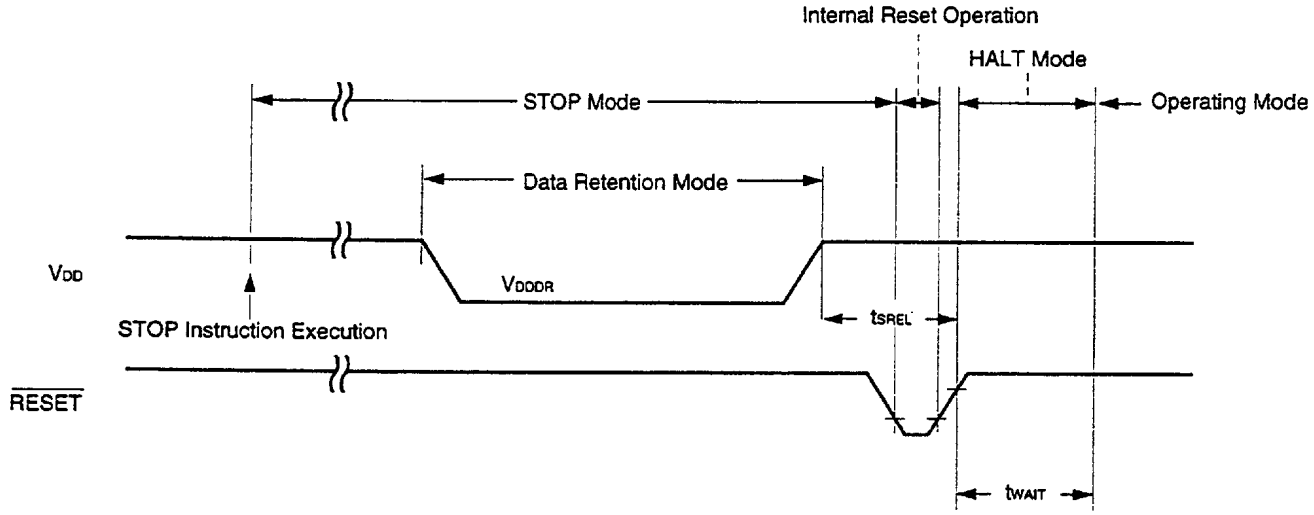
DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (T_A = −40 to +85°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.8		6.0	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 1.8 V Subsystem clock stop and feedback resistor disconnected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabiliation wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/fx$		ms
		Release by interrupt		**Note**		ms

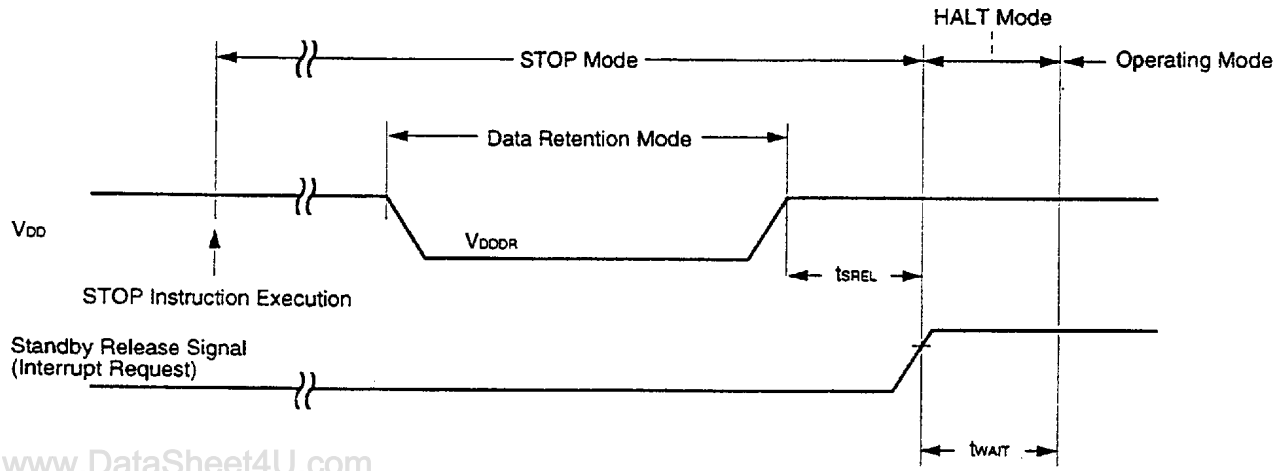
Note In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time selection register (OSTS), selection of $2^{12}/fxx$ and $2^{14}/fxx$ to $2^{17}/fxx$ is possible.

fxx : Main system clock frequency (fx or fx/2)
fx : Main system clock oscillation frequency

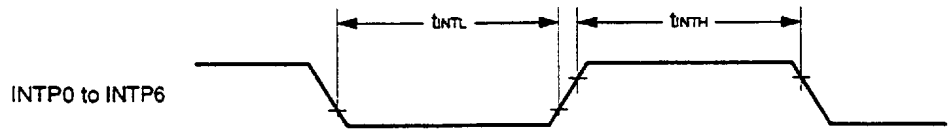
Data Retention Timing (STOP Mode Release by $\overline{RESET}$)



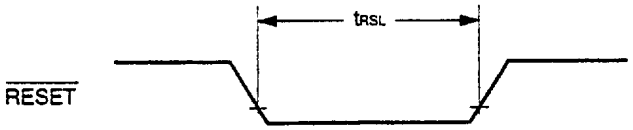
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



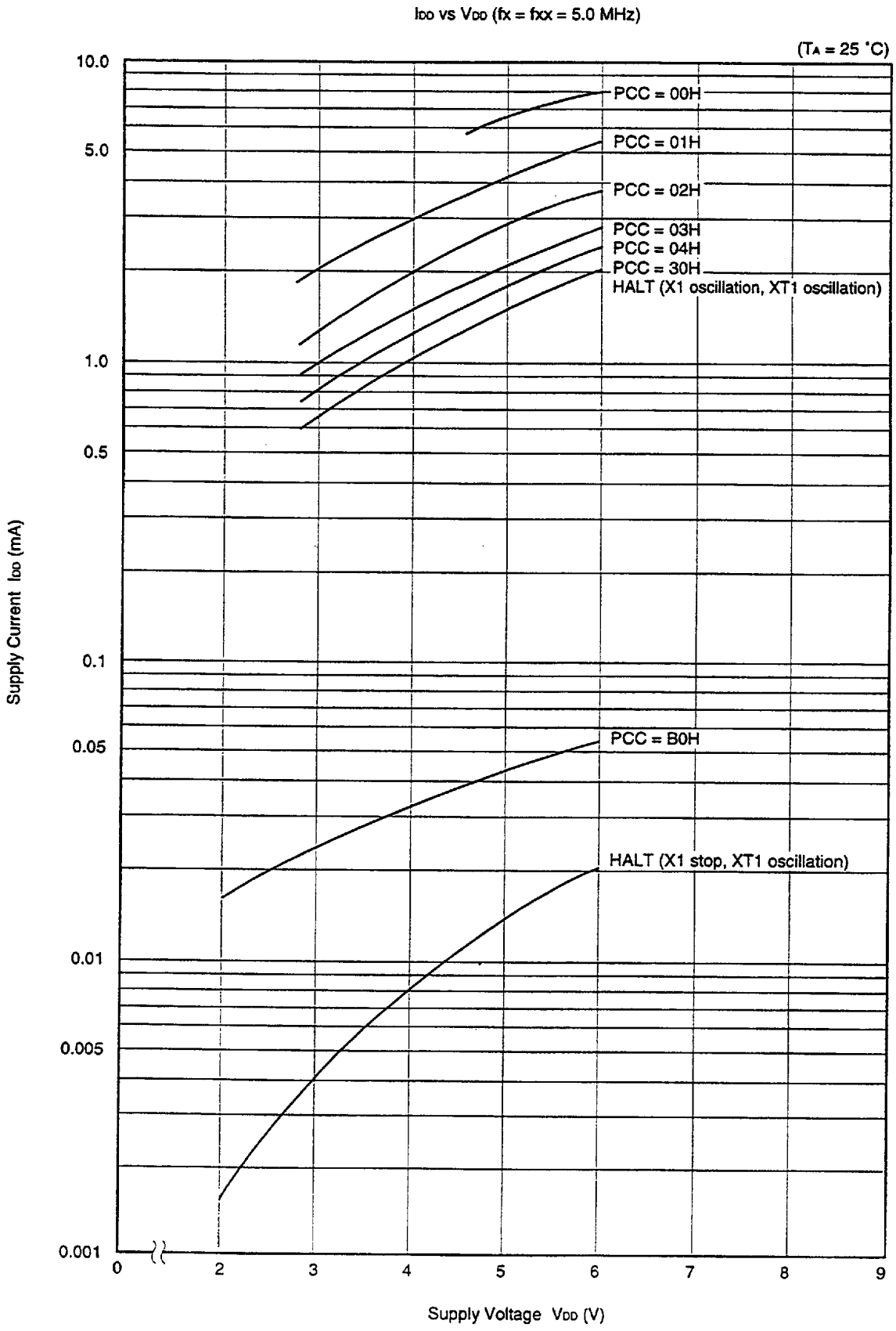
Interrupt Input Timing

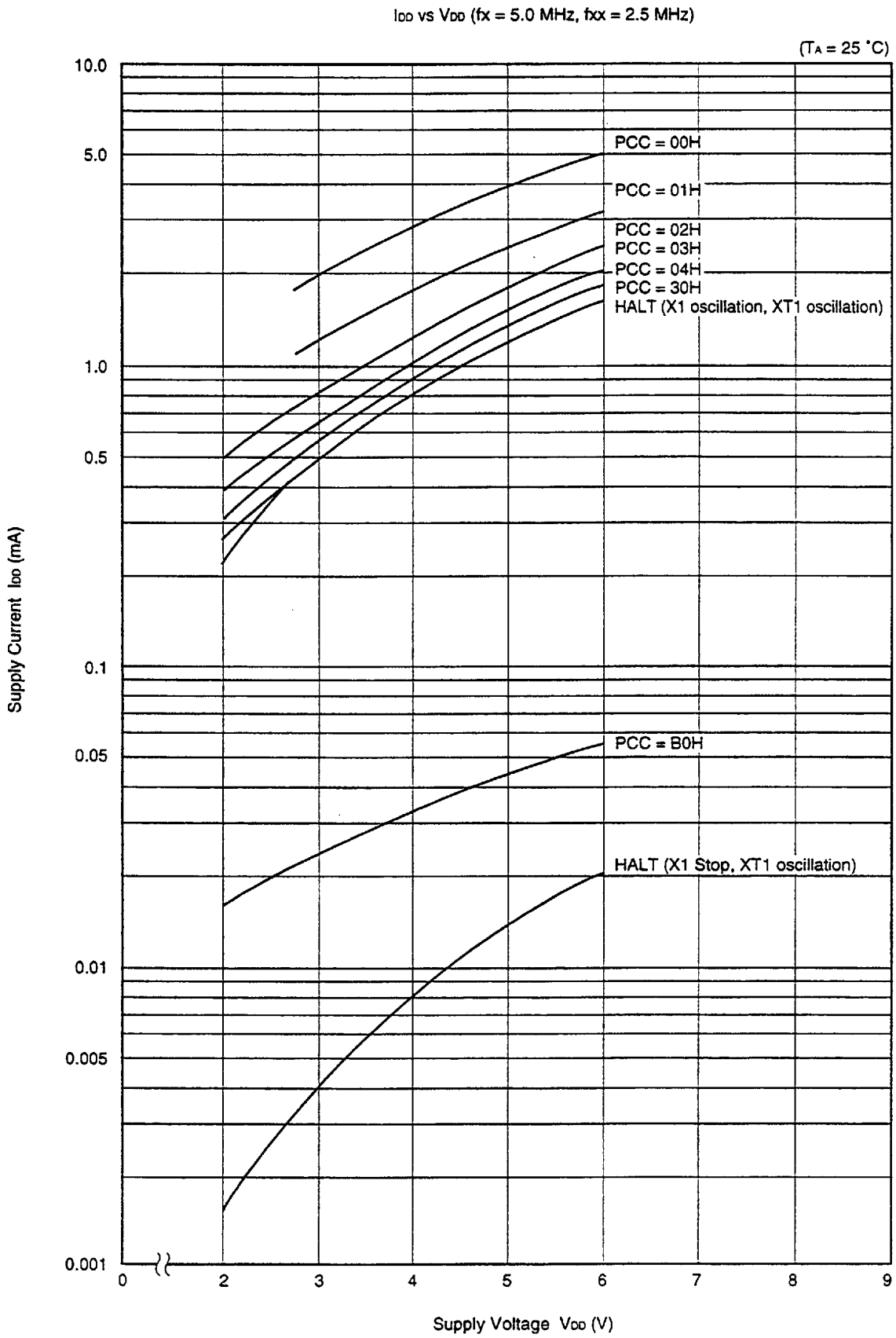


$\overline{\text{RESET}}$ Input Timing



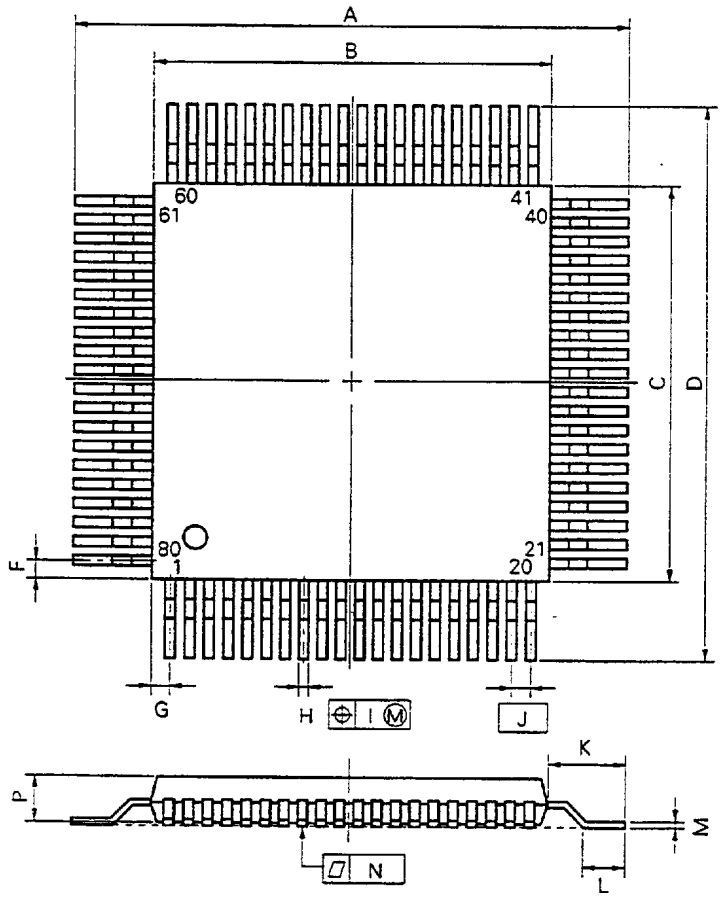
12. CHARACTERISTIC CURVES (REFERENCE VALUE) *



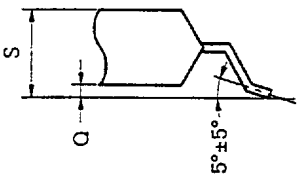


13. PACKAGE DRAWING

80 PIN PLASTIC QFP (□14)



detail of lead end



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S80GC-65-3B9-3

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.8	0.031
G	0.8	0.031
H	$0.30^{+0.10}_{-0.05}$	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

Remark Dimensions and materials of ES product are the same as those of mass-production products. ★

★ 14. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended in the table below.

For a detailed description of recommended soldering conditions, refer to the information document **"Semiconductor Device Mounting Technology Manual" (IEI-1207).**

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 14-1. Surface Mounting Type Soldering Conditions (1/2)

(1) μPD78052YGC-xxx-3B9 : 80-pin plastic QFP (14 x 14 mm)
μPD78053YGC-xxx-3B9 : 80-pin plastic QFP (14 x 14 mm)
μPD78054YGC-xxx-3B9 : 80-pin plastic QFP (14 x 14 mm)
μPD78055YGC-xxx-3B9 : 80-pin plastic QFP (14 x 14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or above), Number of times: Twice max. <precautions> (1) Wait for the device temperature to come down to room temperature after the first reflow before starting the second reflow. (2) Do not perform flux washing of the soldered portion after the first reflow.	IR35-00-2
VPS	Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above), Number of times: Twice max. <precautions> (1) Wait for the device temperature to come down to room temperature after the first reflow before starting the second reflow. (2) Do not perform flux washing of the soldered portion after the first reflow.	VP15-00-2
Partial heating	Pin temperature: 300 °C max. Duration: 3 sec. max. (per pin row)	—

Caution Avoid as much as possible combining two or more soldering methods (except for the partial heating method).

Table 14-1. Surface Mounting Type Soldering Conditions (2/2)

(2) μPD78056YGC-xxx-3B9 : 80-pin plastic QFP (14 x 14 mm)
μPD78058YGC-xxx-3B9 : 80-pin plastic QFP (14 x 14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or above), Number of times: Twice max. <precautions> (1) Wait for the device temperature to come down to room temperature after the first reflow before starting the second reflow. (2) Do not perform flux washing of the soldered portion after the first reflow.	IR35-00-2
VPS	Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above), Number of times: Twice max. <precautions> (1) Wait for the device temperature to come down to room temperature after the first reflow before starting the second reflow. (2) Do not perform flux washing of the soldered portion after the first reflow.	VP15-00-2
Wave soldering	Solder bath temperature : 260 °C max., Duration : 10 sec. max., Number of times: once, Preheating temperature : 120 °C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 °C max. Duration: 3 sec. max. (per pin row)	—

Caution Avoid as much as possible combining two or more soldering methods (except for the partial heating method).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using μPD78054Y subseries.

Language Processing Software

RA78K/0 Notes 1, 2, 3, 4	78K/0 series common assembler package
CC78K/0 Notes 1, 2, 3, 4	78K/0 series common C compiler package
DF78054 Notes 1, 2, 3, 4	Device file common to μPD78054 subseries
CC78K/0-L Notes 1, 2, 3, 4	78K/0 series common C compiler library source file

PROM Writing Tools

PG-1500	PROM programmer
PA-78P054GC PA-78P054KK-T	Programmer adapters connected to PG-1500
PG-1500 controller Notes 1, 2	PG-1500 control program

Debugging Tools

	IE-78000-R	In-circuit emulator common to 78K/0 series
*	IE-78000-R-A Note 8	In-circuit emulator common to 78K/0 series (for integrated debugger)
	IE-78000-R-BK	Break board common to 78K/0 series
	IE-78064-R-EM	Emulation board common to μPD78064 subseries
	EP-78230GC-R	Emulation probe common to μPD78234 subseries
	EV-9200GC-80	Socket to be mounted in the target system board manufactured for 80-pin plastic QFP
*	SM78K0 Notes 5, 6, 7	System simulator common to 78K/0 series
*	ID78K0 Notes 4, 5, 6, 7, 8	Integrated debugger for IE-78000-R-A
	SD78K/0 Notes 1, 2	Screen debugger for IE-78000-R
	DF78054 Notes 1, 2, 5, 6, 7	Device file common to μPD78054 subseries

Real-Time OS

	RX78K/0 Notes 1, 2, 3, 4	Real-time OS for 78K/0 series
*	MX78K0 Notes 1, 2, 3, 4	OS for 78K/0 series

Notes 1. PC-9800 series (MS-DOS™) based
2. IBM PC/AT™ and compatible computer (PC DOS™/IBM DOS™/MS-DOS) based
3. HP9000 Series 300™ (HP-UX™) based
4. HP9000 Series 700™ (HP-UX) based, SPARCstation™ (Sun OS™) based, EWS4800 Series (EWS-UX/V) based
5. PC-9800 Series (MS-DOS + Windows™) based
6. IBM PC/AT and compatible computer (PC DOS/IBM DOS/MS-DOS + Windows) based
7. NEWS™ (NEWS-OS™) based
8. Under development

Fuzzy Inference Development Support System

FE9000 Note 1/ FE9200 Note 2	Fuzzy knowledge data creation tool
FT9080 Note 1/ FT9085 Note 3	Translator
FI78K0 Notes 1, 3	Fuzzy inference module
FD78K0 Notes 1, 3	Fussy inference debugger

Notes 1. PC-9800 series (MS-DOS) based
2. IBM PC/AT and its compatible computers (PC DOS/IBM DOS/MS-DOS + Windows) based
3. IBM PC/AT and its compatible computers (PC DOS/IBM DOS/MS-DOS) based

Remarks 1. For third party development tools, see the **78K/0 Series Selection Guide (IF-1185)**.
2. RA78K/0, CC78K/0, SM78K0, ID78K0, and SD78K/0 are used in combination with DF78054.

★ APPENDIX B. RELATED DOCUMENTS

Device Related Documents

Document Name		Document No. (Japanese)	Document No. (English)
μPD78054 and μPD78054Y Subseries User's Manual		IEU-824	IEU-1356
78K/0 Series User's Manual Instructions		IEU-849	IEU-1372
78K/0 Series Instruction Set		U10904J	–
78K/0 Series Instruction Table		U10903J	–
μPD78054Y Special Function Register Table		U10087J	–
78K/0 Series Application Note	Basics (III)	IEA-767	U10182E

Development Tool Related Documents (User's Manual)

Document Name		Document No. (Japanese)	Document No. (English)
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K/0 C Compiler Application Note	Programming Know-How	EEA-618	EEA-1208
CC78K Series Library Source File		EEU-777	–
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller PC-9800 Series (MS-DOS) Based		EEU-704	EEU-1291
PG-1500 Controller IBM PC Series (PC DOS) Based		EEU-5008	U10540E
IE-78000-R		EEU-810	EEU-1398
IE-78000-R-A		U10057J	U10057E
IE-78000-R-BK		EEU-867	EEU-1427
IE-78064-R-EM		EEU-905	EEU-1443
EP-78230		EEU-985	EEU-1515
SM78K0 System Simulator	Reference	EEU-5002	U10181E
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092J	U10092E
SD78K/0 Screen Debugger PC-9800 Series (MS-DOS) Based	Introduction	EEU-852	–
	Reference	EEU-816	–
SD78K/0 Screen Debugger IBM PC/AT (PC DOS) Based	Introduction	EEU-5024	EEU-1414
	Reference	EEU-993	EEU-1413

Caution The above documents are subject to change without notice. For design purpose, etc., be sure to use the latest document.

Embedded Software Documents (User's Manual)

Document Name		Document No. (Japanese)	Document No. (English)
78K/0 Series Real Time OS	Basics	EEU-912	–
	Installation	EEU-911	–
	Technical	EEU-913	–
MX78K0: OS for 78K/0 Series	Basic	EEU-5010	–
Fuzzy Knowledge Data Creation Tools		EEU-829	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-921	EEU-1458

Other Documents

Document Name	Document No. (Japanese)	Document No. (English)
Semiconductor Device Package Manual	IEI-635	IEI-1213
Semiconductor Device Mounting Technology Manual	IEI-616	IEI-1207
Quality Grades on NEC Semiconductor Device	IEI-620	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System	IEM-5068	IEI-1203
Electrostatic Discharge (ESD) Test	MEM-539	MEI-1201
Guide to Quality Assurance for Semiconductor Devices	MEI-603	MEI-1202
Microcomputer-related Product Guide, Third Party Products	MEI-604	–

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