



UCD4021B

Preliminary

CMOS IC

CMOS 8-STAGE STATIC SHIFT REGISTERS

DESCRIPTION

The **UCD4021B** is a 8-stage synchronous parallel or serial input/serial output registers having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a SERIAL data input, and individual parallel inputs to each register stage. Each register is a D-type, master-slave flip-flop. Q6, Q7, and Q8 are outputs. In **UCD4021B** serial entry is synchronous with the clock but parallel entry is asynchronous.

In **UCD4021B** serial entry is controlled by the PARALLEL/SERIAL CONTROL input. When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the PARALLEL/SERIAL CONTROL input is high, asynchronous parallel entry is made and the CLOCK input of the internal stage is isolated.

FEATURES

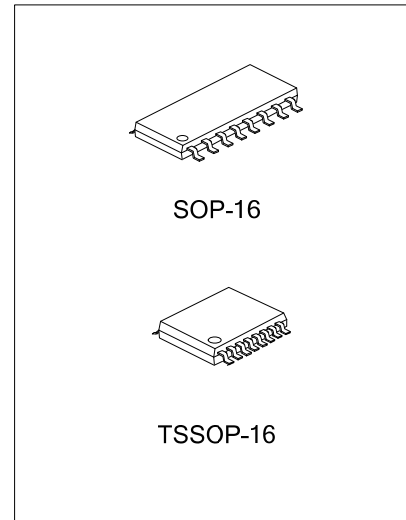
- * Up to 20V operation voltage
- * 12MHz (Typ.) clock rate at 10V
- * Maximum input current of 1µA at 18V
- * Fully static operation
- * 8 master-slave flip-flops plus output buffering and control gating

APPLICATIONS

- * General-purpose register
- * Parallel input/serial output data queueing
- * Parallel to serial data conversion

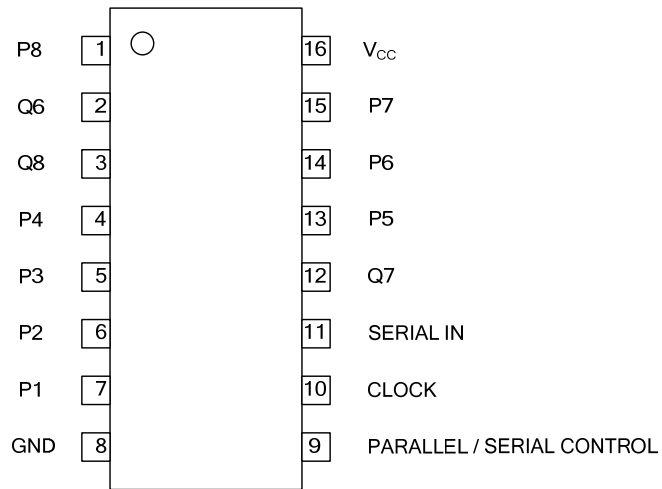
ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCD4021BL-S16-R	UCD4021BG-S16-R	SOP-16	Tape Reel
UCD4021BL-S16-T	UCD4021BG-S16-T	SOP-16	Tube
UCD4021BL-P16-R	UCD4021BG-P16-R	TSSOP-16	Tape Reel
UCD4021BL-P16-T	UCD4021BG-P16-T	TSSOP-16	Tube

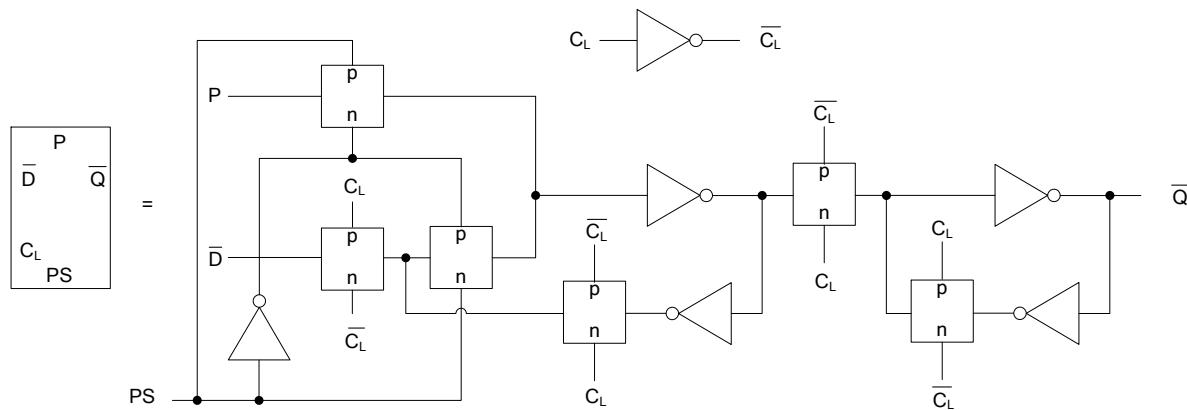
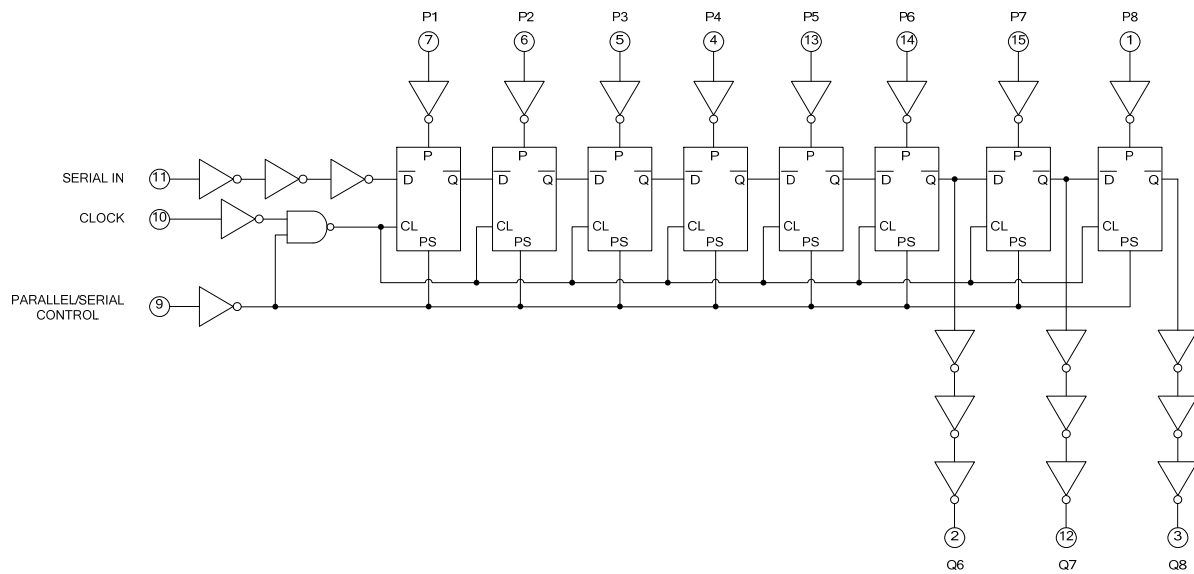


<p>UCD4021BL-S16-R</p> <p>(1)Packing Type (2)Package Type (3)Lead Free</p>	<p>(1) T: Tube, R: Tape Reel (2) S16: SOP-16, P16: TSSOP-16 (3) L: Lead Free, G: Halogen Free</p>
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■ PIN CONFIGURATION



LOGIC DIAGRAM



TRUE TABLE

C_L	SER IN	PAR SER CONTROL	P_1	P_n	Q_1 (INTERNAL)	Q_n
X	X	1	0	0	0	0
X	X	1	0	1	0	1
X	X	1	1	0	1	0
X	X	1	1	1	1	1
\uparrow	0	0	X	X	0	Q_{n-1}
\uparrow	1	0	X	X	1	Q_{n-1}
\downarrow	X	0	X	X	Q_1 (NC)	Q_n (NC)

NOTE: X = DON'T CARE CASE, NC = NO CHANGE

■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 20	V
Input Voltage	V_{IN}	-0.5 ~ $V_{CC} + 0.5$	V
Output Voltage	V_{OUT}	-0.5 ~ $V_{CC} + 0.5$	V
Input Clamp Current ($V_{IN} < 0$, or $V_{IN} > V_{CC}$)	I_{IK}	±10	mA
Power Dissipation	P_D	$T_A = -40^{\circ}\text{C} \sim +100^{\circ}\text{C}$	500
		$T_A = +100^{\circ}\text{C} \sim +125^{\circ}\text{C}$	200
Storage Temperature	T_{STG}	-65 ~ +150	$^{\circ}\text{C}$

Note: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	SOP-16	73
		TSSOP-16	108

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		3		18	V
Clock Pulse Width	t_w	$V_{CC} = 5\text{V}$	180			ns
		$V_{CC} = 10\text{V}$	80			
		$V_{CC} = 15\text{V}$	50			
Clock Frequency	f_{CL}	$V_{CC} = 5\text{V}$			3	MHz
		$V_{CC} = 10\text{V}$			6	
		$V_{CC} = 15\text{V}$			8.5	
Clock Rise and Fall Time	t_r, t_f	$V_{CC} = 5\text{V}$			15	μs
		$V_{CC} = 10\text{V}$			15	
		$V_{CC} = 15\text{V}$			15	
Set-up Time, Serial Input	t_s	$V_{CC} = 5\text{V}$	120			ns
		$V_{CC} = 10\text{V}$	80			
		$V_{CC} = 15\text{V}$	60			
Set-up Time, Parallel Inputs	t_s	$V_{CC} = 5\text{V}$	50			ns
		$V_{CC} = 10\text{V}$	30			
		$V_{CC} = 15\text{V}$	20			
Parallel/Serial Pulse Width	t_w	$V_{CC} = 5\text{V}$	160			ns
		$V_{CC} = 10\text{V}$	80			
		$V_{CC} = 15\text{V}$	50			
Parallel/Serial Removal Time	t_{REM}	$V_{CC} = 5\text{V}$	280			ns
		$V_{CC} = 10\text{V}$	140			
		$V_{CC} = 15\text{V}$	100			

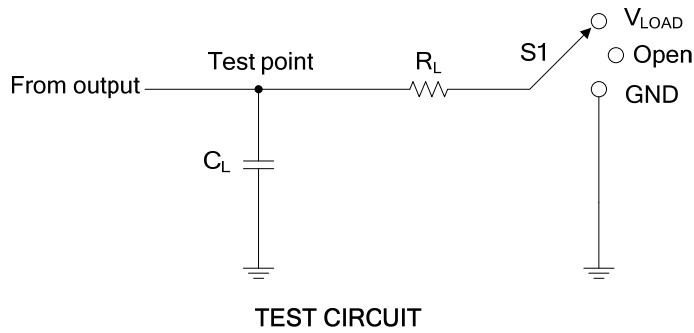
■ ELECTRICAL CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Quiescent Supply Current	I _{DD}	V _{IN} =0, 5V, V _{DD} =5V		0.04	5	μA
		V _{IN} =0, 10V, V _{DD} = 0V		0.04	10	
		V _{IN} =0, 15V, V _{DD} =15V		0.04	20	
		V _{IN} =0, 20V, V _{DD} =20V		0.08	100	
Output Low (Sink) Current	I _{OL}	V _{OUT} =0.4V, V _{IN} =0, 5V, V _{DD} =5V	0.51	1		mA
		V _{OUT} =0.5V, V _{IN} =0, 10V, V _{DD} =10V	1.3	2.6		
		V _{OUT} =1.5V, V _{IN} =0, 15V, V _{DD} =15V	3.4	6.8		
Output High (Source) Current	I _{OH}	V _{OUT} =4.6V, V _{IN} =0, 5V, V _{DD} =5V	-0.51	-1		mA
		V _{OUT} =2.5V, V _{IN} =0, 5V, V _{DD} =5V	-1.6	-3.2		
		V _{OUT} =9.5V, V _{IN} =0, 10V, V _{DD} =10V	-1.3	-2.6		
		V _{OUT} =3.5V, V _{IN} =0, 15V, V _{DD} =15V	-3.4	-6.8		
Output Voltage: Low-Level	V _{OL}	V _{IN} =0, 5V, V _{DD} =5V		0	0.05	V
		V _{IN} =0, 10V, V _{DD} =10V		0	0.05	
		V _{IN} =0, 15V, V _{DD} =15V		0	0.05	
Output Voltage: High-Level	V _{OH}	V _{IN} =0, 5V, V _{DD} =5V	4.95	5		V
		V _{IN} =0, 10V, V _{DD} =10V	9.95	10		
		V _{IN} =0, 15V, V _{DD} =15V	14.95	15		
Input Low Voltage	V _{IL}	V _{OUT} =0.5, 4.5V, V _{DD} =5V			1.5	V
		V _{OUT} =1, 9V, V _{DD} =10V			3	
		V _{OUT} =1.5, 13.5V, V _{DD} =15V			4	
Input High Voltage	V _{IH}	V _{OUT} =0.5, 4.5V, V _{DD} =5V	3.5			V
		V _{OUT} =1, 9V, V _{DD} =10V	7			
		V _{OUT} =1.5, 13.5V, V _{DD} =15V	11			
Input Leakage Current	I _{I(LEAK)}	V _{IN} =0, 18 V, V _{DD} =18V		±10 ⁻⁵	±0.1	μA

■ SWITCHING CHARACTERISTICS (T_A = 25°C, Input t_r, t_f = 20ns, C_L = 50Pf, R_L = 200KΩ)

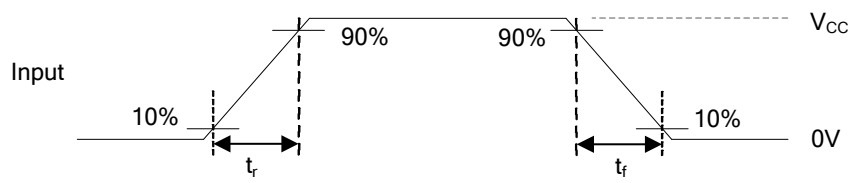
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time	t _{PLH} / t _{PHL}	V _{DD} =5V		160	320	ns
		V _{DD} =10V		80	160	
		V _{DD} =15V		60	120	
Transition Time	t _{THL} / t _{TLH}	V _{DD} =5V		100	200	ns
		V _{DD} =10V		50	100	
		V _{DD} =15V		40	80	
Maximum Clock Input Frequency	f _{CL}	V _{DD} =5V	3	6		MHz
		V _{DD} =10V	6	12		
		V _{DD} =15V	8.5	17		
Minimum Clock Pulse Width	t _w	V _{DD} =5V		90	180	ns
		V _{DD} =10V		40	80	
		V _{DD} =15V		25	50	
Clock Rise and Fall Time	t _r / t _f	V _{DD} =5V			15	μs
		V _{DD} =10V			15	
		V _{DD} =15V			15	
Minimum Setup Time, Serial Inputs	t _s	V _{DD} =5V		60	120	ns
		V _{DD} =10V		40	80	
		V _{DD} =15V		30	60	
Minimum Setup Time, Parallel Inputs	t _s	V _{DD} =5V		25	50	ns
		V _{DD} =10V		15	30	
		V _{DD} =15V		10	20	
Minimum Setup Time, Parallel/Serial Control	t _s	V _{DD} =5V		90	180	ns
		V _{DD} =10V		40	80	
		V _{DD} =15V		30	60	
Minimum Hold Time, Serial In, Parallel In, Parallel/Serial Control	t _H	V _{DD} =5V			0	ns
		V _{DD} =10V			0	
		V _{DD} =15V			0	
Minimum P/S Pulse Width	t _{WH}	V _{DD} =5V		80	160	ns
		V _{DD} =10V		40	80	
		V _{DD} =15V		25	50	
Minimum P/S Removal Time	t _{REM}	V _{DD} =5V		140	280	ns
		V _{DD} =10V		70	140	
		V _{DD} =15V		50	100	
Average Input Capacitance	C _I	Any Input		5	7.5	pF

■ TEST CIRCUIT AND WAVEFORMS

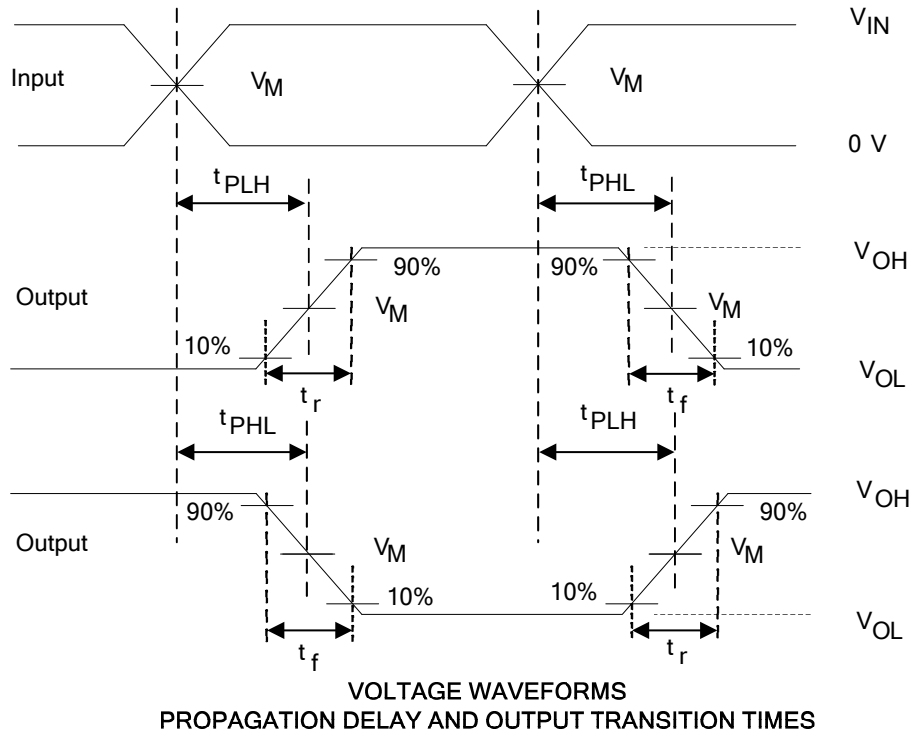


TEST	S1
t_{PLH}/t_{PHL}	GND

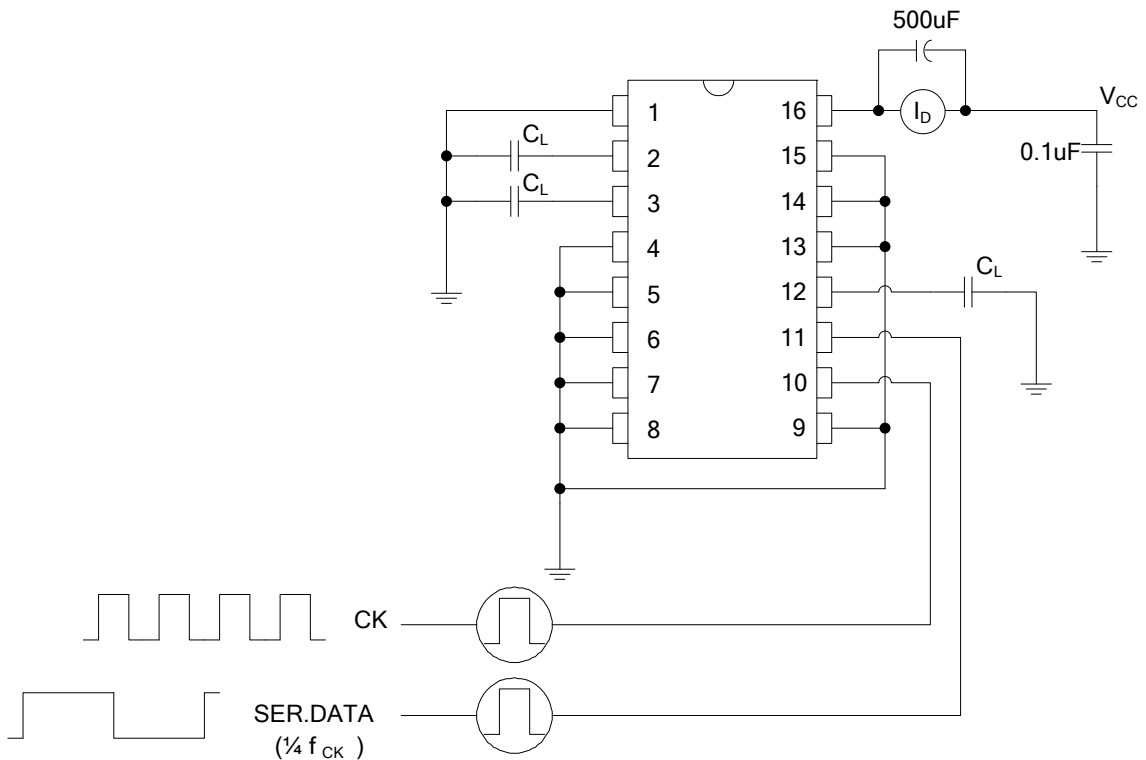
INPUTS		V_M	V_{LOAD}	C_L	R_L
V_{IN}	t_r, t_f				
V_{CC}	20 ns	$V_{CC}/2$	V_{CC}	50 pF	200 K Ω



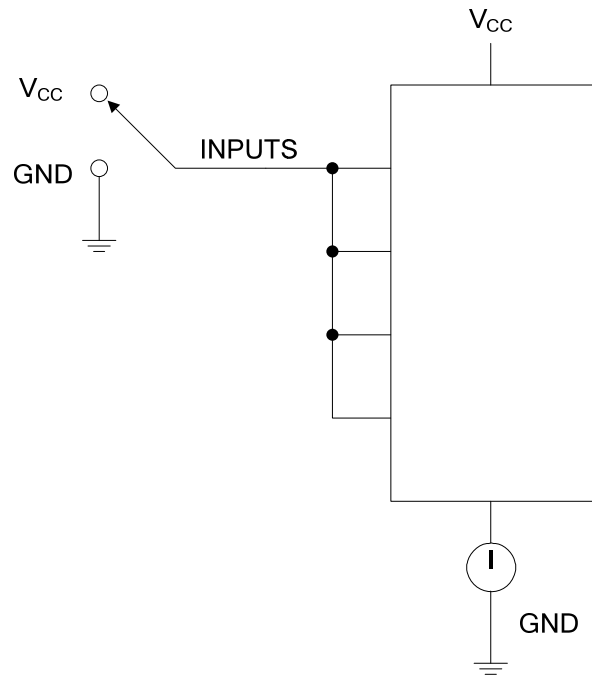
■ TEST CIRCUIT AND WAVEFORMS(Cont.)



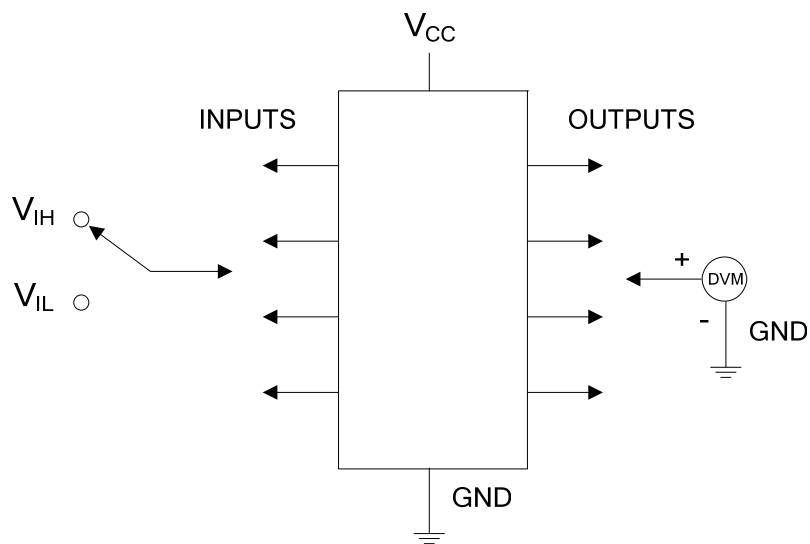
- Notes: 1. C_L includes probe and jig capacitance.
 2. All input pulses are supplied by generators having the following characteristics: PRR \leq 1MHz, $Z_O = 50\Omega$.



■ TEST CIRCUIT AND WAVEFORMS(Cont.)

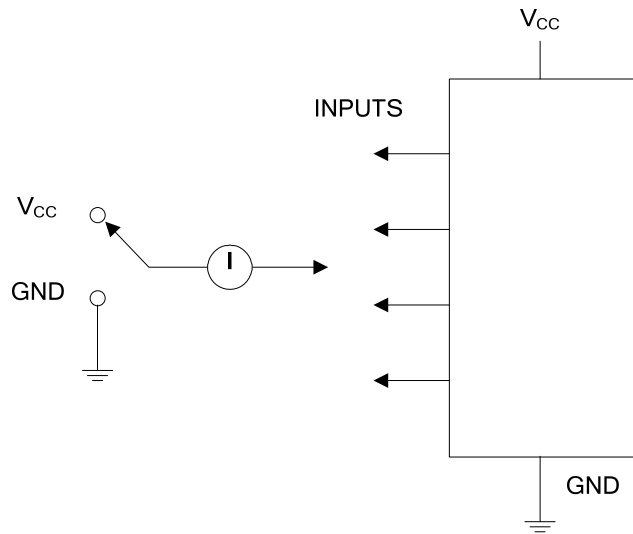


QUIESCENT DEVICE CURRENT TEST CIRCUIT



INPUT VOLTAGE TEST CIRCUIT

■ TEST CIRCUIT AND WAVEFORMS(Cont.)

**INPUT CURRENT TEST CIRCUIT**

Note: measure inputs sequentially, to both V_{CC} and GND; connect all unused inputs to either V_{CC} or GND.

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