

August 1991

Features

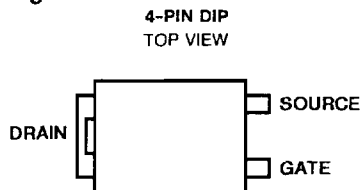
- 0.5A and 0.4A, 350V - 400V
- $r_{DS(on)} = 1.8\Omega$ and 2.5Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

The IRFD320, IRFD332, IRFD322, and IRFD323 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFD320R, IRFD332R, IRFD322R, and IRFD323R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

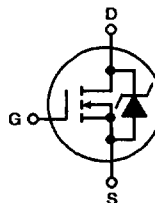
The IRFD types are supplied in the 4-pin dual-in-line plastic package.

Package



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$), Unless Otherwise Specified

	IRFD320 IRFD320R	IRFD332 IRFD332R	IRFD322 IRFD322R	IRFD323 IRFD323R	UNITS	
Drain-Source Voltage (1)	V_{DS}	400	350	400	350	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$) (1)	V_{DGR}	400	350	400	350	V
Continuous Drain Current						
$T_C = +25^\circ\text{C}$	I_D	0.5	0.5	0.4	0.4	A
Pulsed Drain Current (3)	I_{DM}	2.0	2.0	1.6	1.6	A
Gate-Source Voltage	V_{GS}	± 20	± 20	± 20	± 20	V
Maximum Power Dissipation						
$T_C = +25^\circ\text{C}$ (See Figure 13)	P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)		0.008	0.008	0.008	0.008	W/ $^\circ\text{C}$
Inductive Current, Clamped	I_{LM}	2.0	2.0	1.6	1.6	A
(See Figure 14, $L = 100\mu\text{H}$)						
Single Pulse Avalanche Energy Rating (4)	E_{AS}^*	100	100	100	100	mJ
Operating and Storage Junction	T_J, T_{STG}	-55 to $+150$	-55 to $+150$	-55 to $+150$	-55 to $+150$	$^\circ\text{C}$
Temperature Range						
Maximum Lead Temperature for Soldering	T_L	300	300	300	300	$^\circ\text{C}$
(0.063" (1.6mm) from case for 10s)						

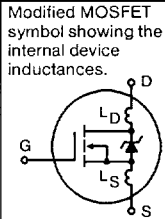
NOTES:

1. $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$.
2. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. $V_{DD} = 40\text{V}$, starting $T_J = +25^\circ\text{C}$, $L = 29.09\text{mH}$, $R_{GS} = 50\Omega$, $I_{PEAK} = 2.5\text{A}$. See Figure 15.

* R Suffix Types Only

Electrical Characteristics $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Drain-Source Breakdown Voltage IRFD320/322, IRFD320R/322R IRFD321/323, IRFD321R/323R	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	400	-	-	V
			350	-	-	V
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I _{GSS}	V _{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I _{GSS}	V _{GS} = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = Max Rating, V _{GS} = 0V	-	-	250	μA
		V _{DS} = Max Rating x 0.8, V _{GS} = 0V, T _C = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRFD320/321, IRFD320R/321R IRFD322/323, IRFD322R/323R	I _{D(ON)}	V _{DS} > I _{D(ON)} × r _{DS(ON)} Max, V _{GS} = 10V	0.5	-	-	A
			0.4	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFD320/321, IRFD320R/321R IRFD322/323, IRFD322R/323R	r _{DS(ON)}	V _{GS} = 10V, I _D = 0.25A	-	1.5	1.8	Ω
			-	1.8	2.5	Ω
Forward Transconductance (Note 2)	g _{fs}	V _{DS} > I _{D(ON)} × r _{DS(ON)} Max, I _D = 0.25A	1.0	2.0	-	S(Ω)
Input Capacitance	C _{ISS}	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz	-	455	-	pF
Output Capacitance	C _{OSS}	See Figure 10	-	100	-	pF
Reverse Transfer Capacitance	C _{RSS}		-	20	-	pF
Turn-On Delay Time	t _{d(ON)}	V _{DD} ≈ 0.5BV _{DSS} , I _D = 0.5A, R _G = 9.1Ω	-	20	40	ns
Rise Time	t _r	See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	25	50	ns
Turn-Off Delay Time	t _{d(OFF)}		-	50	100	ns
Fall Time	t _f		-	25	50	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q _g	V _{GS} = 10V, I _D = 0.5A, V _{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	12	15	nC
Gate-Source Charge	Q _{gs}		-	6.0	-	nC
Gate-Drain ("Miller") Charge	Q _{gd}		-	6.0	-	nC
Internal Drain Inductance	L _D	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die.	-	4.0	-	nH
Internal Source Inductance	L _S	Measured from the source lead, 2.0mm (0.08") from package to source bonding pad.	-	6.0	-	nH
Junction-to-Ambient	R _{θJA}	Free air operation	-	-	120	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I _S	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.	-	-	0.5	A
Pulse Source Current (Body Diode) (Note 3)	I _{SM}		-	-	2.0	A
Diode Forward Voltage (Note 2)	V _{SD}	T _J = +25°C, I _S = 2.0A, V _{GS} = 0V	-	-	1.6	V
Reverse Recovery Time	t _{rr}	T _J = +150°C, I _F = 2.0A, dI _F /dt = 100A/μs	-	450	-	ns
Reverse Recovered Charge	Q _{RR}	T _J = +150°C, I _F = 2.0A, dI _F /dt = 100A/μs	-	3.1	-	μC
Forward Turn-on Time	t _{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .	-	-	-	-

NOTES:

- T_J = +25°C to +150°C
- Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
- Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
- V_{DD} = 40V, starting T_J = +25°C, L = 29.09mH, R_{GS} = 50Ω, I_{PEAK} = 2.5A. (See Figure 15.)

4
N-CHANNEL
POWER MOSFETS

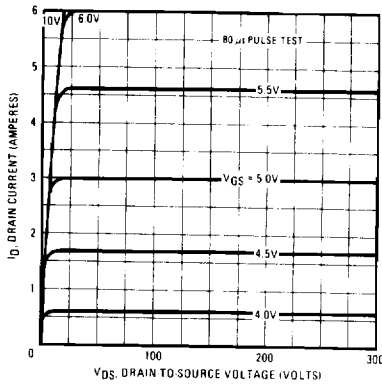


Fig. 1 — Typical Output Characteristics

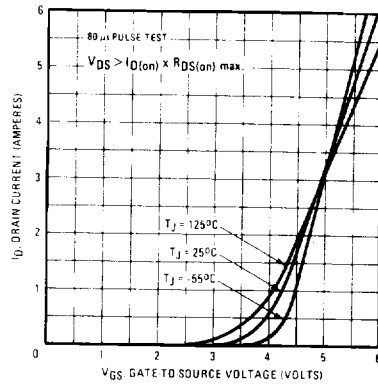


Fig. 2 — Typical Transfer Characteristics

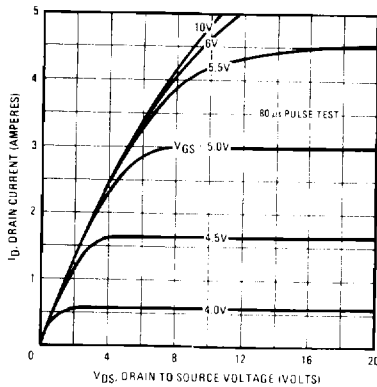


Fig. 3 — Typical Saturation Characteristics

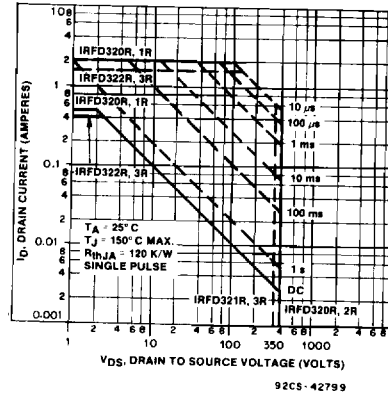


Fig. 4 — Maximum Safe Operating Area

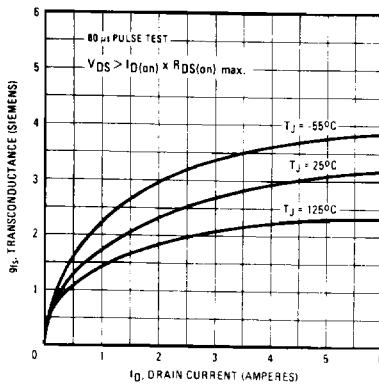


Fig. 5 — Typical Transconductance Vs. Drain Current

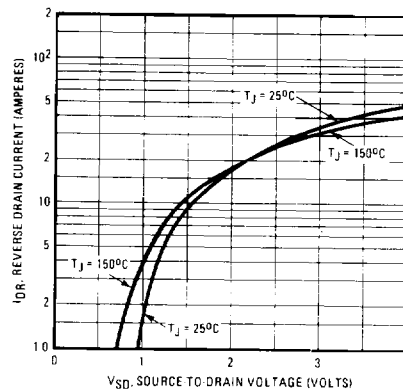


Fig. 6 — Typical Source-Drain Diode Forward Voltage

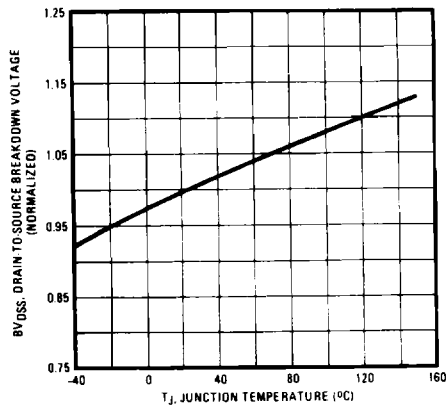


Fig. 7 — Breakdown Voltage Vs. Temperature

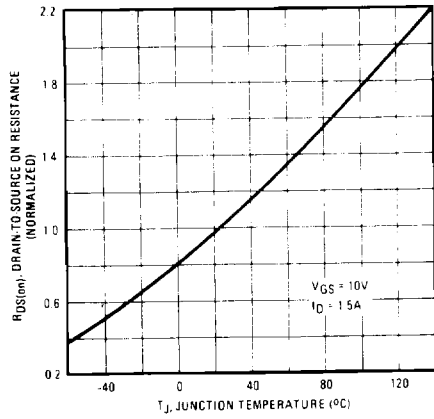


Fig. 8 — Normalized On-Resistance Vs. Temperature

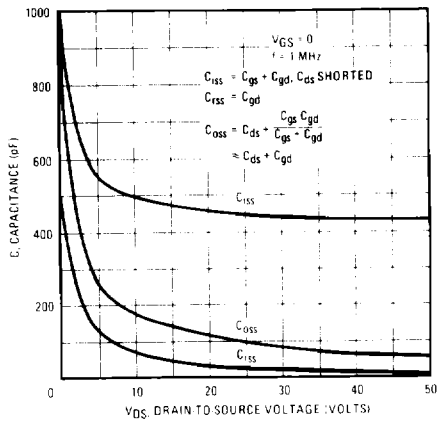


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

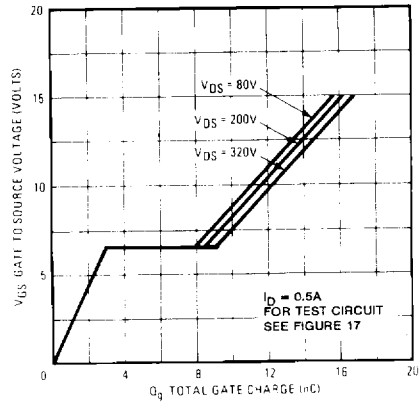


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

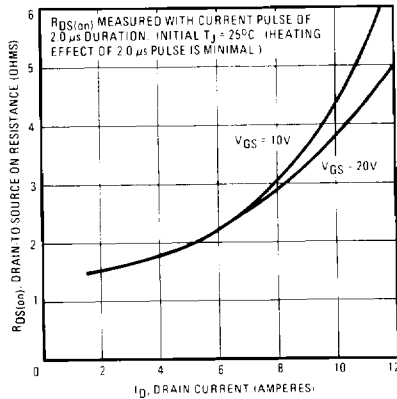


Fig. 11 — Typical On-Resistance Vs. Drain Current

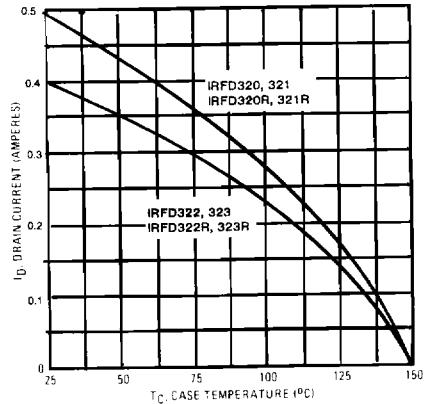


Fig. 12 — Maximum Drain Current Vs. Case Temperature

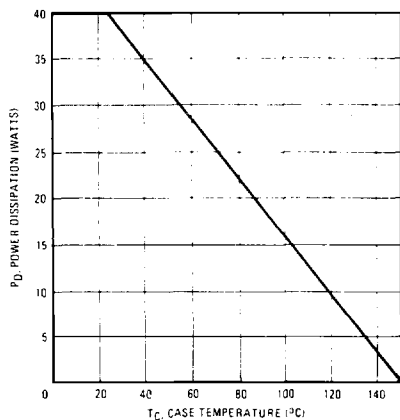


Fig. 13 - Power Vs. Temperature Derating Curve

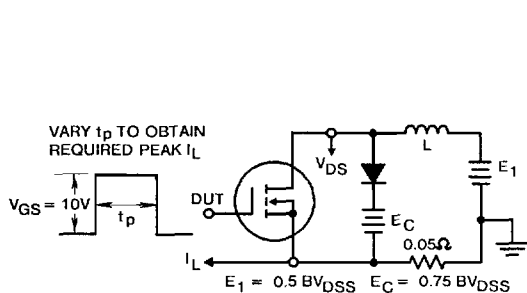


Fig. 14a - Clamped Inductive Test Circuit

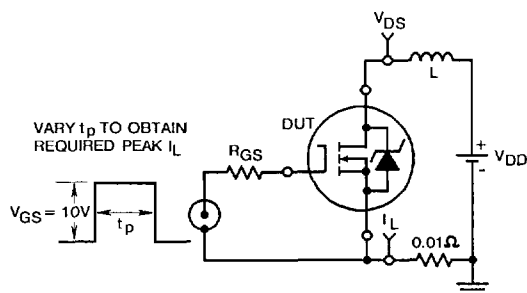


Fig. 15a - Unclamped Energy Test Circuit

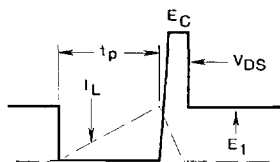


Fig. 14b - Clamped Inductive Waveforms

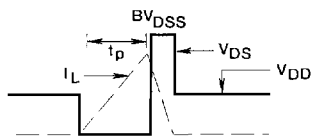


Fig. 15b - Unclamped Energy Waveforms

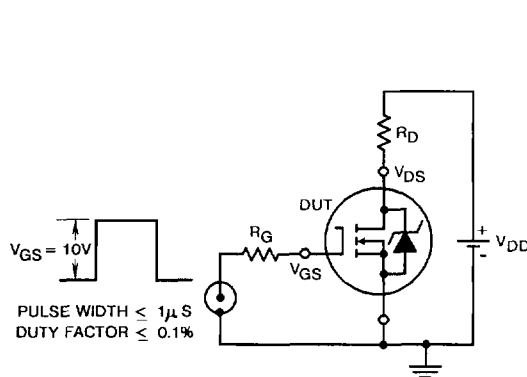


Fig. 16 - Switching Time Test Circuit

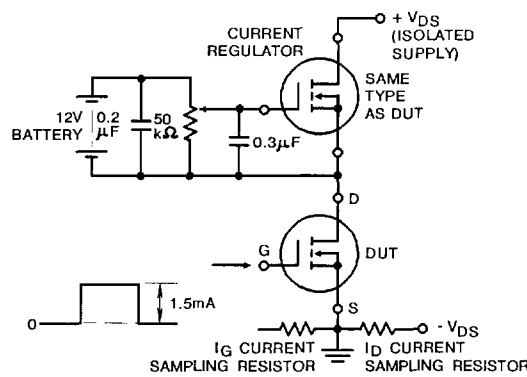


Fig. 17 - Gate Charge Test Circuit