MB87035/36
SCSI Protocol Controller (SPC)
for use with Differential or Single-end Drivers

Edition 1.0
September 1989

GENERAL DESCRIPTION

The MB87035/36 SCSI Protocol Controller (SPC) is a CMOS LSI circuit specifically designed to control a Small Computer Systems Interface (SCSI). The MB87035/36 is an enhanced version of Fujitsu's MB87030 SCSI protocol controller and is pin for pin and register compatible with the MB87030, making it upward software and hardware compatible.

To achieve optimum performance and interface flexibility, the MB87035/36 provides an 8-byte First-In First-Out (FIFO) data buffer register and a 28-bit transfer byte counter which allows burst transfers of up to 256 megabytes. To improve programming requirements, "Attention Detect" and "Arbitration Fail" interrupts are provided. Data transfers can be executed in either the asynchronous or synchronous mode with a maximum offset of 8 bytes. Separate SCSI IN and SCSI OUT ports simplify the interface to differential drivers.

SCSI Compatibility

- Supports all mandatory commands, many optional commands, and some extended commands of SCSI specification (ANSI X 3.131-1986)
- Software and pin for pin compatible with MB87030
- Serves as either INITIATOR or TARGET

Data Bus

- Independent buses for CPU and DMA controller
- Independant SCSI IN and SCSI OUT buses

Data Transfer Modes/Speed

- Asynchronous mode transfers up to 3 megabytes/sec
- Synchronous mode transfers with programmable offset of eight bytes (8-Byte FIFO) up to a maximum of 5 megabytes/sec

Selectable Operating Modes

- DMA transfer
- Program transfer
- Manual transfer
- Diagnostic

Interface

- Usable with single-ended drivers/receivers (off-chip)
- Optimized for differential drivers (off-chip)

Clock Requirements

- 10 MHz clock

Technology/Power Requirements

- Silicon-gate CMOS
- Single +5 V power supply

Enhancements (features not available with MB87030)

- Select with ATN command support
- Maximum 10 MHz operating clock
  5.0 Megabyte/Second transfer rate
- Package and pinout compatible with MB87030
  Exception: (See attachment)
- Upward software compatible with MB87030 and MB87031
- 28-bit transfer byte counter
- Data bus parity generator
- Attention condition detect interrupt
- Arbitration fail interrupt

Available Packaging

- 88-pin plastic PGA
- 100-pin Plastic Flatpack (PQFP)

ELECTRICAL CHARACTERISTICS

Permanent device damage may occur if the above absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ABSOLUTE MAXIMUM RATINGS

Rating	Designator	Values		Unit
Supply Voltage[1]	V_{DD}	V_{SS} = 0.5 to +7.0		V
Input Voltage[1]	V_I	V_{SS} −0.5 to V_{DD} +0.5		V
Output Voltage[1]	V_O	V_{SS} −0.5 to V_{DD} +0.5		V
Operating Temperature	T_{OP}	−25 to +85		°C
Storage Temperature	T_{STG}	−40 to +125		°C
Output Current[2]	I_O	V_{DD} = MAX	$V_O = V_{DD}$ +70	mA
			V_O = 0V −40	

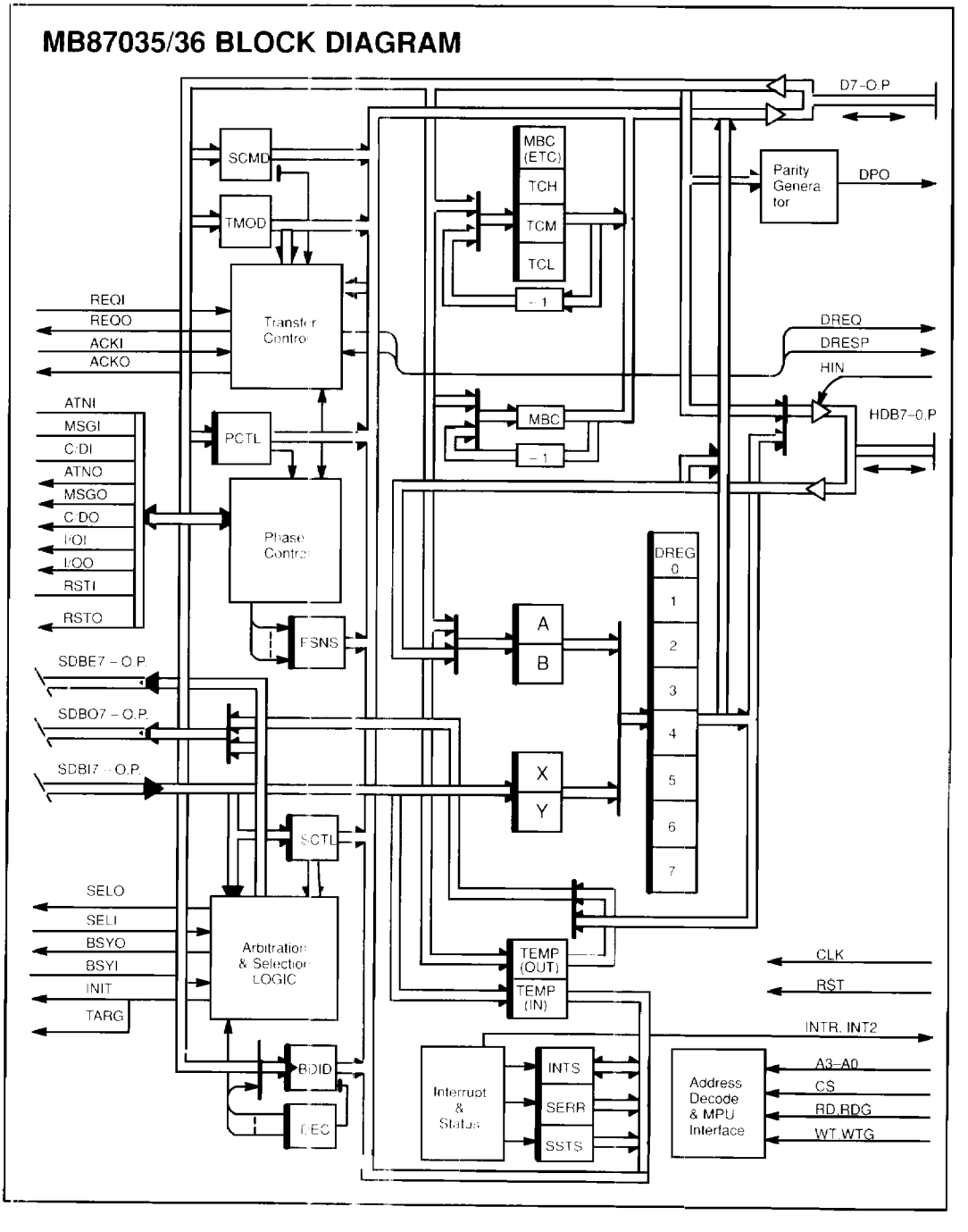
Notes: [1]V_{SS} = 0V
[2]In the case of pin 1. 1 second

RECOMMENDED OPERATING CONDITIONS

Recommended operating conditions are specified to guarantee the function of the device. Therefore, as long as the device is used within the specified limits, device reliability is guaranteed.

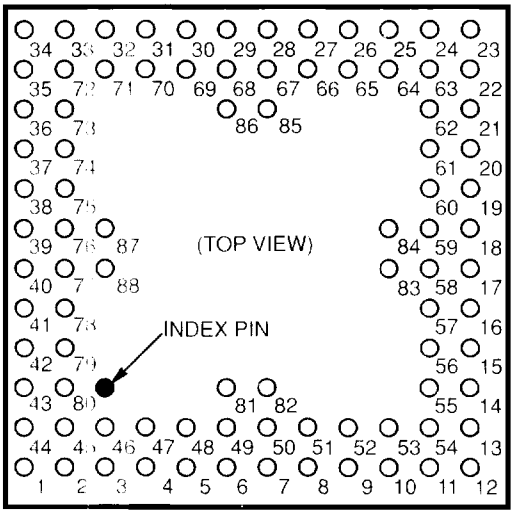
Rating	Designator	Values	Unit
Supply Voltage	V_{DD}	+5.0 ± 5%	V
Operating Ambient Temperature	T_a	0 to +70	°C
H Level Output Current	I_{OH}	Maximum −0.4	mA
L Level Output Current	I_{OL}	Maximum 3.2	mA

MB87035/36 BLOCK DIAGRAM



PIN ASSIGNMENTS

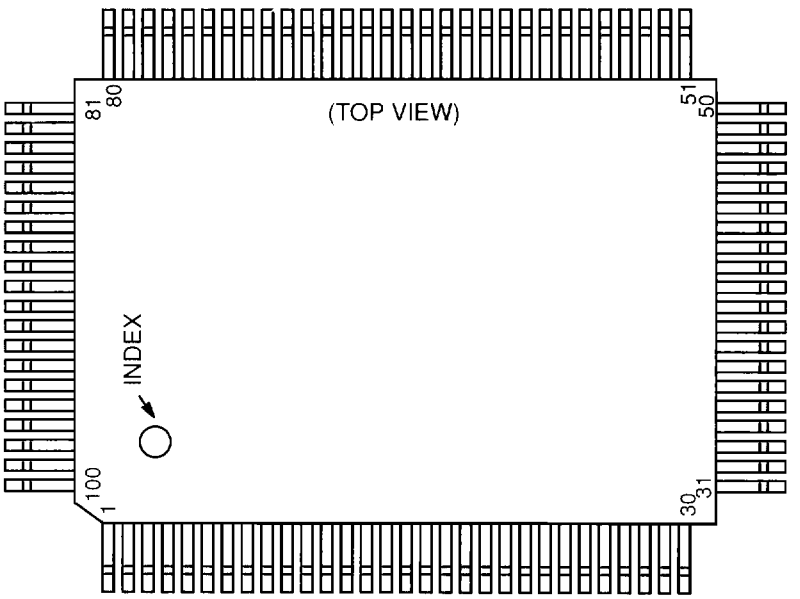
PGA–88P–M01



Pin No.	I/O	Designator	Pin No.	I/O	Designator	Pin No.	I/O	Designator	Pin No.	I/O	Designator
1	I	HIN	23	O	SDBOP	45	I	A1	67	O	SDBE5
2	I/O	HDBO0	24	O	SDBE7	46	I	A2	68	O	SDBE4
3	I/O	HDBO1	25	I	SDBI7	47	I	A3	69	I	SDBI4
4	I/O	HDBO2	26	O	SDBE6	48	I/O	D4	70	O	SDBO3
5	I/O	HDBO3	27	O	SDBO5	49	I/O	D5	71	I	SDBI2
6	I/O	HDBO4	28	I	SDBI5	50	I/O	D6	72	O	SDBO1
7	I/O	HDBO5	29	O	SDBO4	51	I/O	D7	73	O	SDBE0
8	I/O	HDBO6	30	O	SDBE3	52	I/O	DP	74	I	SDBI0
9	I/O	HDBO7	31	I	SDBI3	53	O	INTR	75	I	$\overline{RST}$
10	I/O	HDBOP	32	O	SDBO2	54	I	I/OI	76	O	DREQ
11	O	INIT	33	O	SDBE2	55	I	C/DI	77	I	$\overline{WT}$
12	O	TARG	34	I	SDBI1	56	I	SELI	78	O	DPO
13	O	I/OO	35	O	SDBE1	57	I	MSG1	79	I/O	D2
14	O	C/DO	36	O	SDBO0	58	I	REQI	80	I/O	D3
15	O	SELO	37	I	$\overline{CS}$	59	I	RSTI	81	Power Supply	V_{SS}
16	O	MSGO	38	I	CLK	60	I	ACKI	82	Power Supply	V_{DD}
17	O	REQO	39	I	$\overline{RD}$	61	I	BSYI	83	Power Supply	V_{DD}
18	O	RSTO	40	O	INT2	62	I	ATNI	84	Power Supply	V_{SS}
19	O	ACKO	41	I	DRESP	63	I	SDBIP	85	Power Supply	V_{SS}
20	O	BSYO	42	I/O	D0	64	O	SDBO7	86	Power Supply	V_{DD}
21	O	ATNO	43	I/O	D1	65	O	SDBO6	87	Power Supply	V_{DD}
22	O	SDBEP	44	I	A0	66	I	SDBI6	88	Power Supply	V_{SS}

PIN ASSIGNMENTS

100-Pin Plastic Quad Flatpack (PQFP)



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PIN ASSIGNMENTS
100-Pin Plastic Quad Flatpack (PQFP)

Pin No.	I/O	Designator	Pin No.	I/O	Designator	Pin No.	I/O	Designator	Pin No.	I/O	Designator
1	I	DRESP	26	I/O	D2	51	O	TARG	76	O	SDBE5
2	O	DREQ	27	I/O	D3	52	O	INIT	77	O	SDBO5
3	Power Supply	V_{DD}	28	Power Supply	V_{DD}	53	Power Supply	V_{DD}	78	Power Supply	V_{DD}
4	Power Supply	V_{SS}	29	Power Supply	V_{SS}	54	Power Supply	V_{SS}	79	Power Supply	V_{SS}
5	I	HIN	30	I/O	D4	55	I	ACKI	80	—	NC
6	I/O	HDB0	31	I/O	D5	56	O	ACKO	81	I	SDBI4
7	I/O	HDB1	32	I/O	D6	57	—	NC	82	O	SDBE4
8	I/O	HDB2	33	I/O	D7	58	—	NC	83	O	SDBO4
9	I/O	HDB3	34	I/O	DP	59	I	BSYI	84	I	SDBI3
10	I/O	HDB4	35	I	A0	60	O	BSYO	85	O	SDBE3
11	I/O	HDB5	36	I	A1	61	I	ATNI	86	O	SDBO3
12	I/O	HDB6	37	I	A2	62	O	ATNO	87	I	SDBI2
13	I/O	HDB7	38	I	A3	63	I	RSTI	88	O	SDBE2
14	I/O	HDBP	39	I	$\overline{RST}$	64	O	RSTO	89	O	SDBO2
15	Power Supply	V_{SS}	40	Power Supply	V_{SS}	65	Power Supply	V_{SS}	90	Power Supply	V_{SS}
16	I	$\overline{CLK}$	41	I	REQI	66	I	SDBIP	91	I	SDBI1
17	I	$\overline{CS}$	42	O	REQO	67	O	SDBEP	92	O	SDBE1
18	I	$\overline{WT}$	43	I	I/OI	68	O	SDBOP	93	O	SDBO1
19	O	DPO	44	O	I/OO	69	I	SDBI7	94	I	SDBI0
20	I	$\overline{RD}$	45	I	C/DI	70	O	SDBE7	95	O	SDBE0
21	O	INT2	46	O	C/DO	71	O	SDBO7	96	O	SDBO0
22	O	INTR	47	I	SELI	72	I	SDBI6	97	—	NC
23	—	NC	48	O	SELO	73	O	SDBE6	98	—	NC
24	I/O	D0	49	I	MSGI	74	O	SDBO6	99	—	NC
25	I/O	D1	50	O	MSGO	75	I	SDBI5	100	—	NC

PIN DESCRIPTIONS

Pin No. MB87035 PGA	Pin No. MB87036 QFP	Designator	Function
1	5	HIN	Indicates direction of transmission along data bus lines HDB0–HDB7 and HDBP in the DMA transfer mode. For transmission to be executed, direction of transmission must be properly coordinated with internal operation of the SPC. When HIN is low, the data bus lines are placed in the high-impedance state (input mode). When HIN is high, all bus lines are switched to the output mode.
2–9 10	6–13 14	HDB0–HDB7 HDBP	3 state bidirectional data bus for transferring data to or from the external buffer memory in the DMA mode. As shown below, the direction of data transmission dlepends on the HIN input signal. HIN — HDBn — Operation L — Input Mode — Output H — Output Mode — Input
11 12	52 51	INIT TARG	These two signals indicate operating state of SPC; they are also available as control signals for the SCSI driver/receiver circuits. Initiator — Target — Status L — L — SPC is not connected to SCSI. L — H — SPC is executing RESELECTION phase or is operating as a TARGET. H — L — SPC is executing SELECTION phase or is operating as an INITIATOR.
13 14 15 16 17 18 19 20 21	44 46 48 50 42 64 56 60 62	I/OO C/DO SELO MSGO REQO RSTO ACKO BSYO ATNO	Used to output SCSI control signals. REQO, MSGO, C/DO, and I/OO are active high only when the SPC serves as a TARGET. ACKO and ATNO are active high only when the SPC serves as an INITIATOR.
22 24 26 67 68 30 33 35 73	67 70 73 76 82 85 88 92 95	SDBEP SDBE7 SDBE6 SDBE5 SDBE4 SDBE3 SDBE2 SDBE1 SDBE0	Drive enable signals (corresponding to respective bit positions) when a 3 state buffer is used for the SCSI data bus. SDBE7-SDBE0 and SDBEP correspond to SDBO7–SDBO0 and SDBOP, respectively. Relationships with respect to the SCSI bus are shown below.

SCSI BUS STATUS	SDBOn		SDBEn	
	ID[1]	$\overline{ID}$	ID	$\overline{ID}$
Bus Free	L	L	L	L
Arbitration	H	L	H	L
Selection/Reselection	D[2]	D[2]	H	H
Information Transfer				
SPC → SCSI	D[2]	D[2]	H	H
SCSI → SPC	L	L	L	L

Notes: [1]D indicates bit positions corresponding to the SCSI bus device ID; $\overline{ID}$ indicates the other bit position.
[2]D indicates transfer of valid information.

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PIN DESCRIPTIONS

Pin No. MB87035 PGA	Pin No. MB87036 QFP	Designator	Function
25	69	SDBI7	Inputs for the SCSI data bus; most significant bit (MSB) is SDBI7; least significant bit (LSB) is SDBI0. SDBIP is an odd parity bit; parity checking for the SCSI data bus is programmable.
66	72	SDBI6	
28	75	SDBI5	
69	81	SDBI4	
31	84	SDBI3	
71	87	SDBI2	
34	91	SDBI1	
74	94	SDBI0	
63	66	SDBIP	
64	71	SDBO7	Outputs for the SCSI data bus; most significant bit (MSB) is SDBO7; least significant bit (LSB) is SDBO0. SDBOP is an odd parity bit. If the bus driver is an open collector device, these signals should be applied directly to the driver circuit. If the bus driver is a 3-state device, these signals are used as data and SDBO7–SDBO0 and SDBOP are used as drive-enable signals.
65	74	SDBO6	
27	77	SDBO5	
29	83	SDBO4	
70	86	SDBO3	
32	89	SDBO2	
72	93	SDBO1	
36	96	SDBO0	
23	68	SDBOP	
37	17	$\overline{CS}$	Selection enable signal for accessing an internal register in SPC. When $\overline{CS}$ is active, input/output signals $\overline{RD}$, $\overline{WT}$, A0–A3, D0–D7, and DP are active.
38	16	CLK	Input clock for controlling internal operation and data transfer speed of SPC.
39	20	$\overline{RD}$	Input strobes used for reading out contents of internal register; strobes are effective only when $\overline{CS}$ is active low. For a data transfer cycle in the program transfer mode, the trailing edge of $\overline{RD}$ is used as a timing signal to indicate the end of data read.
41	1	DRESP	During a data transfer cycle in the DMA mode, DRESP is a response signal to the data transfer request signal DREQ. The DRESP pin must be refreshed with an applied pulse after each byte of data is transferred. In output operations, the falling edge of DRESP is used for sampling data on HDB0-HDB7 and HDBP bus lines; in input operations, the SPC holds data to be transferred onto HDB0-HDB7 and HDBP until the falling edge of DRESP occurs.
51	33	D7	Used for writing or reading data from or to an internal register in SPC; these bus lines are 3-state and bidirectional. The most significant bit (MSB) is D7; the least significant bit (LSB) is D0. DP is an odd parity bit. When the $\overline{CS}$ and $\overline{RD}$ inputs are active Low, contents of the internal register are output to the data bus (read operation). In operations other than read, these bus lines are kept in a hgh-impedance state
50	32	D6	
49	31	D5	
48	30	D4	
80	27	D3	
79	26	D2	
43	25	D1	
42	24	D0	
52	34	DP	

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PIN DESCRIPTIONS

Pin No. MB87035 PGA	Pin No. MB87036 QFP	Designator	Function
44–47	35–38	A0–A3	Address input signals for selecting an internal register in the SPC. The MSB is A3; the LSB is A0. When $\overline{CS}$ is active low, read/write is enabled and an internal register is selected by these address inputs via data bus lines D0-D7 and DP.
53	22	INTR	Requests an interrupt to indicate completion of an SPC internal operation or the occurrence of an error. Interrupt masking is allowed except for an interrupt caused by the RSTI input (reset condition of SCSI). When an interrupt is permitted, the INTR signal remains active until the interrupt is cleared.
56 61 58 60 57 55 54 62 59	47 59 41 55 49 45 43 61 63	SELI BSYI REQI ACKI MSGI CDI I/OI ATNI RSTI	Used for receiving SCSI control signals; outputs of the SCSI receiver can be directly connected. (Waveform distortion or any other disturbance should not occur in the REQI and ACKI signals which are used as timing control signals for sequencing data transfers.)
76	2	DREQ	When executing a data transfer cycle in the DMA mode, DREQ is used to indicate a request for data transfer between the SPC and external buffer memory. In the DMA mode, routing of data is as shown below. Output Operations: From external buffer memory to HDB0-HDB7/HDBP to SPC internal data buffer register (8 Bytes) to SDBO0-SDBO7/SDBOP to SCSI. Input Operations: From SCSI to SDBI9-SDBI7/SDBIP to SPC internal data buffer register (8 bytes) to HDB0-HDB7/HDBP to external buffer memory. In an output operation, DREQ becomes active to request a data transfer from the external buffer memory when the SPC internal data buffer register has free space available. In an input operation, DREQ becomes active to request a data transfer to the external buffer memory when the SPC internal buffer memory contains valid data.

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PIN DESCRIPTIONS

Pin No. MB87035 PGA	Pin No. MB87036 QFP	Designator	Function
77	18	$\overline{WT}$	Input strobe used for writing data into an SPC internal register; this signal is asserted only when $\overline{CS}$ is active low. On the trailing edge of $\overline{WT}$, data placed on data bus lines D0-D7/DP is loaded into the internal register selected by address inputs A0-A3, except when all address lines are high (A0-A3 = H). For a data transfer cycle in the program transfer mode, the trailing edge of $\overline{WT}$ is used as a timing signal to indicate a data-ready state.
78	19	DPO	An odd parity output for data byte D7-D0, DPO represents an output when D7-D0/DP are placed in a high-impendance state; DPO is in a high-impedance state when D7-D0/DP serve as outputs. If a parity bit is not genetrated for external memory. DPO can be used as an input for DP.
81, 84 85, 88	4, 29, 54, 79 15, 40 65, 90	V_{SS}	Power supply ground, (0 V).
82. 83 86, 87	3, 28, 53, 78	V_{DD}	+5 V Power Supply.
40	21	INT2	The INT2 output is a non-maskable interrupt request that, when driven High, notifies the SPC when a reset condition is detected on the SCSI bus.
—	23, 57 58, 80 97, 98 99, 100	NC	No connects.

ADDRESSING OF INTERNAL REGISTERS

The MB87035/36 contains 16 byte-wide registers that are externally accessible. These registers are used to control internal operations of the SPC and also to indicate processing/result status. A unique address, identified by address bits A3-A0, is assigned to each of the sixteen registers. These addresses are defined in Table 1. (Note: The phase sense (PSNS) and SPC diagnostic (SDGC) registers have the same hexadecimal address; however, depending upon whether a read or write command is executed, the registers provide two separate functions.)

Table 1. Internal Register Addressing

Register	Mnemonic	Operation	Chip Select (CS)	Address Bits A3	A2	A1	A0
Bus Device ID	BDID	R	0	0	0	0	0
		W					
SPC Control	SCTL	R	0	0	0	0	1
		W					
Command	SCMD	R	0	0	0	1	0
		W					
Transfer Mode	TMOD	R	0	0	0	1	1
		W					
Interrupt Sense	INTS	R	0	0	1	0	0
Reset Interrupt		W					
Phase Sense	PSNS	R	0	0	1	0	1
SPC Diagnostic Control	SDGC	W					
SPC Status	SSTS	R	0	0	1	1	0
—		W					
SPC Error Status	SERR	R	0	0	1	1	1
—		W					
Phase Control	PCTL	R	0	1	0	0	0
		W					
Modified Byte Counter	MBC	R	0	1	0	0	1
Extended Transfer Count		W					

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Table 1. Internal Register Addressing

Register	Mnemonic	Operation	Chip Select ($\overline{CS}$)	Address Bits A3	A2	A1	A0
Data Register	DREG	R	0	1	0	1	0
		W					
Temporary Register	TEMP	R	0	1	0	1	1
		W					
Transfer Counter High	TCH	R	0	1	1	0	0
		W					
Transfer Counter Middle	TCM	R	0	1	1	0	1
		W					
Transfer Counter Low	TCL	R	0	1	1	1	0
		W					
External Buffer	EXBF	R	0	1	1	1	1
		W					

BIT ASSIGNMENTS FOR INTERNAL REGISTERS

Table 2 lists the bit assignments for the sixteen internal registers defined in Table 1. In most cases, bit assignments for the MB87035/36 SPCs are identical to those for the MB87030; however, in the MB87035/36, some features are expanded and others are added to improve overall performance. These modifications and additions are summarized as follows:

Table 2. Bit Assignments For Internal Registers

HEX Address	Register and Mnemonic	R/W Operation	7 (MSb)	6	5	4	3	2	1	0 (LSb)	Parity
0	Bus Device ID (BDID)	R	#7	#6	#5	#4	#3	#2	#1	#0	0
		W						SCSI Bus Device ID ID4	ID2	ID1	—
1	SPC Control (SCTL)	R	Reset & Disable	Control Reset	Diag Mode	ARBIT Enable	Parity Enable	Select Enable	Reselect Enable	INT Enable	P
		W									
2	Command (SCMD)	R	Command Code			RST Out	Intercept Xfer	Transfer Modifer PRG Xfer	0	Term Mode	P
		W									
3	Transfer Mode (TMOD)	R	Sync Xfer	Max. Transfer Offset 4	2	1	Min. Transfer Offset 2	1	0	Xfer Counter Expand	P
		W									
4	Interrupt Sense (INTS)	R	Selected	Reselected	Disconnect	Command Complete	Service Required	Time Out	SPC Hard Error	Reset Condition	P
		W	Reset Interrupt								—
5	Phase Sense (PSNS)	R	REQ	ACK	ATN	SEL	BSY	MSG	C/D	I/O	P
	SPC Diag Control (SDGC)	W	Diag. REQ	Diag. ACK	—	—	Diag. BSY	Diag. MSG	Diag. C/D	Diag. I/O	—
6	SPC Status (SSTS)	R	Connected INIT	TARG	SPC BSY	Xfer In Progress	SCSI RST	TC=0	DREG Status Full	Empty	P
7	SPC Error Status (SERR)	R	Data Error SCSI	SPC	0	0	TC Parity Error	Phase Error	Short Xfer Period	Offset Error	P

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Table 2. Bit Assignments For Internal Registers

HEX Address	Register and Mnemonic	R/W Operation	7 (MSb)	6	5	4	3	2	1	0 (LSb)	Parity
8	Phase Control (PCTL)	R	Bus Free Interrupt Enable	Arbitration Fail Interrupt Enable	Attention Condition Interrupt Enable	Reset Condition Interrupt mask	0	Transfer Phase			P
		W						MSG Out	C/D Out	I/O Out	
9	Modified Byte Counter (MBC)	R	Extended Transfer Counter				MBC				P
			Bit 27	Bit 26	Bit 25	Bit 24	Bit 3	Bit 2	Bit 1	Bit 0	
A	Data Register (DREG)	R	Internal Data Register (8 Byte FIFO)								
		W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	P
B	Temporary Register (TEMP)	R	Temporary Data (Input: From SCSI)								
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	P
		W	Temporary Data (Output: To SCSI)								
			Bit 7	Bit 6	Bit 5		Bit 3	Bit 2	Bit 1	Bit 0	P
C	Transfer Counter High (TCH)	R	Transfer Counter High (MSB)								
		W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	P
D	Transfer Counter Middle (TCM)	R	Transfer Counter Middle (2nd Byte)								
		W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	P
E	Transfer Counter LOW (TCL)	R	Transfer Counter Low (LSB)								
		W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	P
E	External Buffer (EXBF)	R	External Buffer								
		W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	P

MPU Bus Parity Generator

An odd parity bit is output from DPO for each data byte (D7-D0). DPO is a 3-state pin and is placed in a high-impedance state when data from D7-D0 is output to the MPU. If the MPU interface does not contain a parity generator, the output of DPO can be connected to the DP input pin of the SPC.

Reset Condition Interrupt Request Signal

The INT2 output is a non-maskable interrupt request that, when driven High, notifies the SPC when a reset condition is detected on the SCSI bus. Bit 4 (Reset Condition Interrupt Mask Enable) of the Phase Control (PCTL) register does not affect the INT2 output pin.

When a bus reset condition is detected the INTR output also is driven to the high state; however, the state of INTR can be masked by bit 4 of the PCTL register:

Bit 4 = 0: INTR goes high when a reset condition is detected.

Bit 4 = 1: INTR does not go high when a reset condition is detected.

Lost Arbitration Interrupt Request

If bit 6 (Lost Arbitration Interrupt Enable) of the phase control (PCTL) register is set to "1", a COMMAND COMPLETE interrupt is generated when the SPC (serving as initiator or target) loses in the ARBITRATION process. To determine the cause of a COMMAND COMPLETE interrupt (completion of SELECTION, RESELECTION, or lost ARBITRATION), refer to bits 6 (TARGET) and 7 (INITIATOR) of the SPC status (SSTS) register. If both bits are set to "0", the COMMAND COMPLETE interrupt is a result of lost arbitration.

Attention Condition Interrupt

If bit 5 (Attention Condition Interrupt Enable) of the phase control (PCTL) register is set to "1" and the SPC serves as a target, a service required interrupt occurs. To reset the service required interrupt, set bit 3 of the interrupt sense (INTS) register to "1" or revoke the current target role of the SPC.

Expansion of Transfer Byte Counter

If bit 0 of the transfer mode (TMOD) register is set to "1", the transfer byte counter is expanded to 28 bits. In the expanded mode, the high nibble (bits 24 through 27) are entered into the four most significant bit positions (7 bits through 4) of the modified byte count (MBC) register.

Note: *When a hardware data transfer or execution of a SELECT command is in process, access to the TMOD register is forbidden.*

Bit 0 of the TMOD register =1

To access the highest four bits (bits 24 through 27) of the transfer byte counter, data reads or writes are addressed to the high nibble of the modified byte counter (MBC) register. When a TRANSFER or SELECT command is issued, the transfer byte count (or t_{WAIT}) should be placed in the high nibble of the MBC register rather than the TCH, TCM, and TCL registers.

Bit 0 of the TMOD register = 0

The transfer byte counter is not expanded to 28 bits; hence, reading the high nibble of MBC yields a "0" even though some particular value is written into the register. In this case, t_{WAIT} or the transfer byte count is based on a 24-bit transfer byte counter (identical to the MB87030).

During read/write access of an internal register, the following rules are invoked:

(1) Internal registers include only those registers identified in Table 2.
(2) A write command to a read–only register is ignored.
(3) For write operations, all bit positions with a "—" (blank) designator can be written as "0" or as a "1".
(4) All bit positions with an assigned "0" are always read as a zero (0).

Select with ATN Command

- *Initiation:*
  Writing 21H to the SCMD register with the PCTL register's bit 0 (I/O Out) = "0". (When the PCTL register's Bit 0 = "1", the Select command is initiated.)
- *Ignore:*
  The Select with ATN command is ignored (no operation) when MB87035/36 has already been connected with the SCSI bus or when the MB87035/36 is executing the connecting sequence.
- *Cancellation:*
  The Select with ATN command is cancelled in the following cases:
  1. When terminating the selection by time-out.
  2. When failing in arbitration.
  3. When Bus Release command is issued.
  4. When selected by another device.

  Note: *A combination of the Set ATN command and the Select command can also be used.*

DC CHARACTERISTICS

DC characteristics of input and output buffers are guaranteed to the worst case value over the recommended range of operating conditions.

V_{DD} = 5 V ± 5%. V_{SS} = 0 V. T_a = 0 to 70°C

Parameter	Designator	Conditions	Values			Unit
			Minimum	Typical	Maximum	
Supply Voltage	I_{DDS}	Static	—	—	0.1	mA
Output High Voltage	V_{OH}	I_{OH} = -0.4 mA	4.2	—	V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 3.2 mA	V_{SS}	—	0.4	V
Input High Voltage	V_{IH}	TTL Level	2.2	—	V_{DD} +0.5	V
		CMOS Level	V_{DD} x 0.7	—	—	V
Input Low Voltage	V_{IL}	TTL Level	—	—	0.8	V
		CMOS Level	—	—	V_{DD} x 0.3	V
Input Leakage current (during tristate pin input)	I_{LI}	V_I = 0V to V_{DD}	-10	—	10	mA
	I_{LZ}		-10	—	10	mA

INPUT/OUTPUT PIN CAPACITANCE

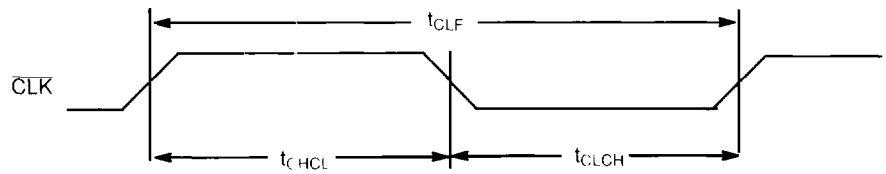
Parameter	Designator	Values	Unit
Input Pin	C_{IN}	9	pF
Output Pin	C_{OUT}	9	pF
Input/Output Pin	$C_{I/O}$	11	pF

Measurement conditions: T_a = 25°C V_{DD} = V_I = 0 V, f = 1 MHz

AC CHARACTERISTICS

Clock Timing

Parameter	Designator	Values		Unit
		Min.	Max.	
Clock Cycle	t_{CLF}	125	200	ns
Clock High Time	t_{CHCL}	50	—	ns
Clock Low Time	t_{CLCH}	40	—	ns



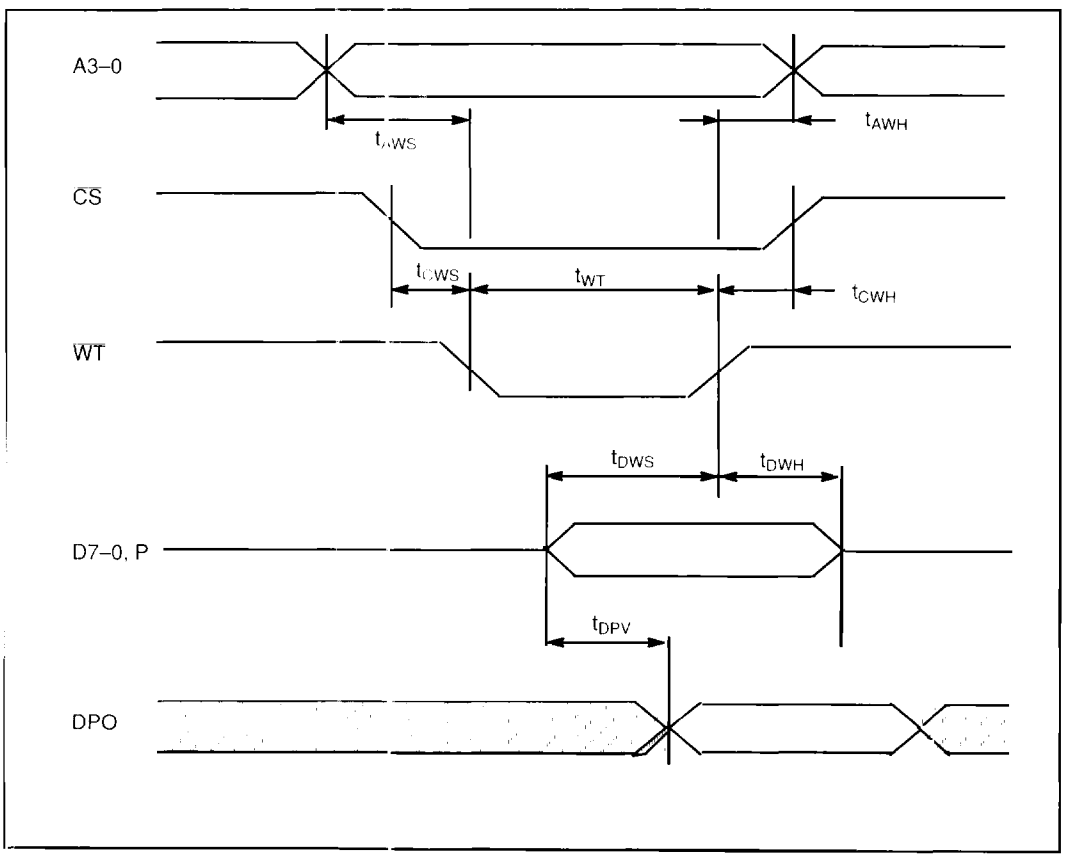
Hardware Reset

Parameter	Designator	Values		Unit
		Min.	Max.	
Reset Pulse Width	t_{RSTW}	50	—	ns

AC CHARACTERISTICS

Register Write (excluding EXBF register)

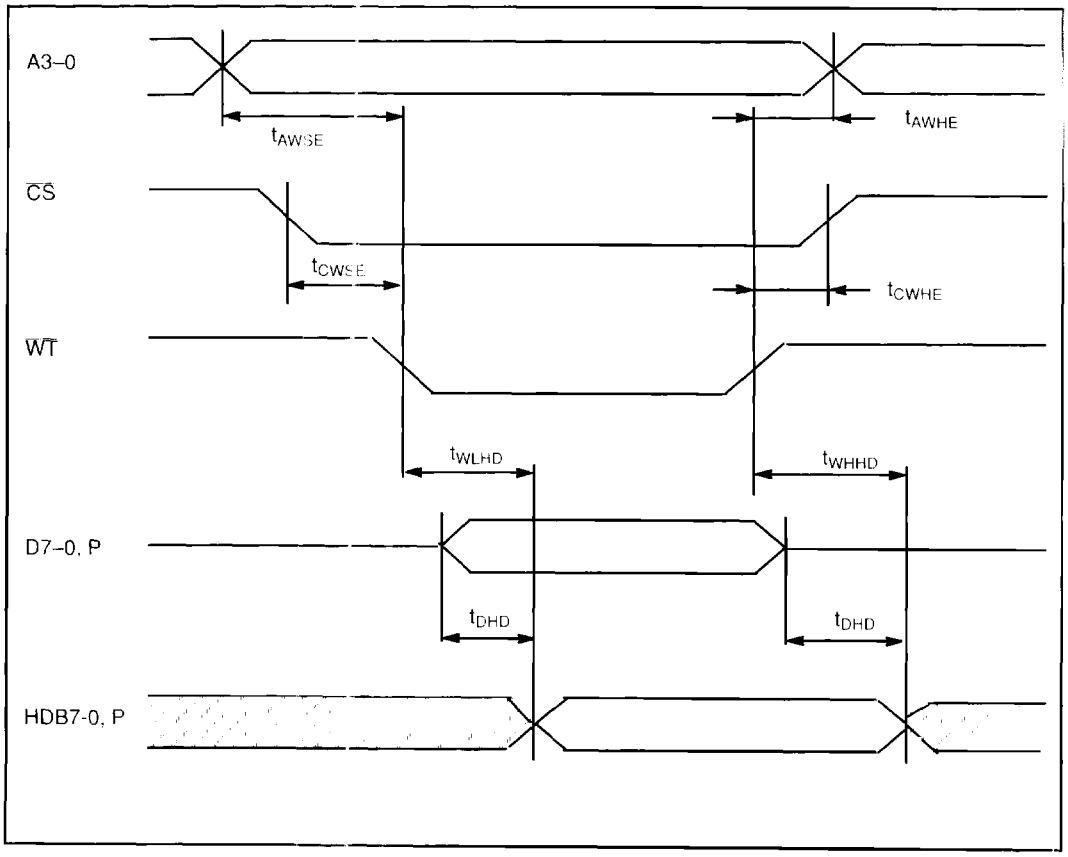
Parameter	Designator	Values		Unit
		Min.	Max.	
Address Setup	t_{AWS}	35	—	ns
Address Hold	t_{AWH}	5	—	ns
CS Setup	t_{CWS}	20	—	ns
CS Hold	t_{CWH}	10	—	ns
Data Bus Setup	t_{DWS}	25	—	ns
Data Bus Hold	t_{DWH}	15	—	ns
Write Pulse Width	t_{WT}	50	—	ns
Data Bus Valid to DPO Valid	t_{DPV}	—	55	ns



AC CHARACTERISTICS

EXBF Register Write

Parameter	Designator	Values		Unit
		Min.	Max.	
Address Setup	t_{AWSE}	35	—	ns
Address Hold	t_{AWHE}	5	—	ns
$\overline{CS}$ Setup	t_{CWSE}	20	—	ns
$\overline{CS}$ Hold	t_{CWHE}	10	—	ns
$\overline{WT}$ "L" to DMA bus output valid	t_{WLHD}	—	55	ns
$\overline{WT}$ "H" to DMA bus output valid	t_{WHHD}	10	—	ns
MPU data bus to DMA bus delay	t_{DHD}	—	50	ns

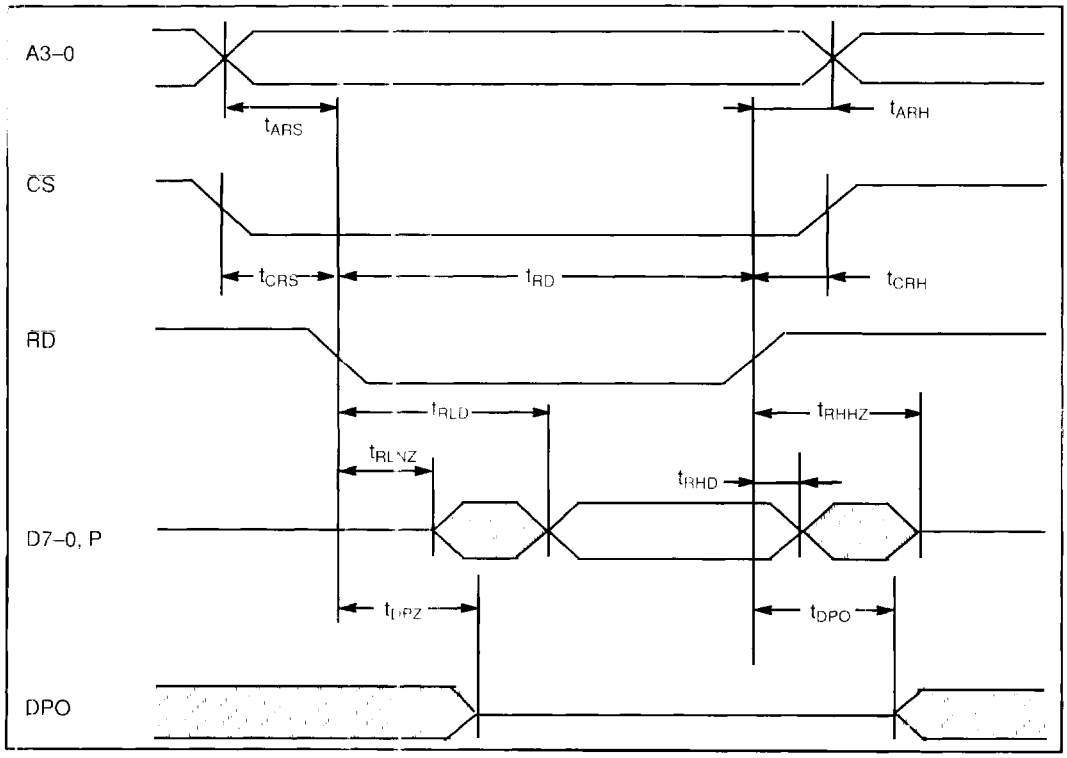


AC CHARACTERISTICS

Register Read (excluding EXBF register)

Parameter		Designator	Values		Unit
			Min.	Max.	
Address Setup		t_{ARS}	35	—	ns
Address Hold		t_{ARH}	5	—	ns
$\overline{CS}$ Setup		t_{CRS}	20	—	ns
$\overline{CS}$ Hold		t_{CRH}	10	—	ns
$\overline{RD}$ "L" to data bus output		t_{RLNZ}	10	40	ns
$\overline{RD}$ "H" to data bus high Z		t_{RHHZ}	10	40	ns
$\overline{RD}$ "L" to data valid	D7 to D0	t_{RLD}	—	70	ns
	DP		—	85	ns
$\overline{RD}$ "H" to data invalid		t_{RHD}	10	—	ns
$\overline{RD}$ pulse width		t_{RD}	50	—	ns
$\overline{RD}$ "L" to DPO high Z*		t_{DPZ}	10	40	ns
$\overline{RD}$ "H" to DPO output		t_{DPO}	10	40	ns

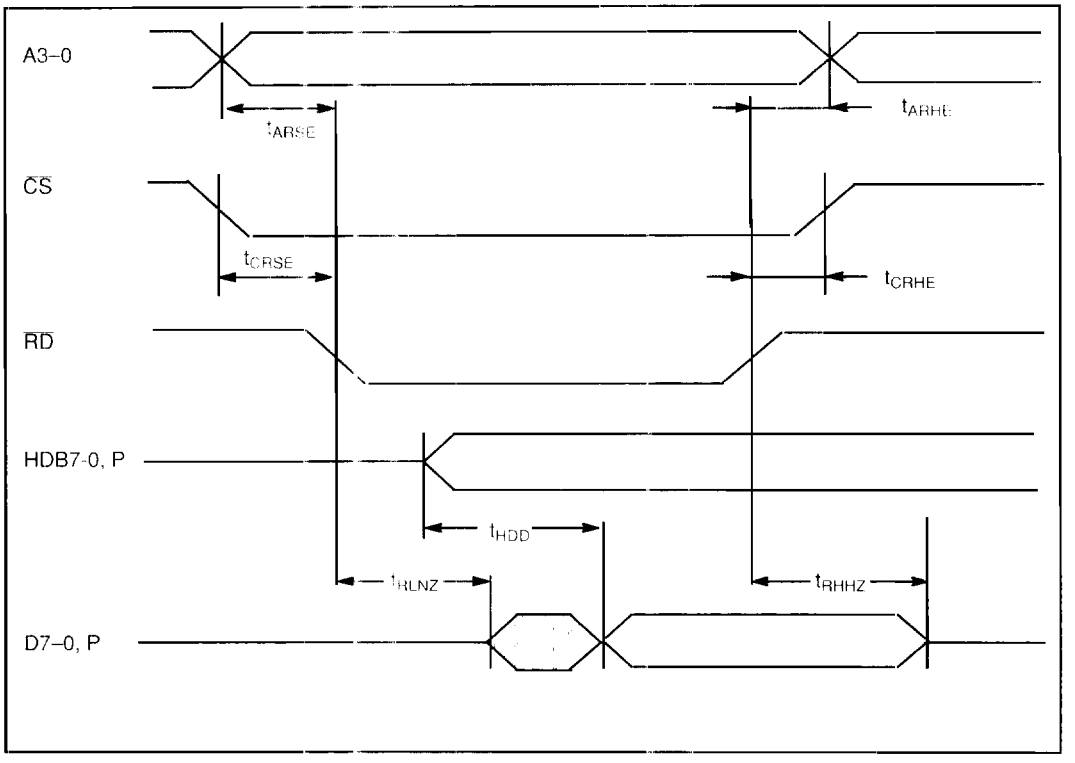
*DPO becomes High Z when both $\overline{RD}$ and $\overline{CS}$ are "L"



AC CHARACTERISTICS

EXBF Register Read

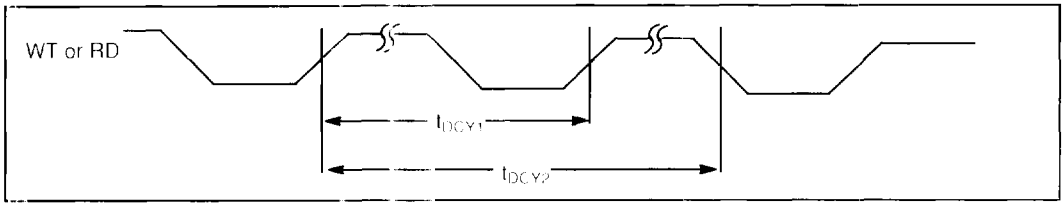
Parameter	Designator	Values		Unit
		Min.	Max.	
Address Setup	t_{ARSE}	35	—	ns
Address Hold	t_{ARHE}	5	—	ns
$\overline{CS}$ Setup	t_{CRSE}	20	—	ns
$\overline{CS}$ Hold	t_{CRHE}	10	—	ns
$\overline{RD}$ "L" to data bus output	t_{RLNZ}	10	40	ns
$\overline{RD}$ "H" to data bus high Z	t_{RHHZ}	10	40	ns
DMA bus to MPU data bus delay	t_{HDD}	—	50	ns



AC CHARACTERISTICS

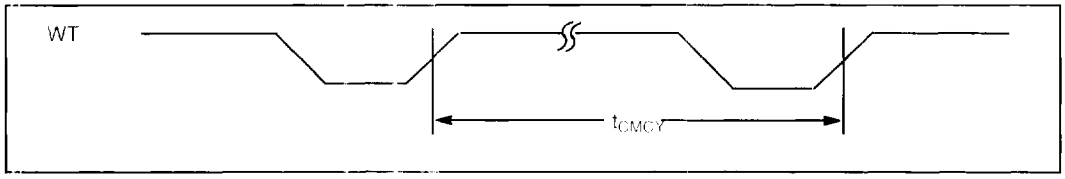
DREG Access Cycle Time

Parameter	Designator	Values		Unit
		Min.	Max.	
DREG access cycle time 1	t_{DCY1}	$2t_{CLF}$		ns
DREG access cycle time 2	t_{DCY2}	$3t_{CLF}$		ns



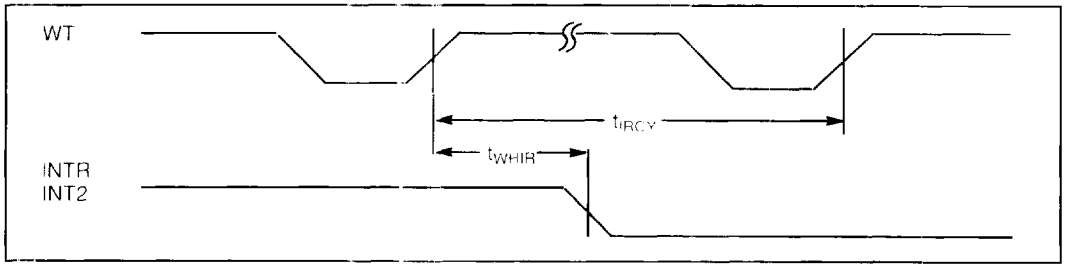
Command Issue Cycle Time

Parameter	Designator	Values		Unit
		Min.	Max.	
SCMD register write cycle	t_{CMCY}	$4t_{CLF}$		ns



Interrupt REset

Parameter	Designator	Values		Unit
		Min.	Max.	
WT "H" to interrupt signal "L"	t_{WHIR}	t_{CLF}	$3t_{CLF}$ +80	ns
INTS register write cycle	t_{IRCY}	$4t_{CLF}$		ns

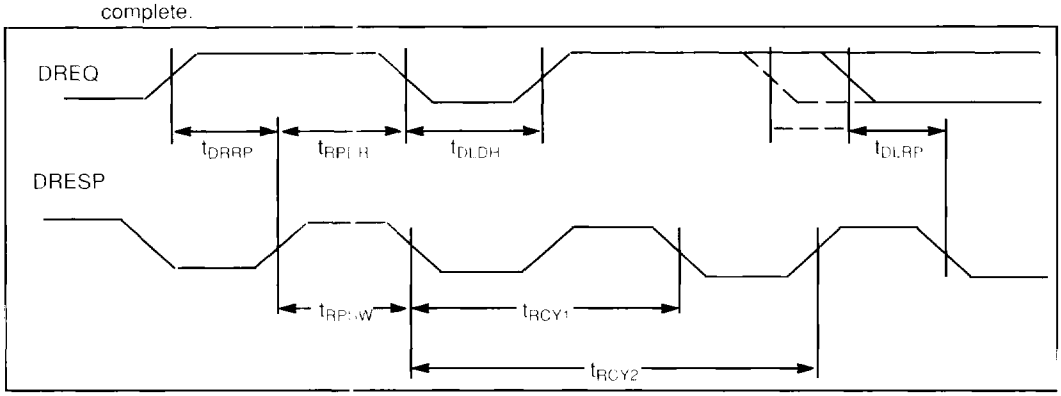


AC CHARACTERISTICS

DMA Access Timing

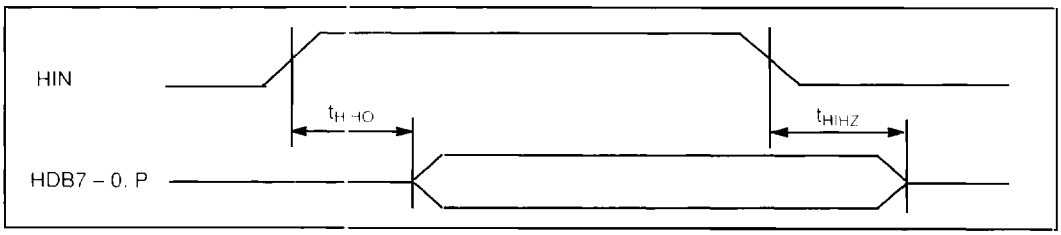
Parameter	Designator	Values		Unit
		Min.	Max.	
DREQ "H" to DRESP "H"	t_{DHRP}	t_{CLF}		ns
DRESP "H" to DREQ "L"	t_{RPDR}	5	70	ns
DREQ "L" to DREQ "H"	t_{DLDH}	0		ns
DRESP pulse width	t_{RPSW}	50		ns
DRESP cycle time 1	t_{RCY1}	$2t_{CLF}$		ns
DRESP cycle time 2	t_{RCY2}	$3t_{CLF}$		ns
DREQ "L" to DRESP "L"	t_{DLRP}		$5t_{CLF}$	ns

Notes: Utilized when using data buffer storage function and/or using transfer pause command. In these cases, if DREQ and DRESP do not become "L" simultaneously, the response to DREQ is undetermined. Also, write to data buffer will not be performed correctly unless t_{DLRP} and t_{RPSW} are complete.



DMA Bus Output Control

Parameter	Designator	Values		Unit
		Min.	Max.	
HIN "H" to DMA bus output	t_{HIHO}	5	40	ns
HIN "L" to DMA bus high Z	t_{HIHZ}	5	40	ns

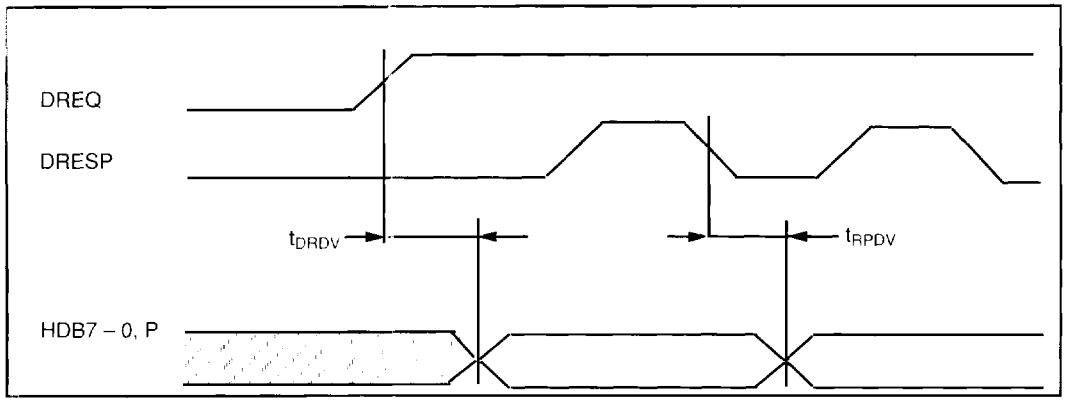


AC CHARACTERISTICS

DMA Transfer: Data Received from SCSI

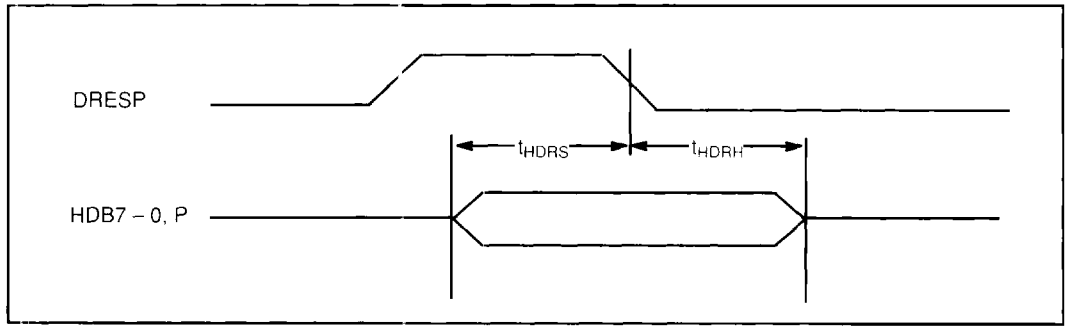
Parameter	Designator	Values		Unit
		Min.	Max.	
DREQ "H" to data output valid*	t_{DRDV}	—	60	ns
DRESP "L" to data switch	t_{RPDV}	15	90	ns

*Utilized when internal data buffer is changed from Not Empty to Empty.



DMA Transfer: Sending Data to SCSI

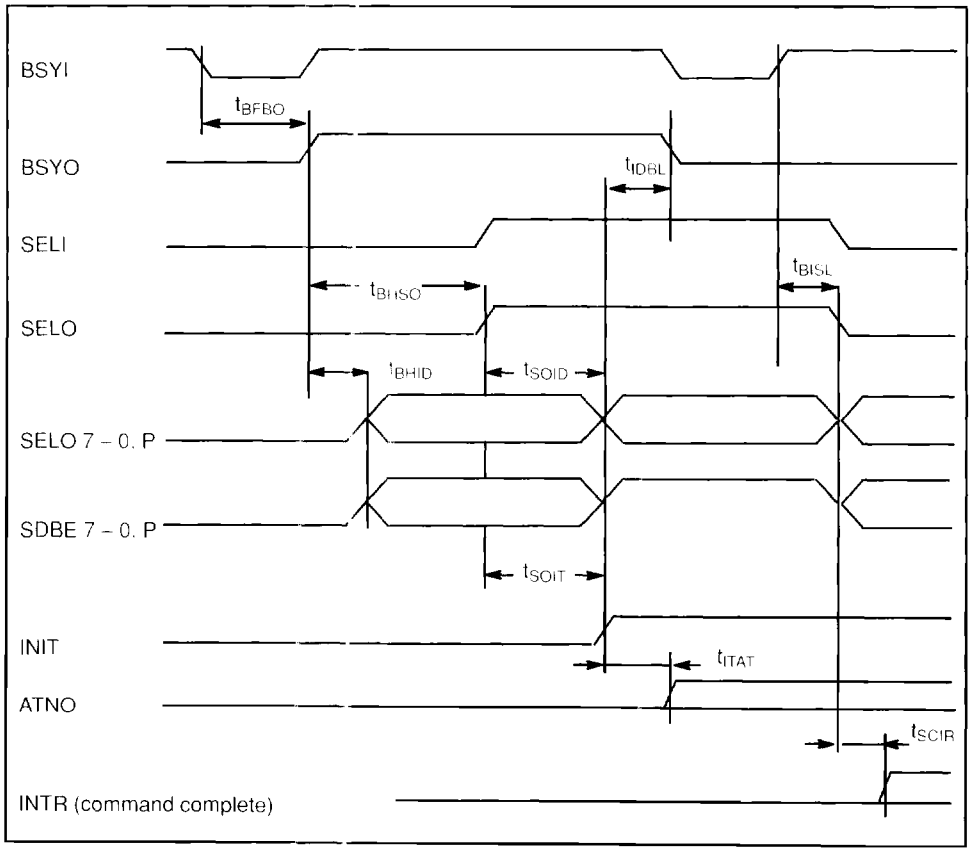
Parameter	Designator	Values		Unit
		Min.	Max.	
Input data setup	t_{HDRS}	20	—	ns
Input data hold	t_{HDRH}	15	—	ns



AC CHARACTERISTICS

Selection: Initiator (including arbitration)				
Parameter	Designator	Values		Unit
		Min.	Max.	
Bus free to BYSO "H"	t_{BFBO}	(6 + n) t_{CLF}*	(7 + n) t_{CLF} + 70*	ns
BSYO "H" to to sending its own ID bit	t_{BHID}	0	60	ns
BSYO "H" to SELO "H"	t_{BHSO}	$32t_{CLF}$ −40	$32t_{CLF}$ +30	ns
SELO "H" to to sending ID	t_{SOID}	$11t_{CLF}$ −30	$11t_{CLF}$ +50	ns
SELO "H" to INIT "H"	t_{SOIT}	$11t_{CLF}$ −30	$11t_{CLF}$ +50	ns
INIT "H" to ATNO "H"	t_{ITAT}	−10	30	ns
Sending ID to BSYO "L"	t_{IDBL}	$2t_{CLF}$ −50	$2t_{CLF}$ +30	ns
BSYI "H" to SEYO "L", ID hold	t_{BISL}	$2t_{CLF}$	$3t_{CLF}$ +120	ns
SELO "L" to INTR "H"	t_{SCIR}	—	40	ns

*n = TCL register setting value

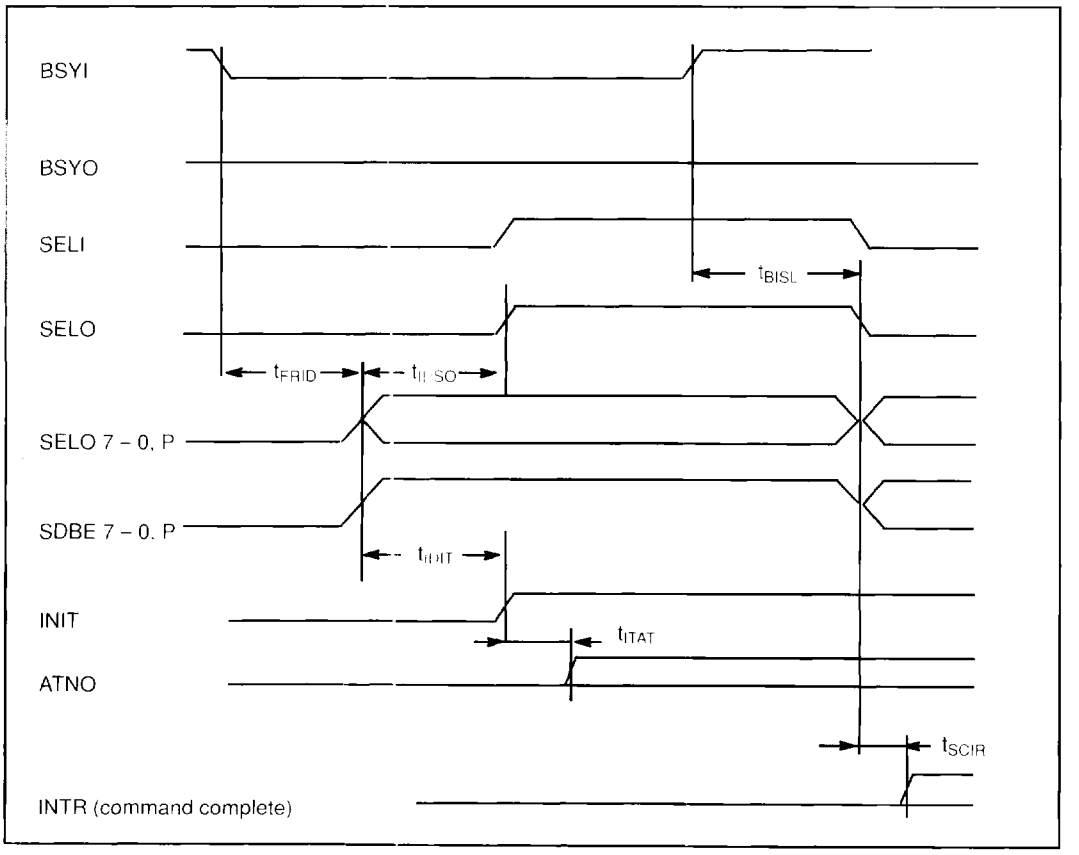


AC CHARACTERISTICS

Selection: Initiator (no arbitration)

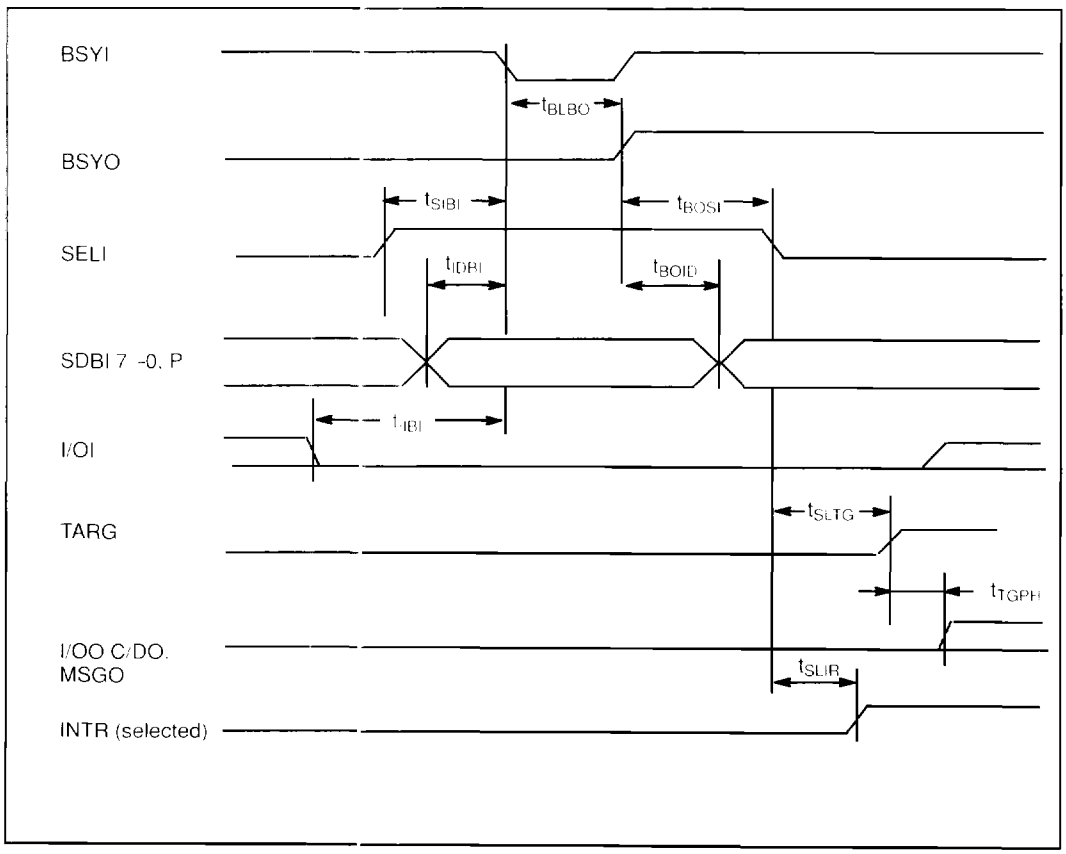
Parameter	Designator	Values		Unit
		Min.	Max.	
Bus free to sending ID	t_{FRID}	(6 + n) t_{CLF}*	(7 + n) t_{CLF} + 90*	ns
Sending ID to SELO "H"	t_{IDSO}	$11t_{CLF}$ −50	$11t_{CLF}$ +30	ns
Sending ID to INIT "H"	t_{IDIT}	$11t_{CLF}$ −50	$11t_{CLF}$ +40	ns
INIT "H" to ATNO "H"	t_{ITAT}	−10	30	ns
BSYI "H" to SELO "L", ID hold	t_{BISL}	$2t_{CLF}$	$3t_{CLF}$ +120	ns
SELO "L" to INTR "H"	t_{SCIR}	—	40	ns

*n = TCL register setting value



Selection: Target (including arbitration)

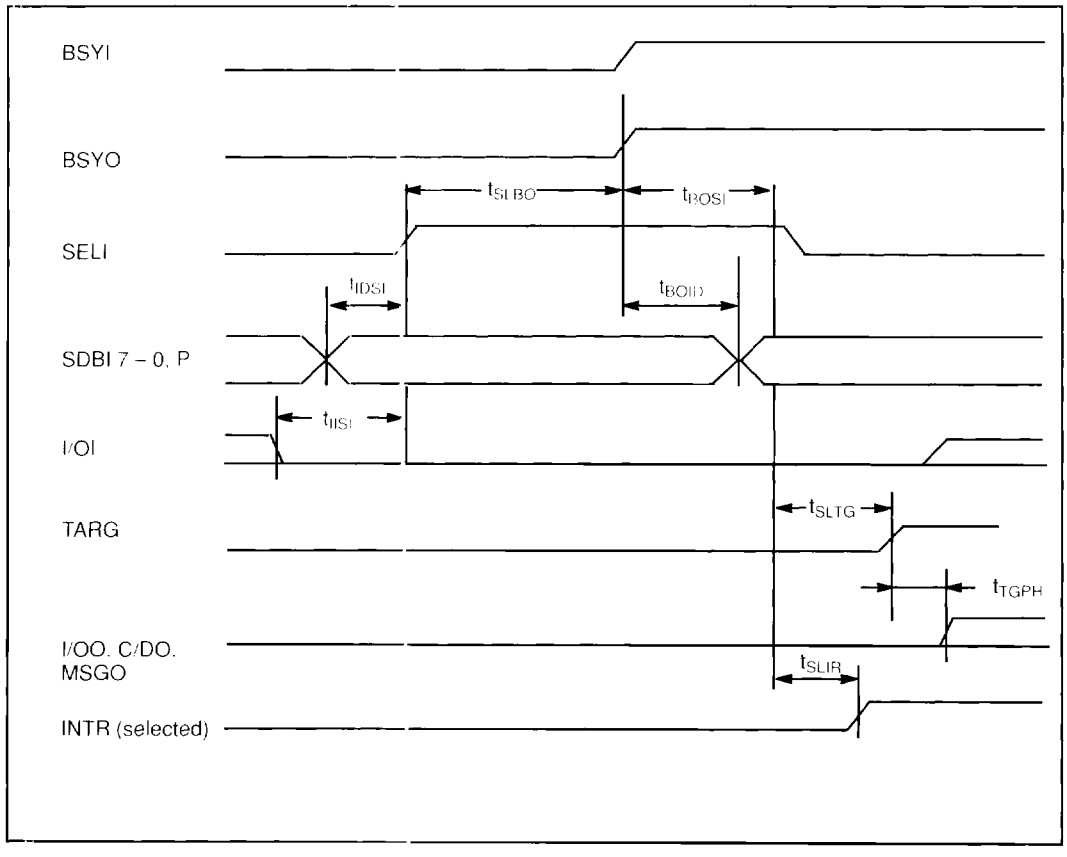
Parameter	Designator	Values		Unit
		Min.	Max.	
SELI "H" to BSYI "L"	t_{SIBI}	0	—	ns
ID valid to BSYI "L"	t_{IDBI}	0	—	ns
I/OI "L" to BSYI "L"	t_{IIBI}	0	—	ns
BSYI "L" to BSYO "H"	t_{BLBO}	$4t_{CLF}$	$5t_{CLF}$ +60	ns
BSYO "H" ID hold	t_{BOID}	20	—	ns
BSYO "H" to SELI "L"	t_{BOSI}	0	—	ns
SELI "L" to TARG "H"	t_{SLTG}	$3t_{CLF}$	$4t_{CLF}$ +70	ns
TARG "H" to Phase signal outpu	t_{TGPH}	−10	30	ns
SELI "L" to INTR "H"	t_{SLIR}	—	$3t_{CLF}$ +70	ns



AC CHARACTERISTICS

Selection: Target (no arbitration)

Parameter	Designator	Values		Unit
		Min.	Max.	
ID valid to SELI "H"	t_{IDSI}	0	—	ns
I/OI "L" to SELI "H"	t_{IISI}	0	—	ns
SELI "H" to BSYO "H"	t_{SLBO}	$4t_{CLF}$	$5t_{CLF}$ +100	ns
BSYO "H" to ID hold	t_{BOID}	20	—	ns
BSYO "H" to SELI "L"	t_{BOSI}	0	—	ns
SELI "L" to TARG "H"	t_{SLTG}	$3t_{CLF}$	$4t_{CLF}$ +70	ns
TARG "H" to Phase signal output	t_{TGPH}	−10	30	ns
SELI "L" to INTR "H"	t_{SLIR}	—	$3t_{CLF}$ +70	ns

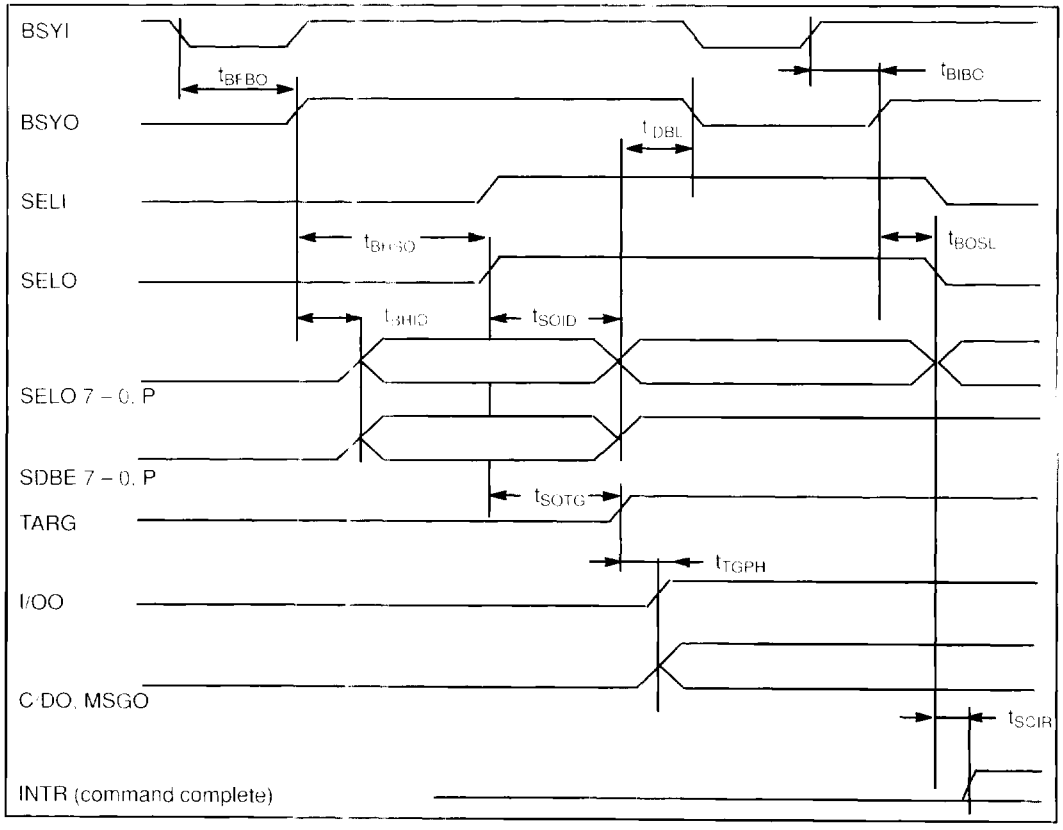


AC CHARACTERISTICS

Reselection: Target

Parameter	Designator	Values		Unit
		Min.	Max.	
Bus free to BYSO "H"	t_{BFBO}	(6 + n) t_{CLF}*	(7 + n) t_{CLF} + 70*	ns
BSYO "H" to sending its own ID bit	t_{BHID}	0	60	ns
BSYO "H" to SELO "H"	t_{BHSO}	$32t_{CLF}$ −40	$32t_{CLF}$ +30	ns
SELO "H" to sending ID	t_{SOID}	$11t_{CLF}$ −30	$11t_{CLF}$ +50	ns
SELO "H" to TARG "H"	t_{SOTG}	$11t_{CLF}$ −30	$11t_{CLF}$ +50	ns
TARG "H" to sending phase signal	t_{TGPH}	−10	30	ns
Sending ID to BSYO "L"	t_{IDBL}	$2t_{CLF}$ −50	$2t_{CLF}$ +30	ns
BSYI "H" to BSYO "H"	t_{BIBO}	2 t_{CLF}	$3t_{CLF}$ +90	ns
BSYO "H" to SELO "L", ID hold	t_{BOSL}	t_{CLF} −20	t_{CLF} +60	ns
SELO "L" to INTR "H"	t_{SCIR}	—	40	ns

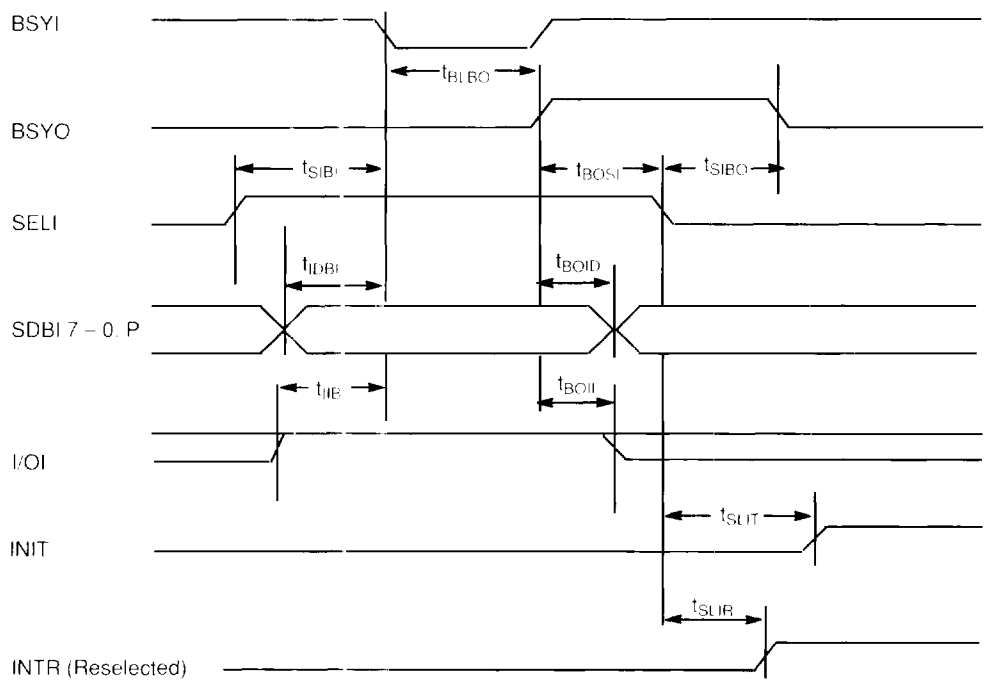
*n = TCL register setting value



AC CHARACTERISTICS

Reselection: Initiator

Parameter	Designator	Values		Unit
		Min.	Max.	
SELI "H" to BSYI "L"	t_{SIBI}	0	—	ns
ID valid to BSYI "L"	t_{IDBI}	0	—	ns
I/OI "H" to BSYI "L"	t_{IIBI}	0	—	ns
BSYI "L" to BSYO "H"	t_{BLBO}	$4t_{CLF}$	$5t_{CLF}$ +60	ns
BSYO "H" to ID hold	t_{BOID}	20	—	ns
BSYO "H" to SELI "L"	t_{BOSI}	0	—	ns
BSYO "H" to I/D hold	t_{BOII}	20	—	ns
SELI "L" to INIT "H"	t_{SLIT}	$3t_{CLF}$	$4t_{CLF}$ +70	ns
SELI "L" to BSYO "L"	t_{SIBO}	$2t_{CLF}$	$3t_{CLF}$ +60	ns
SELI "L" to INTR "H"	t_{SLIR}	—	$3t_{CLF}$ +70	ns



AC CHARACTERISTICS

Asynchronous Transfer: Initiator REQ-ACK Timing

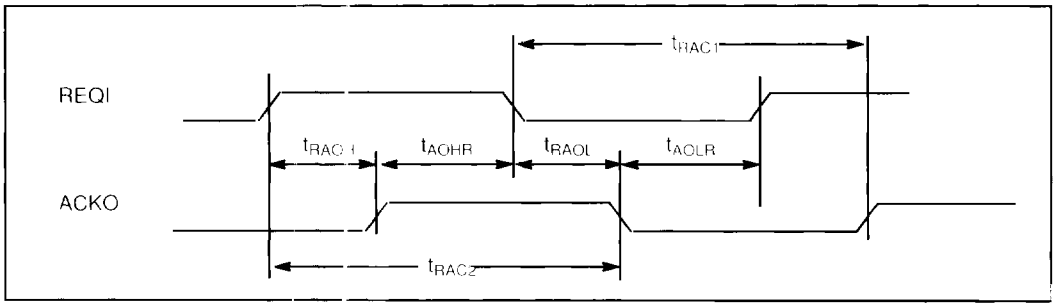
Parameter	Designator	Values		Unit
		Min.	Max.	
REQI "H" to ACKO "H"	t_{RAOH}	10	75 [3]	ns
ACKO "H" to REQI "L"	t_{AOHR}	0	—	ns
REQI "L" to ACKO "L"	t_{RAOL}	10	75 [3]	ns
ACKO "L" to REQI "H"	t_{AOLR}	10	—	ns
REQI "L" to ACKO "H" [1]	t_{RAC1}	$2t_{CLF}$	$3t_{CLF}+110$ [3]	ns
REQI "H" to ACKO "L" [2]	t_{RAC2}	$2t_{CLF}$	$3t_{CLF}+110$ [3]	ns

Notes: [1]The time from REQI "L" to ACK "H" is set by the longer one of either (t_{RAOL} + t_{AOLR} + t_{RAOH}) or t_{RAC1}.

[2]Used during input. The time from REQ1 "H" to ACKO "L" is set by the longer one of either (t_{RAOH} + t_{AOHR} + t_{RAOL}) or t_{RAC2}.

[3]The time value of this table is not valid under the following conditions:

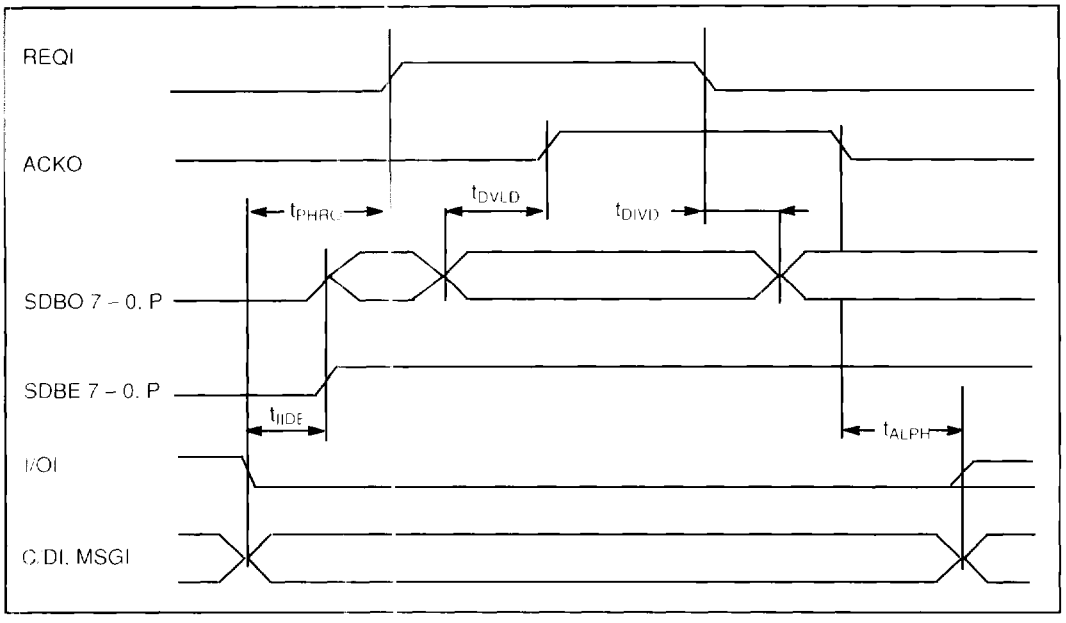
1. Data buffer is empty during output.
2. Data buffer is full during input.
3. During the transfer of the first bit or the last bit.
4. When SPC automatically sends ATNO signals during input.



AC CHARACTERISTICS

Asynchronous Transfer: Initiator Output

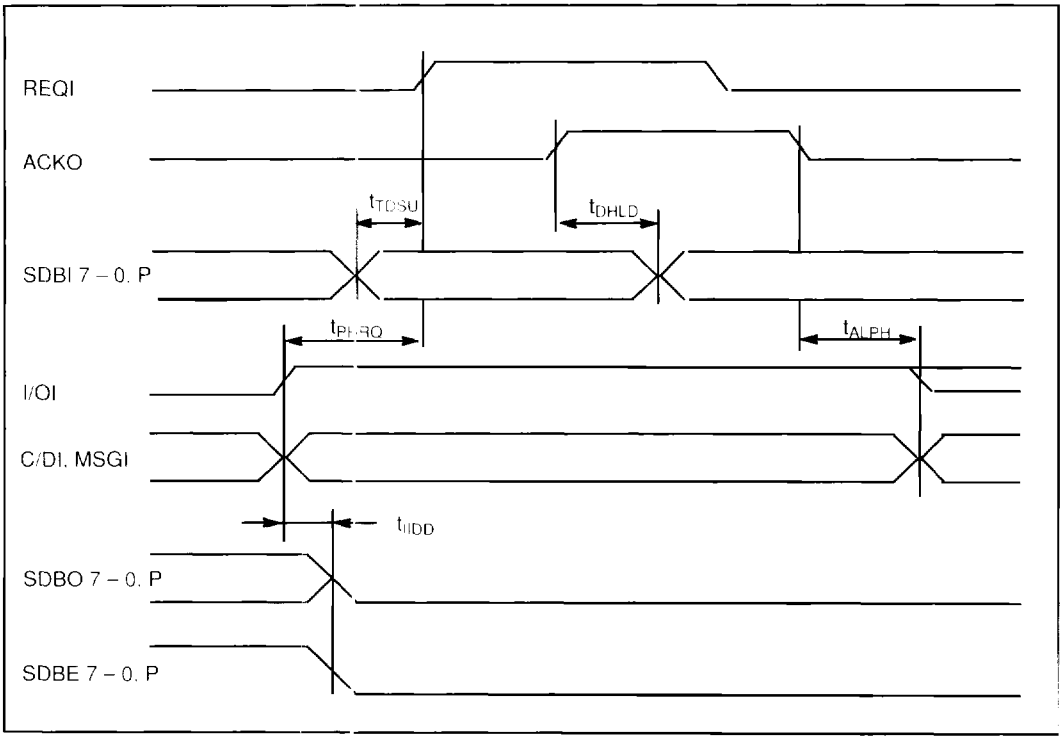
Parameter	Designator	Values		Unit
		Min.	Max.	
I/O "L" to Data bus output	t_{IIDE}	10	100	ns
Set Phase to REQI "H"	t_{PHRQ}	100	—	ns
Data bus output invalid to ACKO "H	t_{DVLD}	$2t_{CLF}-80$	—	ns
REQI "L" to Data bus hold	t_{DIVD}	15	—	ns
ACKO "L" to Phase change	t_{ALPH}	10	—	ns



AC CHARACTERISTICS

Asynchronous Transfer: Initiator Input

Parameter	Designator	Values		Unit
		Min.	Max.	
I/OI "H" to Data bus output terminate	t_{IIDD}	—	100	ns
Set Phase to REQI "H"	t_{PHRQ}	100	—	ns
Data bus valid to REQI "H"	t_{TDSU}	10	—	ns
ACKO "H" to Data bus hold	t_{DHLD}	15	—	ns
ACKO "L" to Phase change	t_{ALPH}	10	—	ns



AC CHARACTERISTICS

Asynchronous Transfer: Target, REQ-ACK Timing

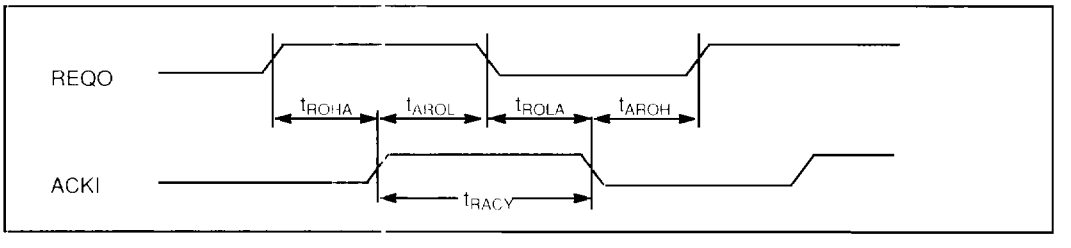
Parameter	Designator	Values		Unit
		Min.	Max.	
REQO "H" to ACKI "H"	t_{ROHA}	20	--	ns
ACKI "H" to REQO "L"	t_{AROL}	10	60	ns
REQO "L" to ACKI "L"	t_{ROLA}	0	--	ns
ACKI "L"to REQO "H"	t_{AROH}	10	70 [2]	ns
ACKI "H" to REQO "H"[1]	t_{RACY}	$2t_{CLF}$	$3t_{CLF}$ +110 [2]	ns

Notes: [1]The time for ACKI "H" to REQO "H" is set by the longer one of either (t_{AROL} + t_{ROLA} + t_{AROH}) or t_{RACY}.

[2]The time value of this table is not valid under the following conditions:

a When data buffer is empty during output.

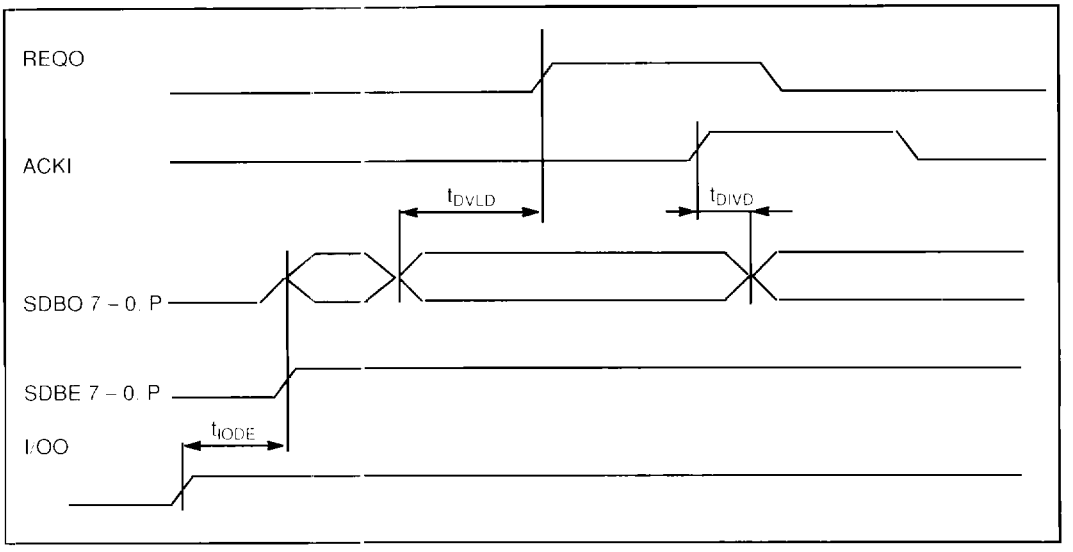
b When data buffer is full during input.



AC CHARACTERISTICS

Asynchronous Transfer: Target, Output

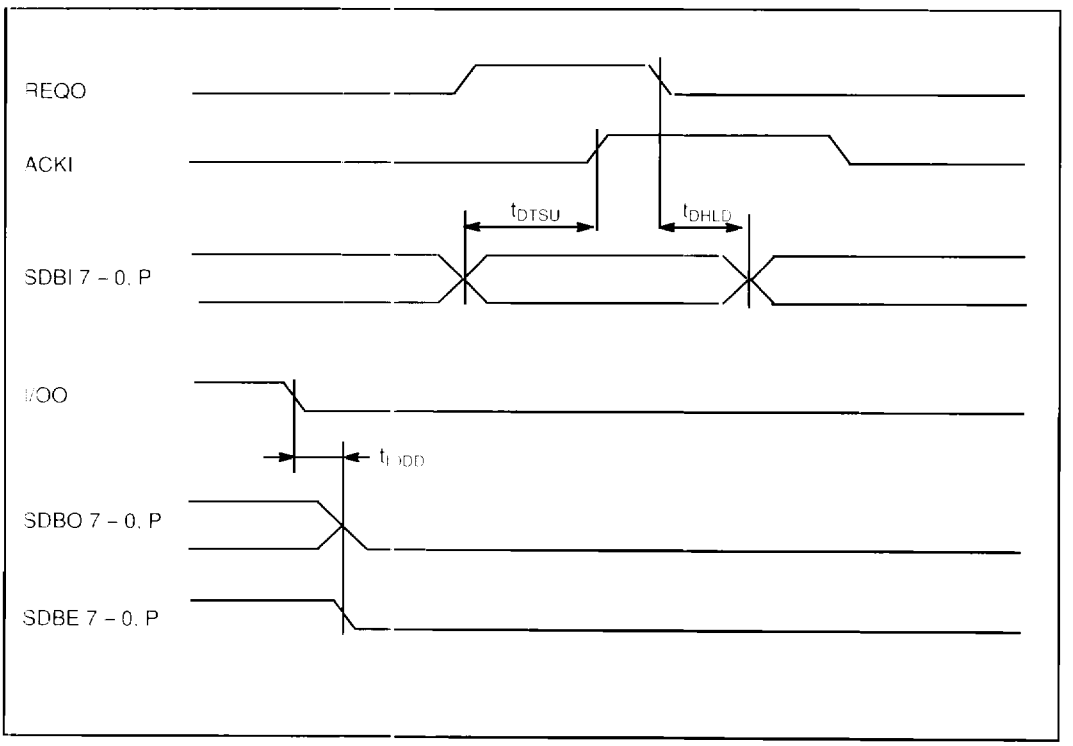
Parameter	Designator	Values		Unit
		Min.	Max.	
I/O "H" to Data bus output	t_{IODE}	$7t_{CLF}$	$8t_{CLF}+110$	ns
Data bus output valid to REQO "H"	t_{DVLD}	$2t_{CLF}-80$	—	ns
ACKI "H" to Data bus hold	t_{DIVD}	15	—	ns



AC CHARACTERISTICS

Asynchronous Transfer: Target, Input

Parameter	Designator	Values		Unit
		Min.	Max.	
I/O "L" to Data bus output terminate	t_{IODD}	—	60	ns
Data bus output valid to ACKI "H"	t_{DTSU}	10	—	ns
REQO "L" to Data bus hold	t_{DHLD}	15	—	ns



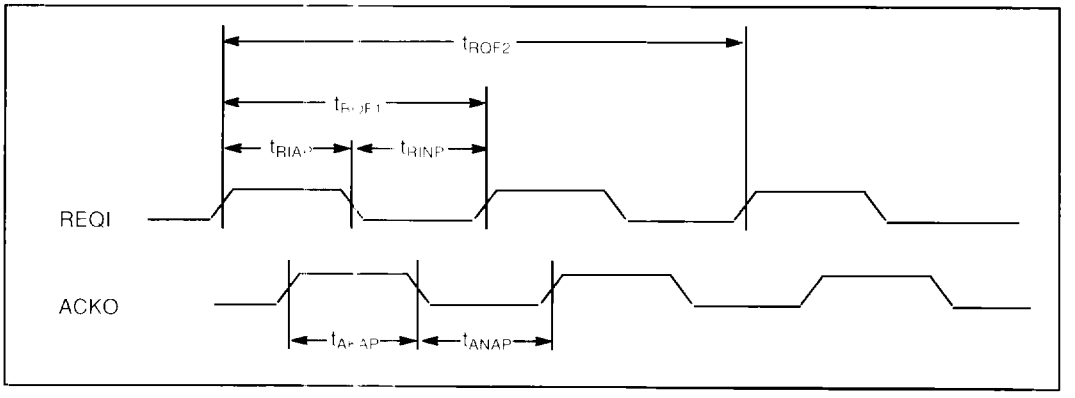
AC CHARACTERISTICS

Synchronous Transfer: Initiator, REQ-ACK Cycle

Parameter	Designator	Values		Unit
		Min.	Max.	
REQI Assertion Period	t_{RIAP}	50	—	ns
REQI Nonassertion Period	t_{RINP}	50	—	ns
REQI Cycle time1	t_{ROF1}	t_{CLF}	—	ns
REQI Cycle time2	t_{ROF2}	$3t_{CLF}$	—	ns
ACKO Assertion Period	t_{AKAP}	t_{CLF} −10	—	ns
ACKO Nonassertion Period	t_{ANAP}	nt_{CLF} −10*	—	ns

Notes: *n is set by TMOD register

TMOD Register		n
Bit3	Bit2	
0	0	1
0	1	2
1	0	3
1	1	4



AC CHARACTERISTICS

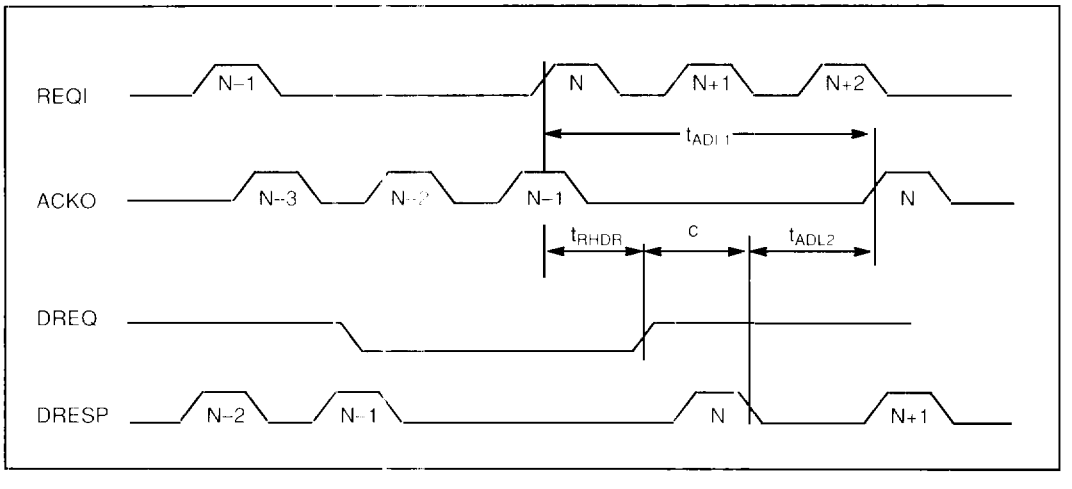
Synchronous Transfer: Initiator, REQ-ACK Timing

Parameter	Designator	Values		Unit
		Min.	Max.	
ACKO Answer delay time1[1]	t_{ADL1}	$3t_{CLF}$	$4t_{CLF}$ +100	ns
REQI "H" to DREQ "H"[2]	t_{RHDR}	t_{CLF} +40	$3t_{CLF}$ +60	ns
ACKO Answer delay time2[3]	t_{ADL2}	$3t_{CLF}$	$4t_{CLF}$ +120	ns

Notes: [1]For the case when maximum input offset value is less than 4 or during output. The minimum time between receiving bit N of REQI and sending bit N of ACKO. (Not applicable when data buffer is empty during output.)

[2]During input

[3]Applicable when maximum input offset value is between 5 and 8. This is the minimum time between receiving bit N of DRESP and sending bit N of ACKO. In this case, the minimum time between receiving bit N of REQI and sending bit N of ACKO is (t_{RHDR} +(DRESP answer time X) + t_{ADL2})



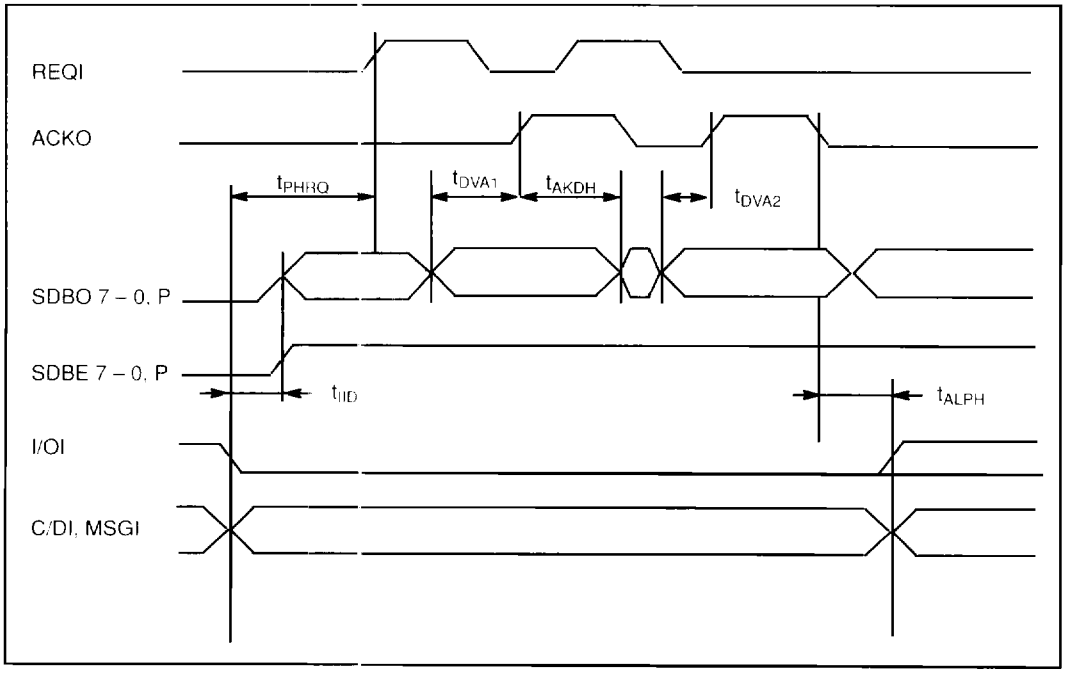
AC CHARACTERISTICS

Synchronous Transfer: Initiator, Output

Parameter	Designator	Values		Unit
		Min.	Max.	
I/OI "L" to Data bus output	t_{IIDE}	10	100	ns
Set Phase to REQI "H"	t_{PHRQ}	100	—	ns
Data bus output valid to ACKO "H"[1]	t_{DVA1}	$2t_{CLF}$ –70	—	ns
	t_{DVA2}	nt_{CLF} –60 [2]	—	ns
ACKO "H" to Data bus hold	t_{AKDH}	t_{CLF} –20	—	ns
ACKO "L" to Phase change	t_{ALPH}	10	—	ns

Notes: [1]The time from data bus output valid to ACKO "H" is set by the shorter one of t_{DVA1} or t_{DVA2}.
[2]n is set by TMOD register.

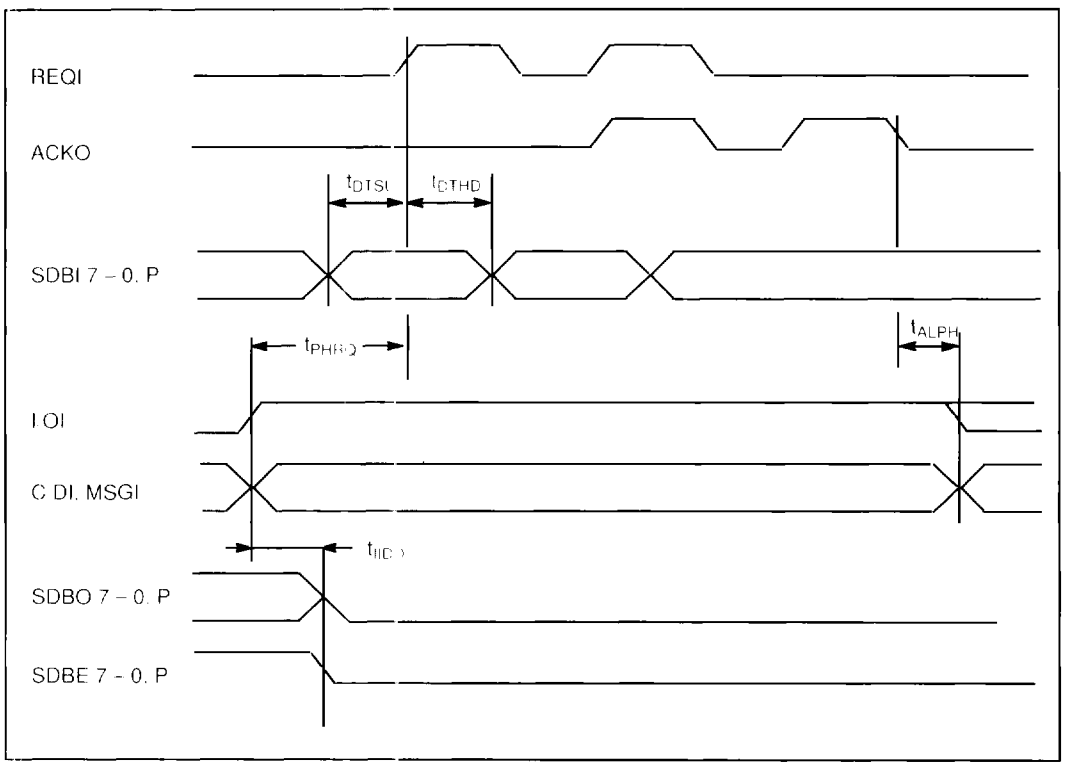
TMOD Register		n
Bit3	Bit2	
0	0	1
0	1	2
1	0	3
1	1	4



AC CHARACTERISTICS

Synchronous Transfer: Initiator, Input

Parameter	Designator	Values		Unit
		Min.	Max.	
I/OI "H" to Data bus output terminate	t_{IIDD}	—	100	ns
Set Phase to REQI "H"	t_{PHRQ}	100	—	ns
Data bus valid to REQI "H"	t_{DTSU}	10	—	ns
REQI "H" to Data bus hold	t_{DTHD}	40	—	ns
ACKO "L" to Phase change	t_{ALPH}	10	—	ns



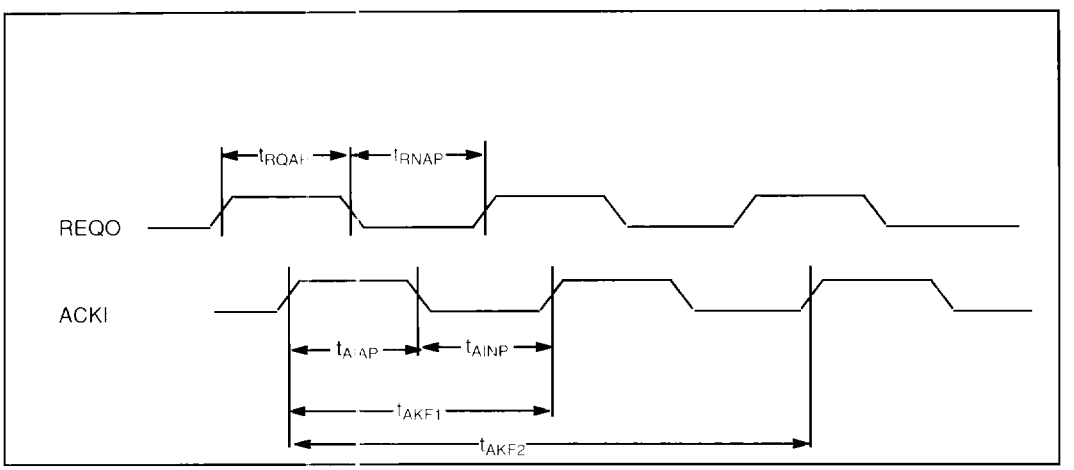
AC CHARACTERISTICS

Synchronous Transfer: Target, REQ-ACK Cycle

Parameter	Designator	Values		Unit
		Min.	Max.	
REQO Assertion Period	t_{RQAP}	t_{CLF} −10	—	ns
REQO Nonassertion Period	t_{RNAP}	nt_{CLF} −10*	—	ns
ACKI Assertion Period	t_{AIAP}	50	—	ns
ACKI Nonassertion Period	t_{AINP}	50	—	ns
ACKI Cycle time1	t_{AKF1}	t_{CLF}	—	ns
ACKI Cycle time2	t_{AKF2}	$3t_{CLF}$	—	ns

Notes: *n is set by TMOD register.

TMOD Register		n
Bit3	Bit2	
0	0	1
0	1	2
1	0	3
1	1	4

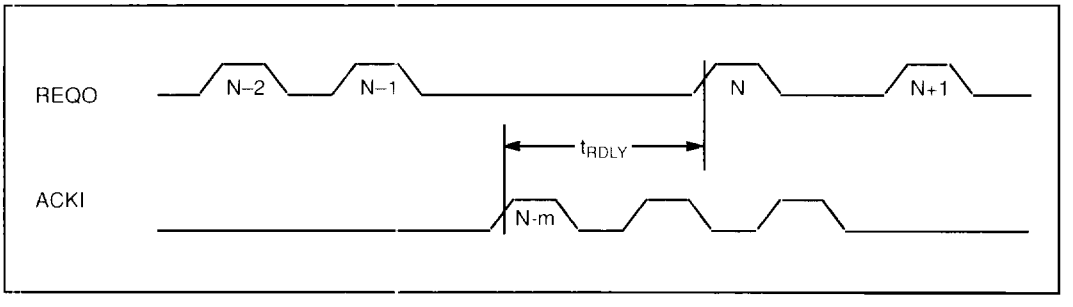


AC CHARACTERISTICS

Synchronous Transfer: Target, REQ-ACK Timing

Parameter	Designator	Values		Unit
		Min.	Max.	
REQO Send delay time[1]	t_{RDLY}	$3t_{CLF}$	$4t_{CLF}$ +100	ns

Notes: [1]The time between receiving bit (N – m) of ACKI and sending bit N of REQO during maximum offset value is set at m (m = 1 to 8).



AC CHARACTERISTICS

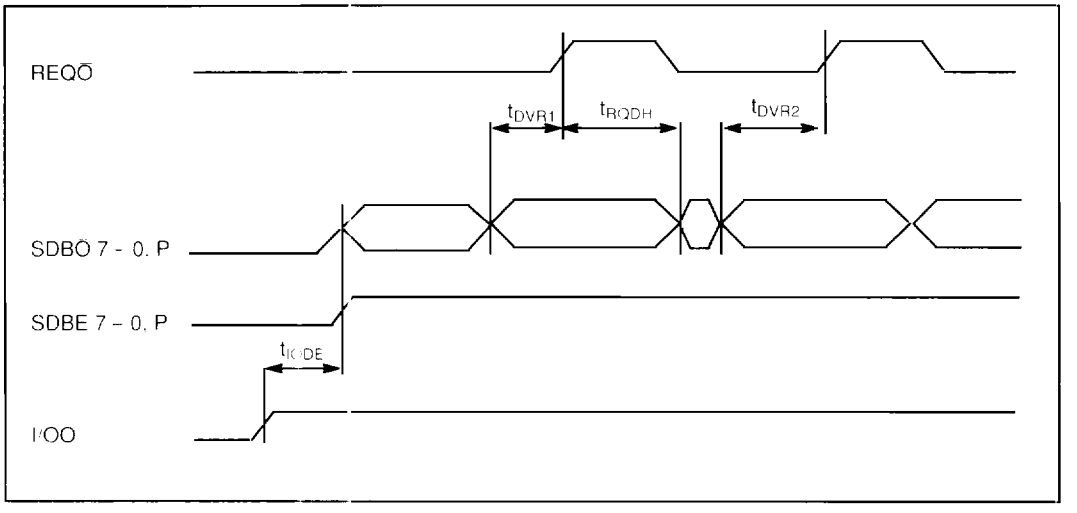
Synchronous Transfer: Target, Output

Parameter	Designator	Values		Unit
		Min.	Max.	
I/OO "H" to Data bus output	t_{IODE}	$7t_{CLF}$	$8t_{CLF}$ +110	ns
Data bus output valid to REQO "H"[2]	t_{DVR1}	$2t_{CLF}$ −70	—	ns
	t_{DVR2}	nt_{CLF} −60 [1]	—	ns
REQO "H" to Data bus hold	t_{RQDH}	t_{CLF} −20	—	ns

Notes: [1]is set by TMOD register.

[2]The time between data bus output valid and REQO "H" is set by the shorter one of t_{DVR1} or t_{DVR2}.

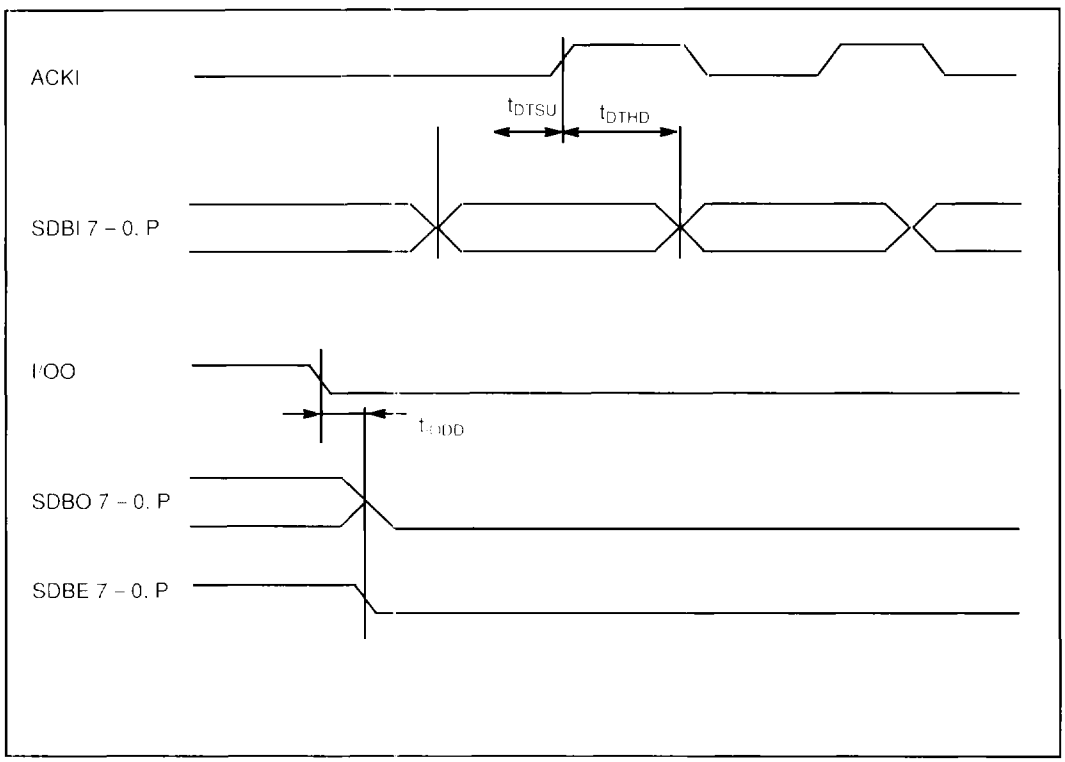
TMOD Register		n
Bit3	Bit2	
0	0	1
0	1	2
1	0	3
1	1	4



AC CHARACTERISTICS

Synchronous Transfer: Target, Input

Parameter	Designator	Values		Unit
		Min.	Max.	
I/OO "L" to Data bus output	t_{IODD}	—	60	ns
Data bus output valid to ACKI "H"	t_{DTSU}	10	—	ns
ACKI "H" to Data bus hold	t_{DTHD}	40	—	ns

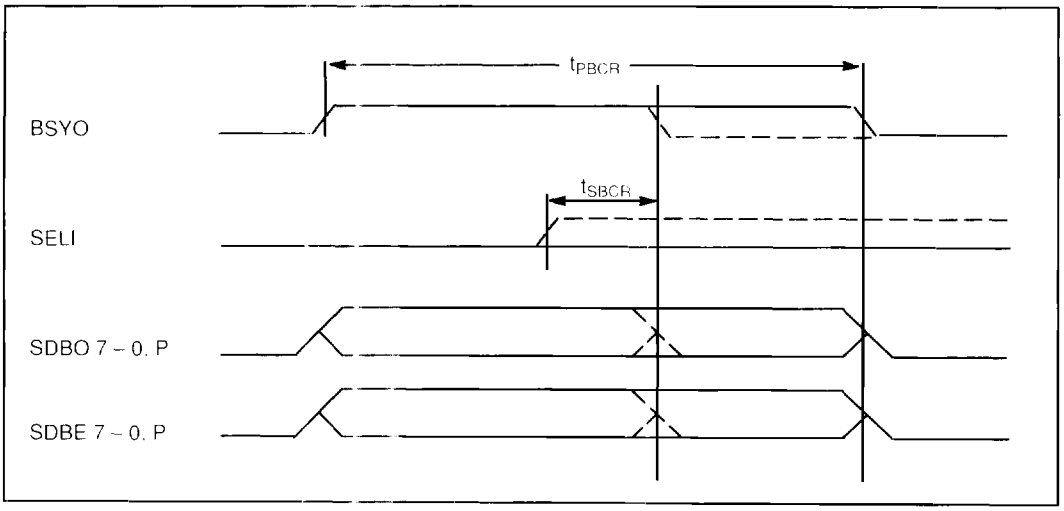


AC CHARACTERISTICS

Bus Free: Arbitration Failure

Parameter	Designator	Values		Unit
		Min.	Max.	
Begin arbitration to BSYO "L", ID bit send terminate[1]	t_{PBCR}	$32t_{CLF}-40$	$32t_{CLF}+60$	ns
SELI "H" to BSYO "L", ID bit send terminate[2]	t_{SBCR}	$2t_{CLF}$	$3t_{CLF}+120$	ns

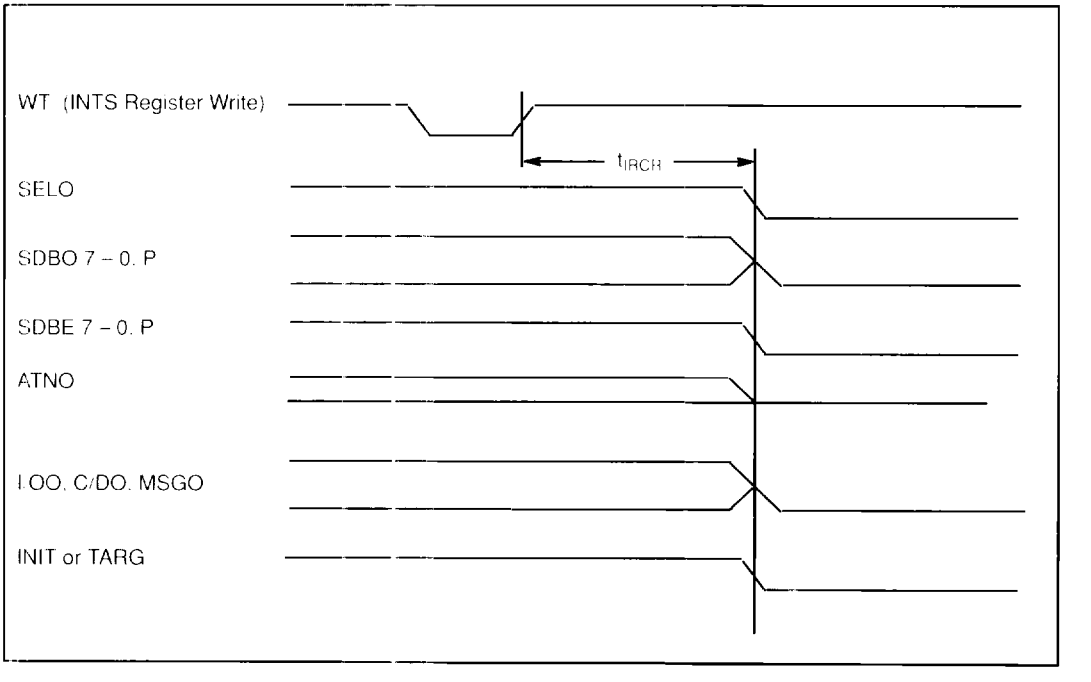
Notes: [1]When choosing ID bit which has a higher priority number than itself.
[2]When other bus device asserts SEL signals.



AC CHARACTERISTICS

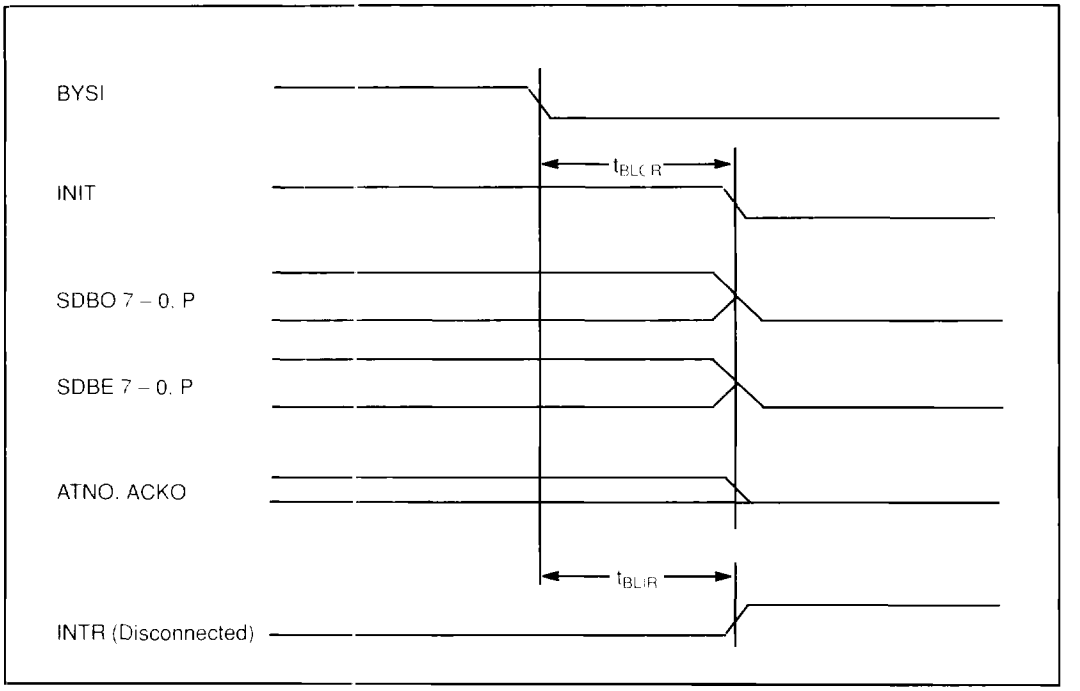
Bus Free: Selection, Reselection Timeout

Parameter	Designator	Values		Unit
		Min.	Max.	
Timeout interrupt reset to SELO "L", bus clear, INIT or TARG "L"	t_{IRCR}	---	$3t_{CLF}$ +110	ns



AC CHARACTERISTICS

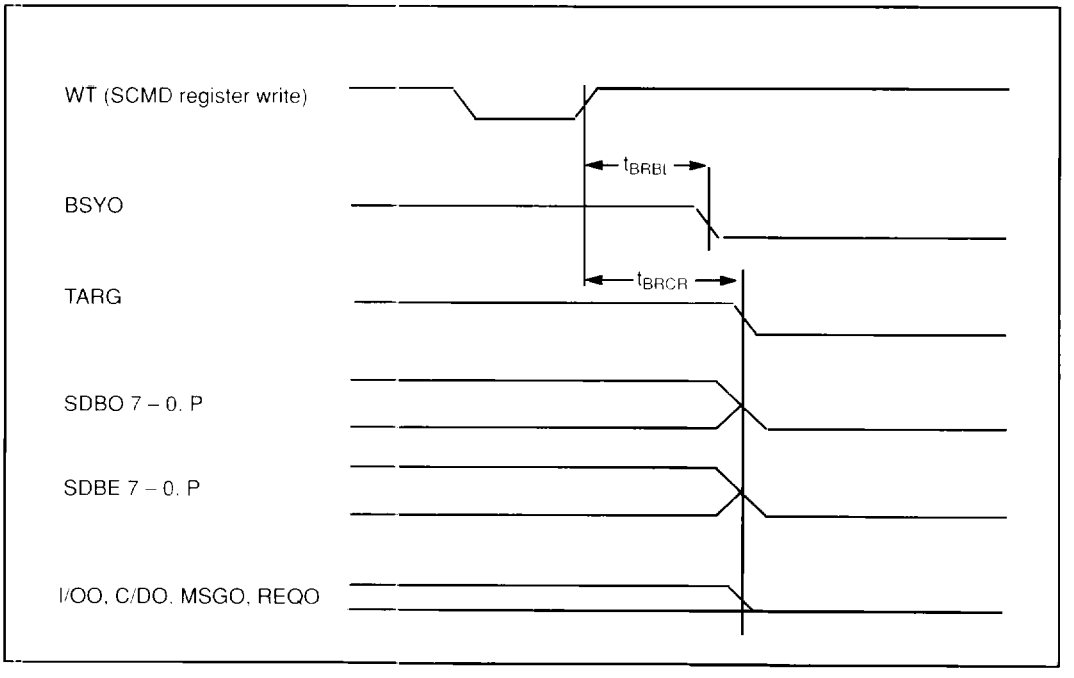
Bus Free: Initiator (Disconnected)				
Parameter	Designator	Values		Unit
		Min.	Max.	
BSYI "L" to INIT "L" bus clear	t_{BLCR}	—	$5t_{CLF}$ +120	ns
BSYI "L" to INTR "H"	t_{BLIR}	—	$6t_{CLF}$ +80	ns



AC CHARACTERISTICS

Bus Free: Target (Bus Release Command)

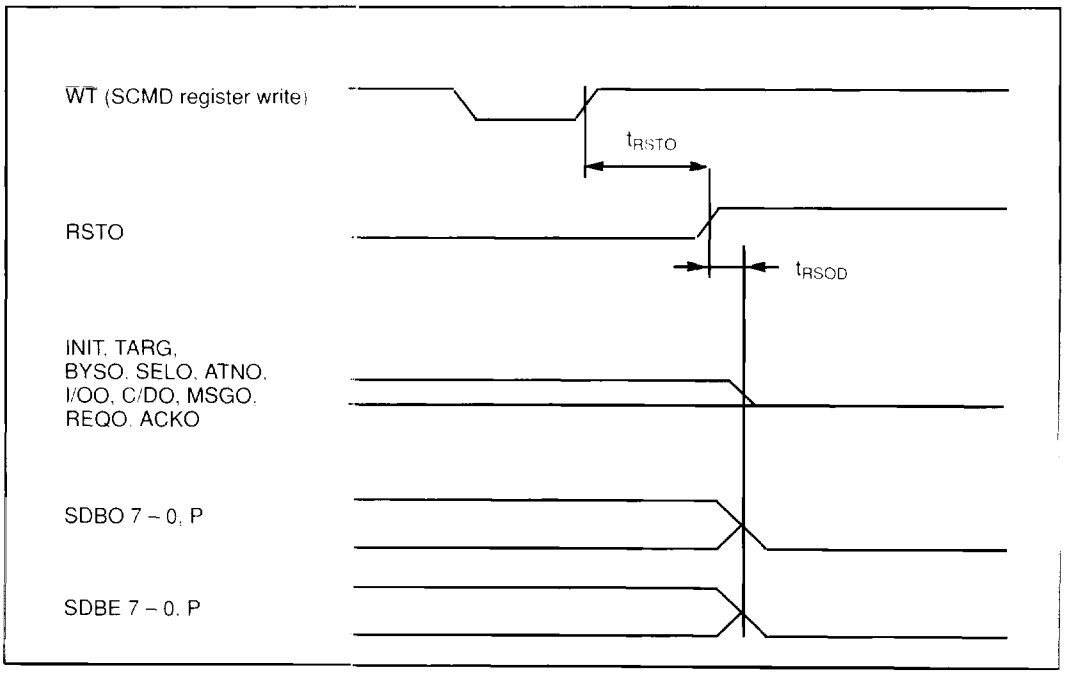
Parameter	Designator	Values		Unit
		Min.	Max.	
Issue Bus Release Command to BSYO "L"	t_{BRBL}	—	$3t_{CLF}$ +80	ns
Issue Bus Release Command to TARG "L", bus clear	t_{BRCR}	—	$3t_{CLF}$ +130	ns



AC CHARACTERISTICS

Reset Condition: Send RST Signal

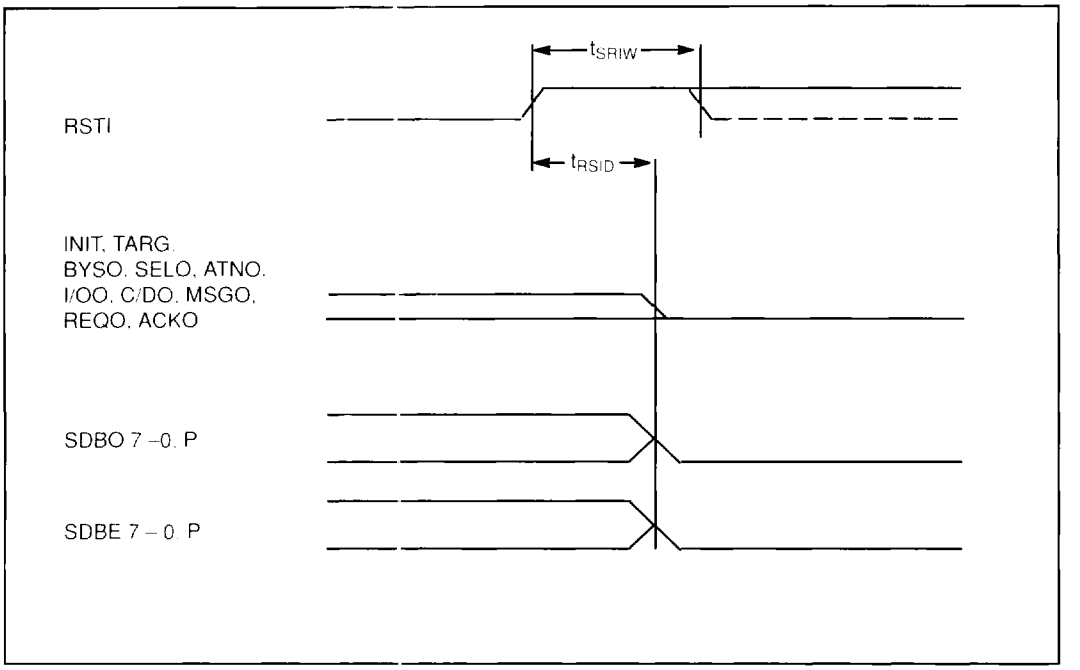
Parameter	Designator	Values		Unit
		Min.	Max.	
Write "1" to SCMD register bit 4 to RSTO "H"	t_{RSTO}	—	60	ns
RSTO "H" to send signal terminate	t_{RSOD}	—	80	ns



AC CHARACTERISTICS

Reset Condition: RST Signal Detection

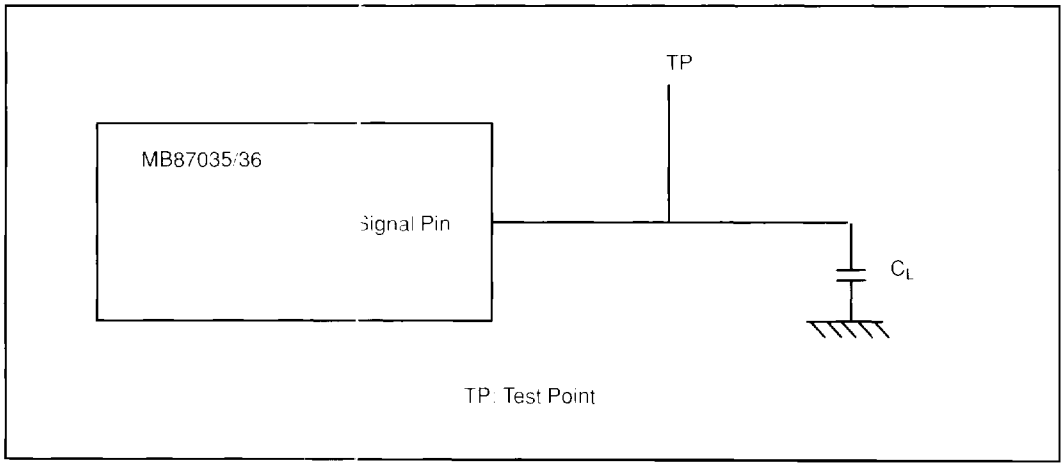
Parameter	Designator	Values		Unit
		Min.	Max.	
Reset condition detection time	t_{SRIW}	$3t_{CLF}$	—	ns
RSTI "H" to signal send terminate	t_{RSID}	—	$4t_{CLF}$ +120	ns



AC CHARACTERISTICS

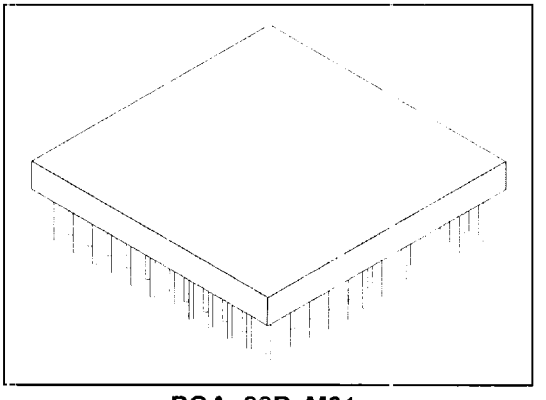
AC Characteristics Measurement Condition

Pin Name	C_L	Unit
D7 – D0, DP, HDB7 – HDB0, HDBP	85	pF
DPO	65	pF
Other than above output pins	60	pF



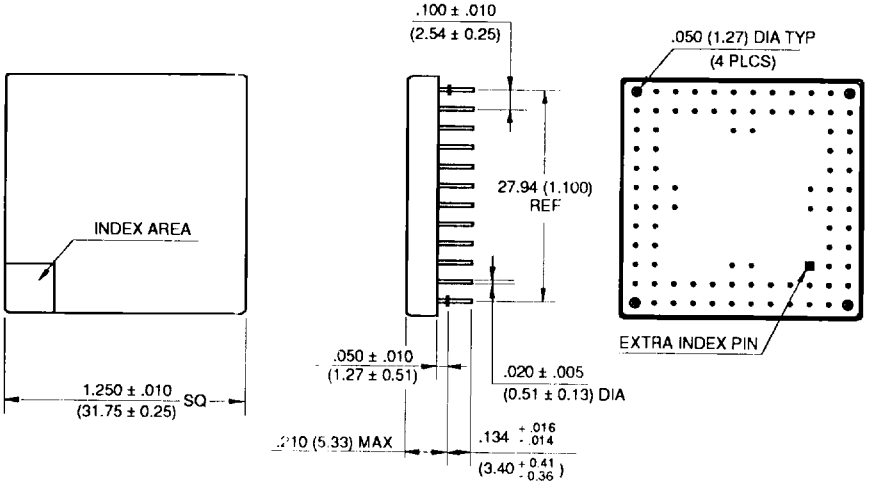
PIN GRID ARRAY (MB87035)

88-Lead Plastic Pin Grid Array



PGA–88P–M01

88-LEAD PLASTIC PIN GRID ARRAY PACKAGE
(Case No.: PGA-88P-M01)

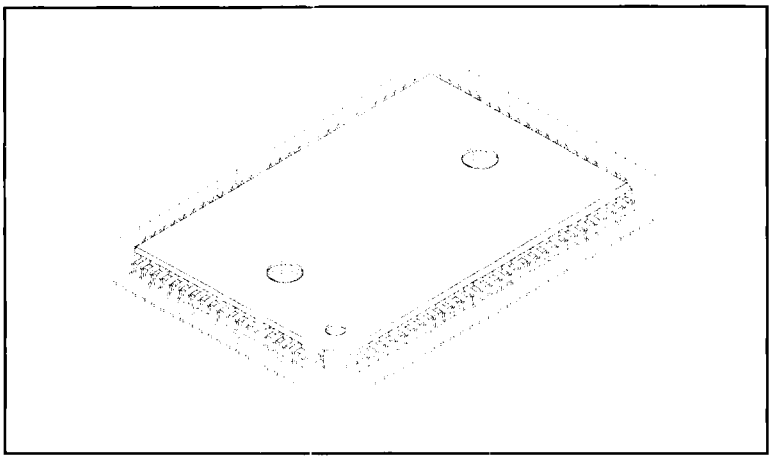


Dimensions in
inches (millimeters)

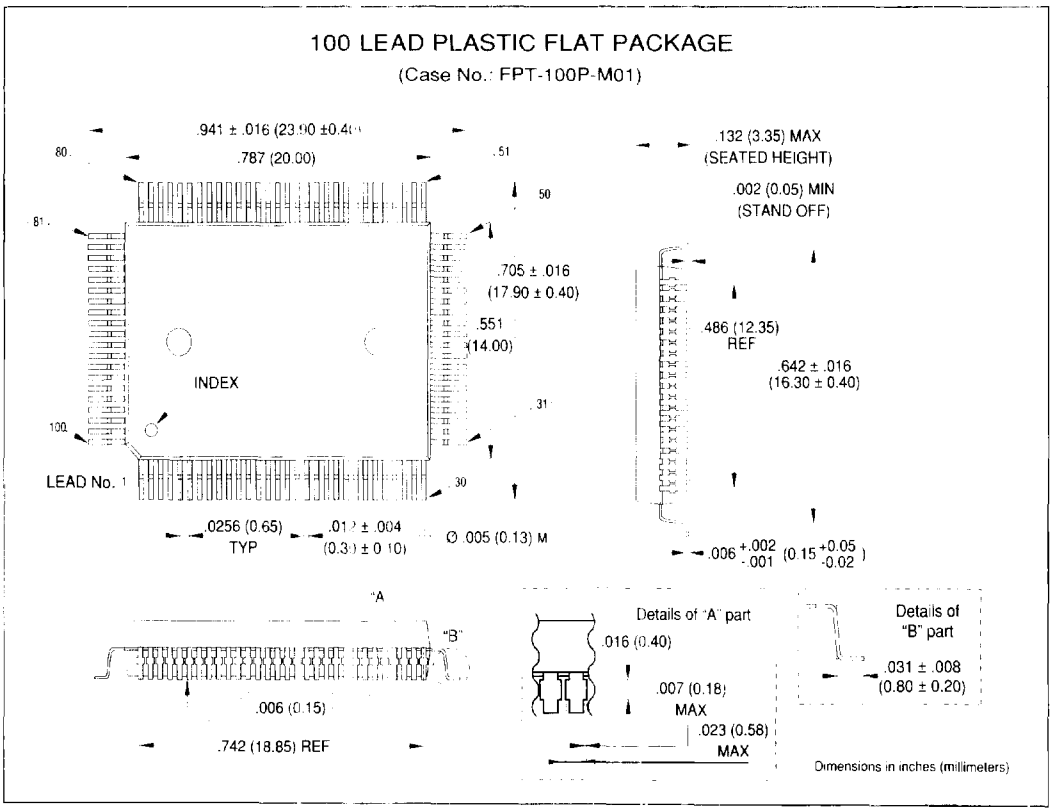
R88002SC-3C

FLAT PACKAGE (MB87036)

100-Lead Plastic Pin Grid Array



FPT–100P–M01



Additional Notes About Input Clock Frequency

MB87035/36 guarantees performance up to input clock frequency of 10 MHz. However, if the input clock frequency exceeds 8 MHz, SCSI timing requirments may not be satisfied.

- If used with systems which must meet SCSI timing requirements, input clock frequency may be between 5 and 8 MHz.
- If used with systems which do not have to meet SCSI requirements, input clock frequency may be between 5 and 10 MHz.

Timing Requirement Conditions if Input Clock Frequency >8MHz

Item	Action Condition	Application INIT	Application TARG	Timing Parameter	Time Condition (Minimum Value) SCSI Specification	Time Condition (Minimum Value) MB87035/36 AC Characteristics[1]
1	Selection Phase	○		The time between asserting SEL after arbitration and sending ID to data bus	1.2 ms	$11t_{CLF}$ –30 ns
	Reselection Phase		○			
2	Reselection Phase		○	The time between the target asserting BSY after acknowledging BSY from the initiator and negating SEL.	90 ns	t_{CLF} –20 ns
3	Information Transfer Phase		○	The time between activating I/O to True and activating of data bus	800 ns	$7t_{CLF}$ ns
4	Synchronous Transfer Output	○	○	Data bus hold time after asserting ACK or REQ	100 ns	t_{CLF} –20 ns
5	Asynchronous Transfer Output[3]	○	○	The time between acknowledging data bus output and asserting ACK or REQ	55 ns	$2t_{CLF}$ –80 ns
6	Synchronous Transfer Output[3]	○	○	The time between acknowledging data bus output and asserting ACK or REQ	55 ns	$2t_{CLF}$ –70 ns also $n \bullet t_{CLF}$ –60 ns[2]
7	Synchronous Transfer	○	○	ACK, REQ negation period	90 ns	$n \bullet t_{CLF}$ –10 ns[2]

Notes: [1]t_{CLF} is clock cycle (ns)
[2]n is set by TMOD register (n = 1–4)
[3]Items 5 – 7 can violate SCSI specifications depending on the setting of TMOD register and/or the transmission characteristics of the interface. Items 6 and 7 can violate SCSI specifications if the appropriate value is not set for the TMOD register even if clock input is below 8 MHz.