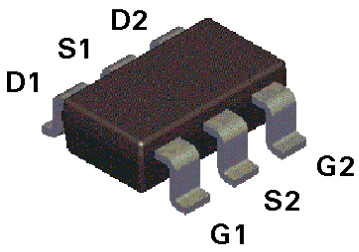
General Description

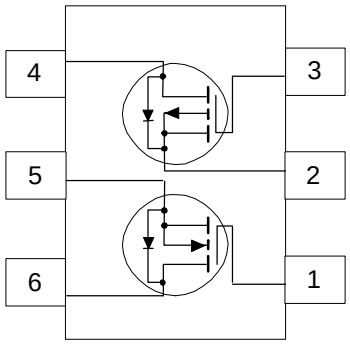
These dual N and P-channel enhancement mode power field effect transistors are produced using TY's proprietary, high cell density, DMOS technology. This very high density process has been designed to minimize on-state resistance, provide rugged and reliable performance and fast switching. These devices is particularly suited for low voltage, low current, switching, and power supply applications.

Features

- N-Channel 0.51A, 50V, $R_{DS(ON)}$ = 2Ω @ V_{GS}=10V
- P-Channel -0.34A, -50V. $R_{DS(ON)}$= 5Ω @ V_{GS}=-10V.
- High density cell design for low $R_{DS(ON)}$.
- Proprietary SuperSOT™-6 package design using copper lead frame for superior thermal and electrical capabilities.
- High saturation current.



SuperSOT™-6



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage		50	-50	V
V_{GSS}	Gate-Source Voltage - Continuous		20	-20	V
I_D	Drain Current - Continuous	(Note 1a)	0.51	-0.34	A
	- Pulsed		1.5	-1	
P_D	Maximum Power Dissipation	(Note 1a)	0.96		W
		(Note 1b)	0.9		
		(Note 1c)	0.7		
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150		°C
THERMAL CHARACTERISTICS					
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	130		°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	60		°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	N-Ch	50			V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-50			
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 40 V, V_{GS} = 0 V	N-Ch			1	µA
		T_J = 125°C				500	
		V_{DS} = -40 V, V_{GS} = 0 V	P-Ch			-1	
		T_J = 125°C				-500	
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	All			-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1	1.9	2.5	V
		T_J = 125°C		0.8	1.5	2.2	
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	-1	-2.5	-3.5	
		T_J = 125°C		-0.8	-2.2	-3	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 0.51 A	N-Ch		1	2	Ω
		T_J = 125°C			1.7	3.5	
		V_{GS} = 4.5 V, I_D = 0.35 A			1.6	4	
		V_{GS} = -10 V, I_D = -0.34 A	P-Ch		2.5	5	
		T_J = 125°C			4	10	
		V_{GS} = -4.5 V, I_D = -0.25 A			5.3	7.5	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	N-Ch	1.5			A
		V_{GS} = -10 V, V_{DS} = -10 V	P-Ch	-1			
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 0.51 A	N-Ch		400		mS
		V_{DS} = -10 V, I_D = -0.34 A	P-Ch		250		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N-Channel V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		20		pF
			P-Ch		40		
C_{oss}	Output Capacitance		N-Ch		13		pF
		P-Channel V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz	P-Ch		13		
C_{rss}	Reverse Transfer Capacitance		N-Ch		5		pF
			P-Ch		4		

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameters	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	N-Channel V_{DD} = 25 V, I_D = 0.25 A, V_{GS} = 10 V, R_{GEN} = 25 Ω	N-Ch		6	20	nS
			P-Ch		14	20	
t_r	Turn - On Rise Time		N-Ch		6	20	
			P-Ch		6	20	
$t_{D(off)}$	Turn - Off Delay Time	P-Channel V_{DD} = -25 V, I_D = -0.25 A, V_{GS} = -10 V, R_{GEN} = 25 Ω	N-Ch		11	20	
			P-Ch		13	20	
t_f	Turn - Off Fall Time		N-Ch		5	20	
			P-Ch		6	20	
Q_g	Total Gate Charge	N-Channel V_{DS} = 25 V, I_D = 0.51 A, V_{GS} = 10 V	N-Ch		1		nC
			P-Ch		1.3		
Q_{gs}	Gate-Source Charge	P-Channel V_{DS} = -25 V, I_D = -0.34 A, V_{GS} = -10 V	N-Ch		0.19		nC
			P-Ch		0.23		
Q_{gd}	Gate-Drain Charge		N-Ch		0.33		nC
			P-Ch		0.38		
DRAIN-SOURCE DIODE CHARACTERISTICS							
I_S	Maximum Continuous Source Current		N-Ch			0.51	A
			P-Ch			-0.34	
I_{SM}	Maximum Pulse Source Current (Note 2)		N-Ch			1.5	A
			P-Ch			-1	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.51 A (Note 2)	N-Ch		0.8	1.2	V
		V_{GS} = 0 V, I_S = -0.34 A (Note 2)	P-Ch		-0.8	-1.2	

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

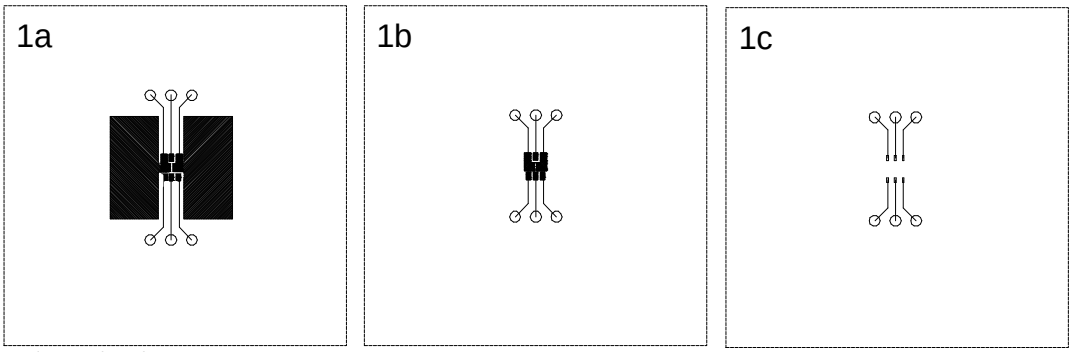
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 130°C/W when mounted on a 0.125 in^2 pad of 2oz cpper.

b. 140°C/W when mounted on a 0.005 in^2 pad of 2oz cpper.

c. 180°C/W when mounted on a 0.0015 in^2 pad of 2oz cpper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.