N-Channel 30-V (D-S) MOSFET

GENERAL DESCRIPTION

The LT4420C is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- 30V/13.5A,$R_{DS(ON)}$=13mΩ@V_{GS}=10V
- 30V/11A,$R_{DS(ON)}$=18mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

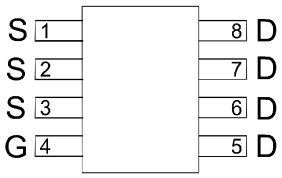
APPLICATIONS

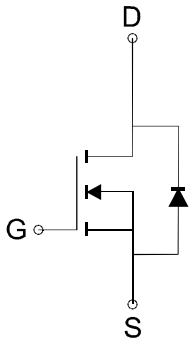
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION

(SOP-8)

Top View





N-Channel MOSFET

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DSS}	30		V
Gate-Source Voltage		V_{GSS}	±20		V
Continuous Drain Current(tJ=150℃)	T_A=25℃	I_D	13.5	9.5	A
	T_A=70℃		10.8	7.0	
Pulsed Drain Current		I_{DM}	50		A
Continuous Source Current (Diode Conduction)		I_S	2.7	1.36	A
Maximum Power Dissipation	T_A=25℃	P_D	3	1.5	W
	T_A=70℃		1.9	0.95	
Operating Junction Temperature		T_J	-55 to 150		℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	T≦10 sec	33	℃/W
			Steady State	63	
Thermal Resistance-Junction to Case		$R_{\theta JC}$	30		℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.0	2.0	3.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
		V_{DS}=30V, V_{GS}=0V T_J=55℃			5	
$I_{D(ON)}$	On-State Drain Current [a]	V_{DS}≧5V, V_{GS}= 10V	30			A
$R_{DS(ON)}$	Drain-Source On-State Resistance [a]	V_{GS}=10V, I_D= 13.5A		11	13	mΩ
		V_{GS}=4.5V, I_D= 11A		15	18	
G_{FS}	Forward Transconductance [a]	V_{DS}=15V, I_D=10A		17		S
V_{SD}	Diode Forward Voltage	I_S=2.3A, V_{GS}=0V		0.76	1.1	V
DYNAMIC						
Qg	Gate Charge	V_{DS}=15V, V_{GS}=4.5V, I_D=10A		12	14	nC
Qgt	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=10A		23	26	
Qgs	Gate-Source Charge			5		
Qgd	Gate-Drain Charge			4.9		
Ciss	Input capacitance	V_{DS}=-15V, V_{GS}=0V, f=1MHz		1100	1300	pF
Coss	Output Capacitance			250		
Crss	Reverse Transfer Capacitance			65		
Rg	Gate Resistance	f =1MHz		1.8		Ω
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=25V, R_L =25Ω I_D=1A, V_{GEN}=10V R_G=6Ω		15	18	ns
tr	Turn-On Rise Time			14	17	
$t_{d(off)}$	Turn-Off Delay Time			50	65	
tf	Turn-On Fall Time			6	8	

Notes: a. Pulse test; pulse width ≦ 300us, duty cycle≦ 2%

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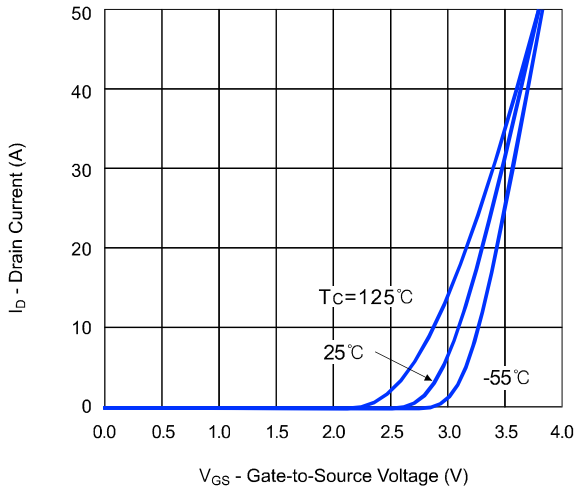
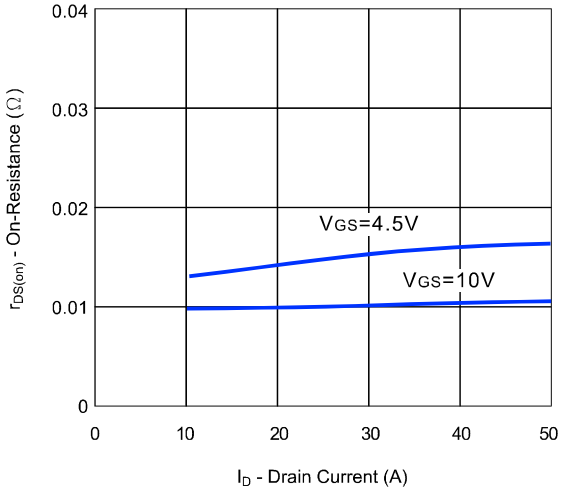
Typical Characteristics (TJ =25℃ Noted)

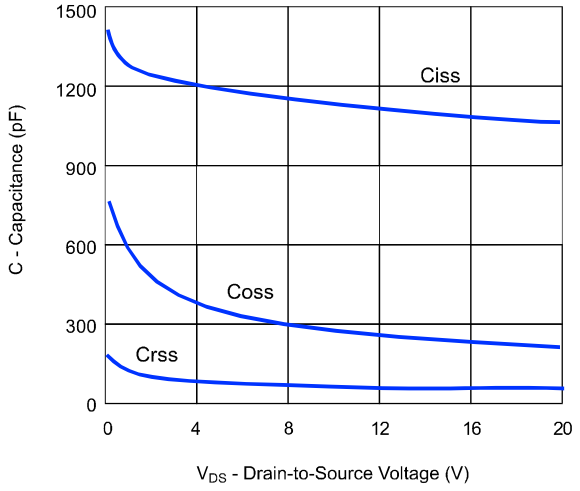
Transfer Characteristics



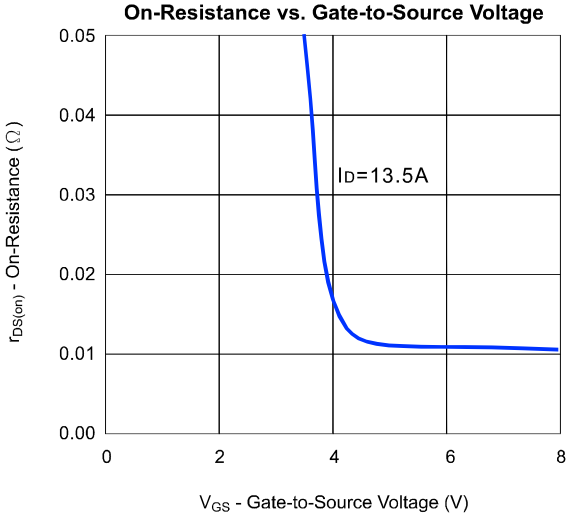
On-Resistance vs. Drain Current



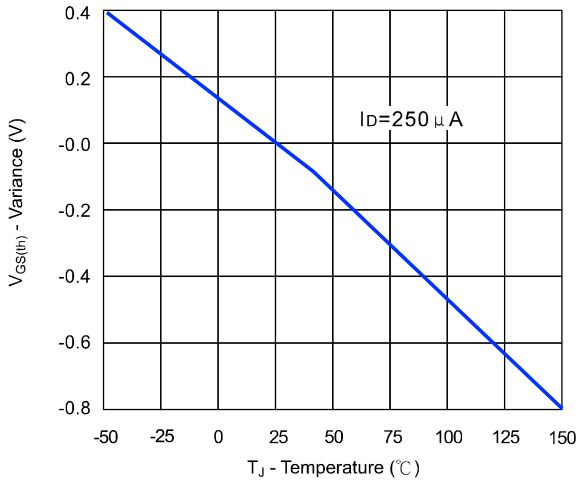
Capacitance



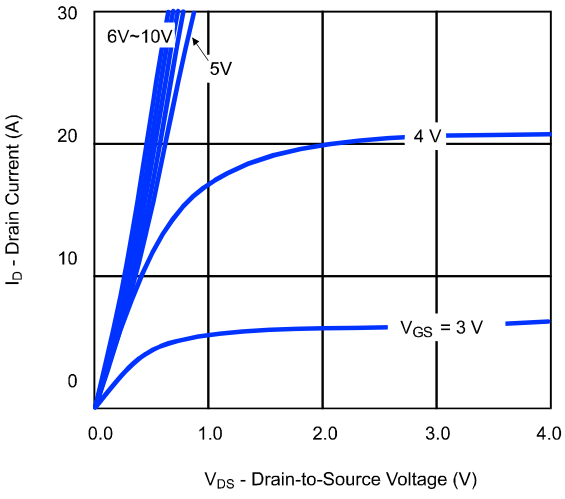
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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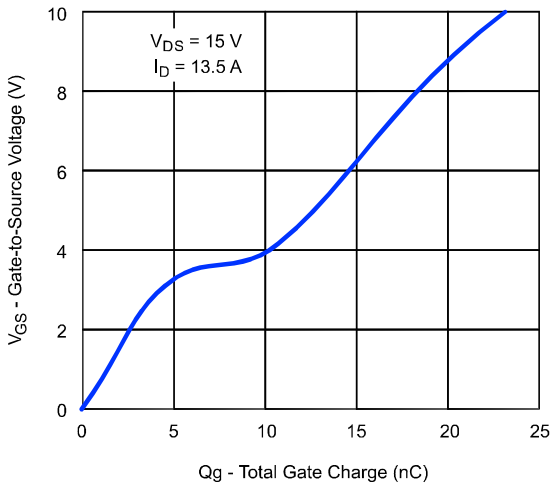
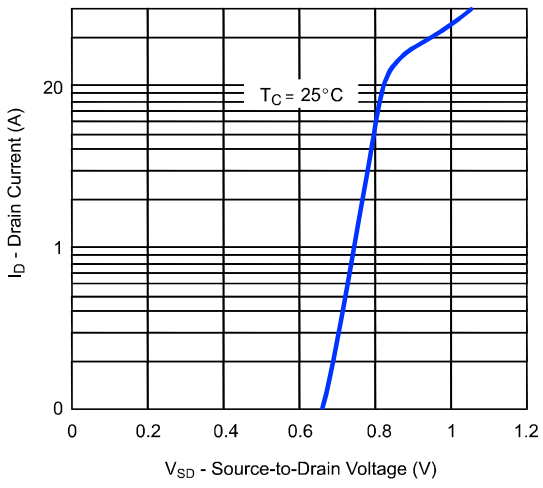
Typical Characteristics (T_J =25℃ Noted)

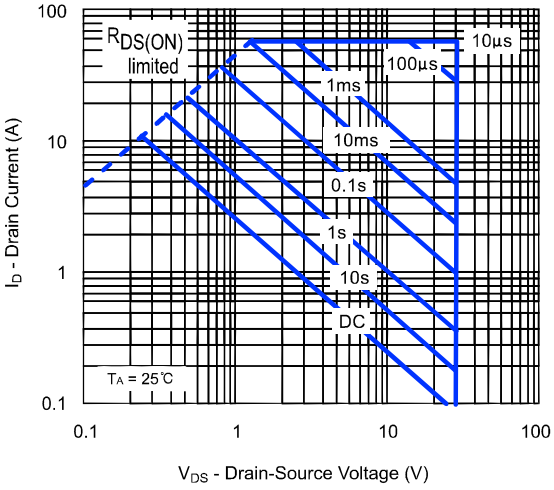
Gate Charge



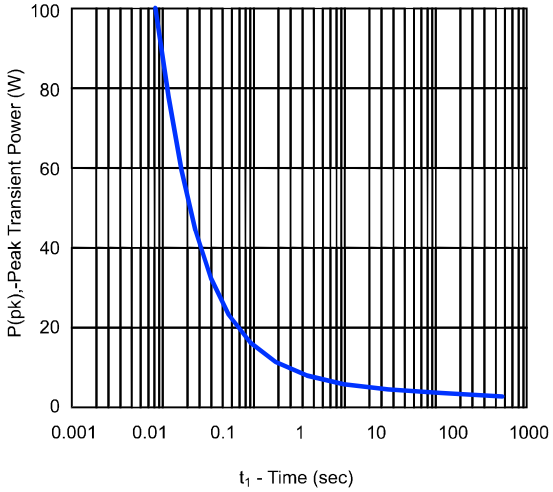
On-Resistance vs. Drain Current



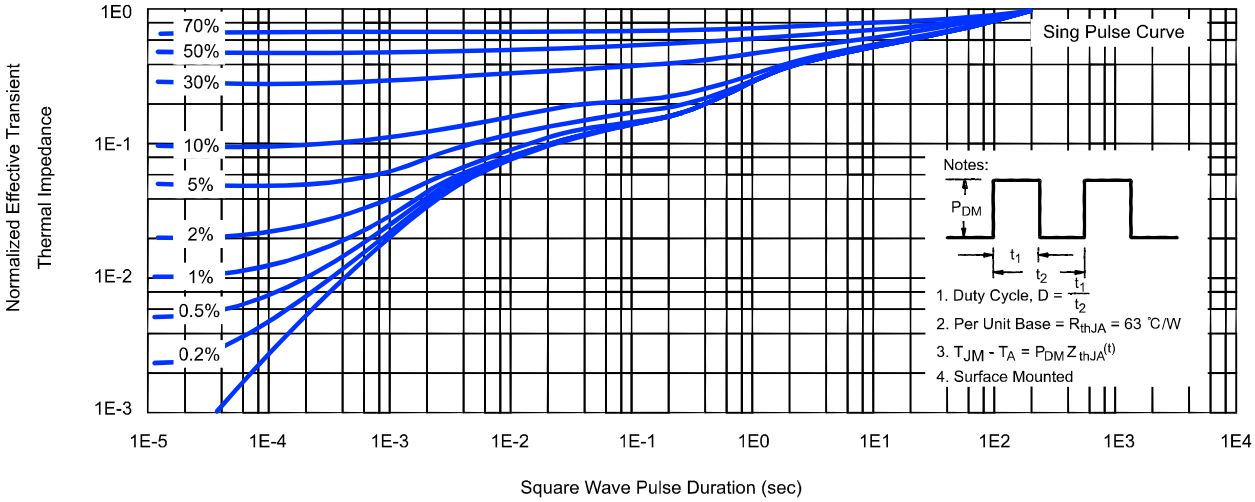
Maximum Forward Biased Safe Operating Area



Single Pulse Maximum Power Dissipation



Normalized Thermal Transient Impedance, Junction-to-Ambient



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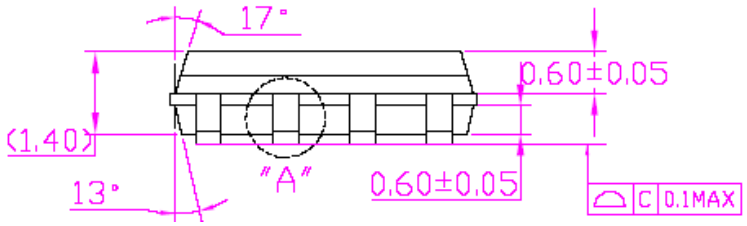
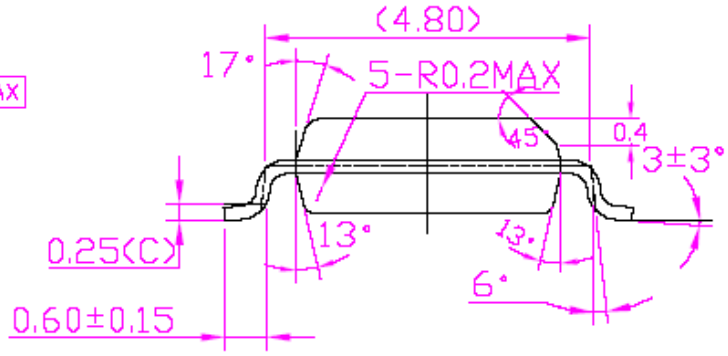
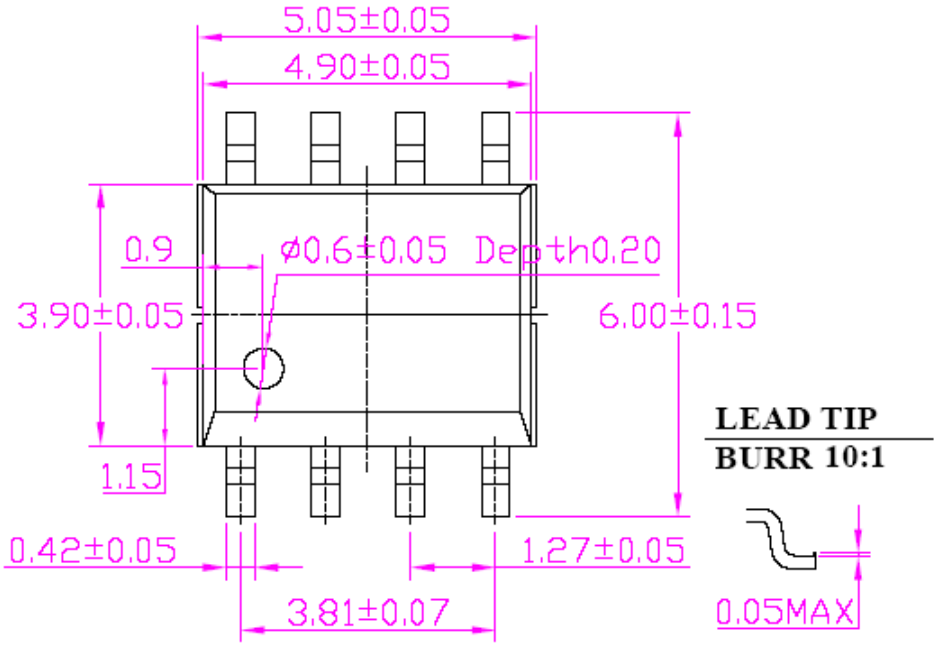
SOP-8 Package Outline



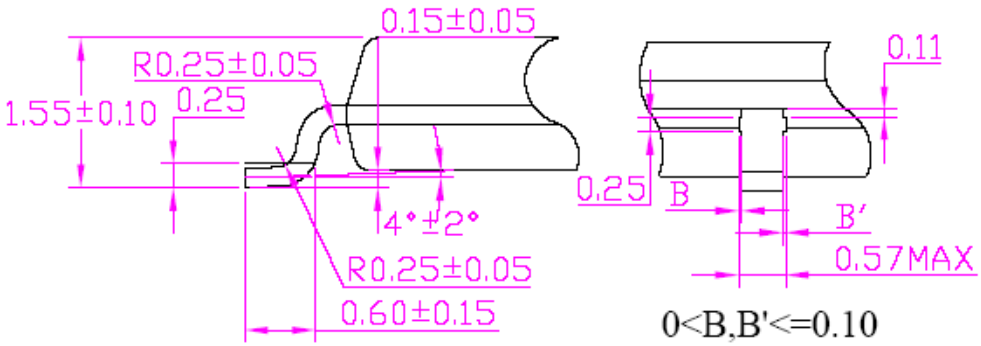


LEAD FORM
PART 15:1

"A"PART
15:1



LEAD TIP
BURR 10:1



0<B,B'<=0.10

NOTES:

1. PKG ALL SURFACES ARE Ra0.8-1.2um.

2. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both sides).

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