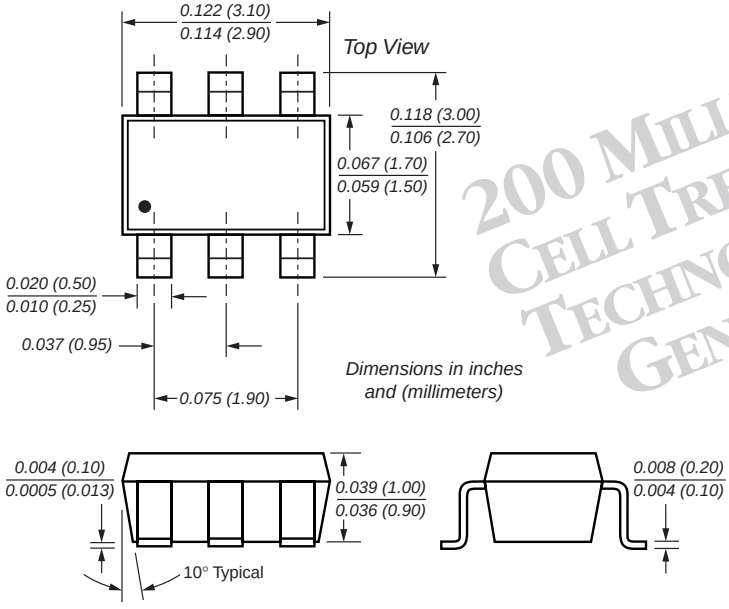
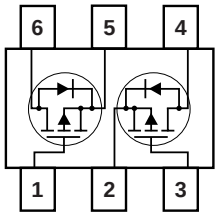
Dual P-Channel Logic Level Enhancement-Mode MOSFET

SOT-23-6L

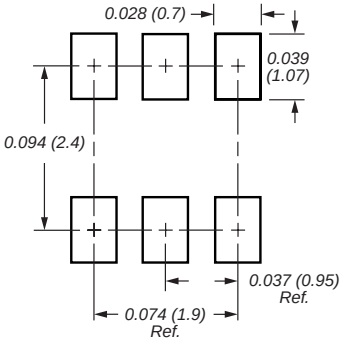
V_{DS} –20V
$R_{DS(ON)}$ 0.135Ω
I_D –2.3A



Pin Configuration (Top View)



Mounting Pad Layout



Mechanical Data

Case: SOT-23-6L package

Terminals: Leads solderable per MIL-STD-750, Method 2026

Marking Code: M3

Features

- Advanced trench process technology
- High density cell design for ultra low on-resistance
- Popular SOT-23-6L package with copper lead-frame for superior thermal and electrical capabilities
- Compact and low profile
- –1.8V rated

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

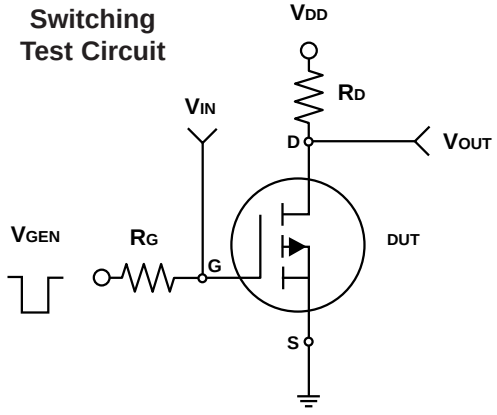
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–20	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Drain Current[2] T_J = 150°C	T_A = 25°C T_A = 70°C	I_D	–2.3 –1.8	A
Pulsed Drain Current[1]		I_{DM}	–8	
Maximum Power Dissipation[2]	T_A = 25°C T_A = 70°C	P_D	1.15 0.73	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C
Junction-to-Ambient Thermal Resistance[2]		$R_{\theta JA}$	110	°C/W

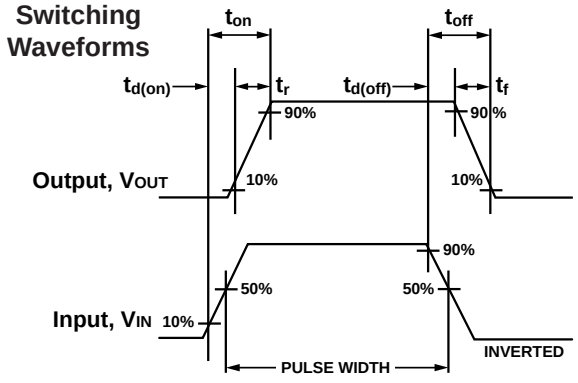
Note: (1) Pulse width limited by maximum junction temperature.
(2) Surface mounted on a 1in^2 2oz. Cu PCB (FR-4 material)

Electrical Characteristics (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = –250µA	–20	–	–	V
Breakdown Voltage Temp. Coefficient	$\Delta BV_{DSS}/\Delta T_J$	Reference to 25°C, I_D=–1mA	–	–8.8	–	mV/°C
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = –250µA	–0.45	–	–	V
Gate-Body Leakage	I_{GSS}	V_{GS} = ±8V, V_{DS} = ±0V	–	–	±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –16V, V_{GS} = 0V	–	–	–1	µA
		V_{DS}= –16V, V_{GS}=0V, T_J=85°C	–	–	–10	
On-State Drain Current(1)	$I_{D(on)}$	V_{DS} ≥ –5V, V_{GS} = –4.5V	–5	–	–	A
Drain-Source On-State Resistance(1)	$R_{DS(on)}$	V_{GS} = –4.5V, I_D = –2.3A	–	109	135	mΩ
		V_{GS} = –2.5V, I_D = –2.0A	–	146	180	
		V_{GS} = –1.8V, I_D = –1.7A	–	205	250	
Forward Transconductance(1)	g_{fs}	V_{DS} = –5V, I_D = –2.3A	–	5	–	S
Dynamic						
Total Gate Charge(1)	Q_g	V_{DS} = –10V, V_{GS} = –4.5V I_D = –2.3A	–	5.1	7.5	nC
Gate-Source Charge(1)	Q_{gs}		–	1.0	–	
Gate-Drain Charge(1)	Q_{gd}		–	1.2	–	
Turn-On Delay Time(1)	$t_{d(on)}$	V_{DD} = –8V, R_L = 8Ω I_D ≅ –1A, V_{GEN} = –4.5V R_G = 6Ω	–	7	20	ns
Turn-OnRise Time(1)	t_r		–	45	60	
Turn-Off Delay Time(1)	$t_{d(off)}$		–	162	200	
Turn-OffFall Time(1)	t_f		–	116	160	
Input Capacitance	C_{iss}	V_{DS} = –10V, V_{GS} = 0V f = 1.0MHz	–	343	–	pF
Output Capacitance	C_{oss}		–	77	–	
Reverse Transfer Capacitance	C_{rss}		–	58	–	
Source-Drain Diode						
Maximum Diode Forward Current	I_S	T_A = 25°C	–	–	–1.3	A
Maximum Pulsed Diode Forward Current(2)	I_{SM}	—	–	–	–8	A
Diode Forward Voltage(1)	V_{SD}	V_{GS} = 0V, I_S = –1.05A	–	–0.85	–1.1	V

Notes:
(1) Pulse test; pulse width ≤ 300µs, duty cycle ≤ 2%
(2) Pulse width limited by maximum junction temperature





Ratings and Characteristic Curves (T_A = 25°C unless otherwise noted)

Fig. 1 – Output Characteristics

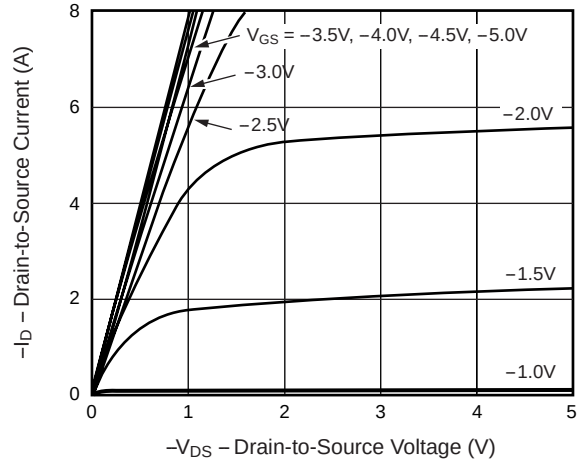


Fig. 2 – Transfer Characteristics

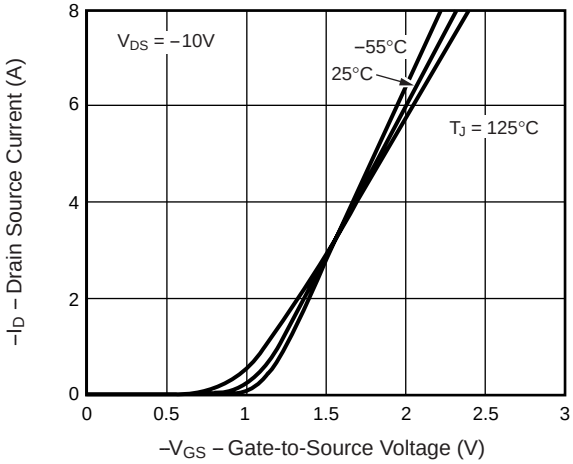


Fig. 3 – Threshold Voltage vs. Temperature

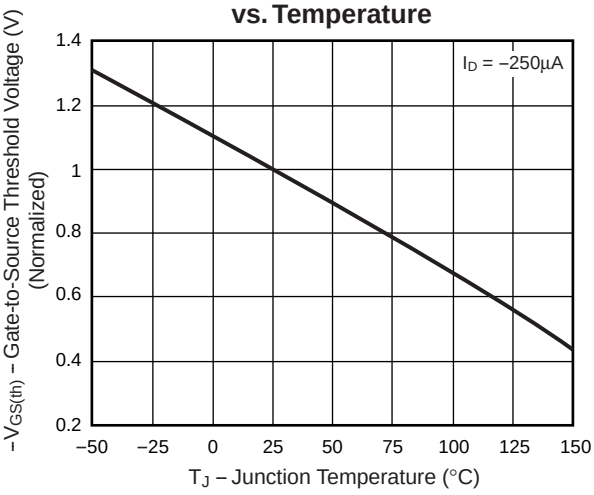


Fig. 4 – On-Resistance vs. Drain Current

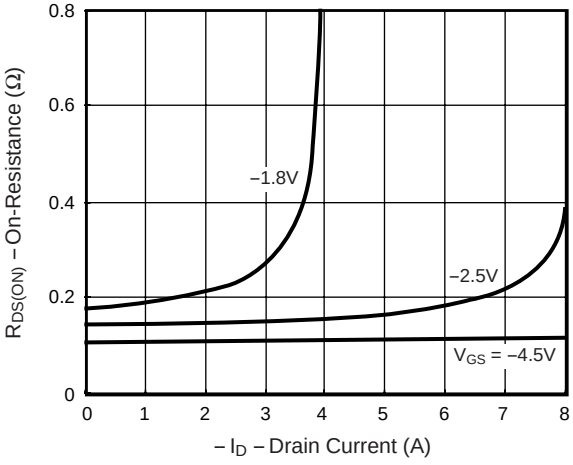


Fig. 5 – On-Resistance vs. Junction Temperature

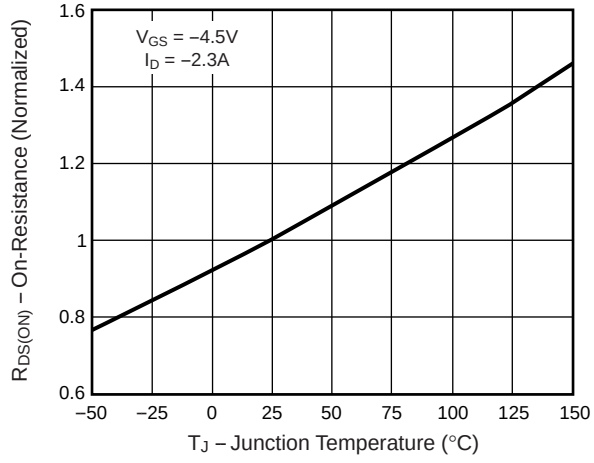
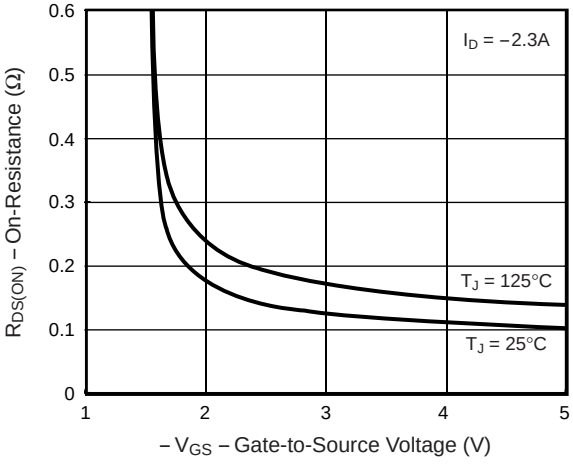


Fig. 6 – On-Resistance vs. Gate-to-Source Voltage



Ratings and Characteristic Curves (T_A = 25°C unless otherwise noted)

Fig. 7 – Gate Charge

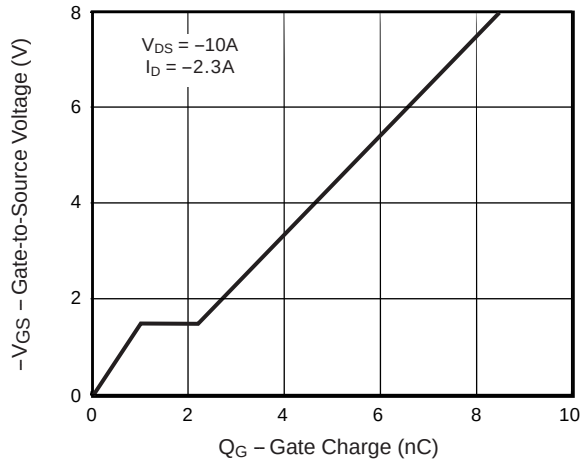


Fig. 8 – Capacitance

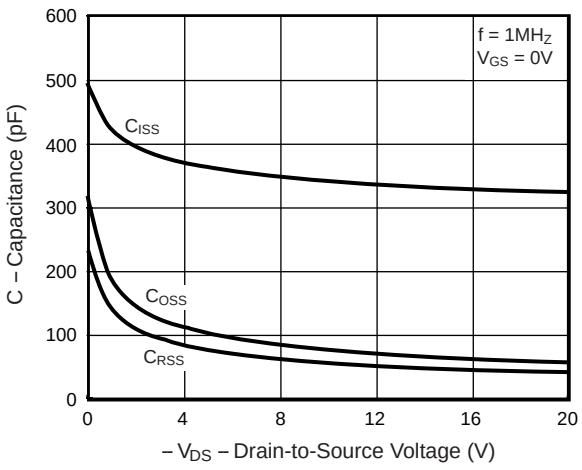


Fig. 9 – Source-Drain Diode Forward Voltage

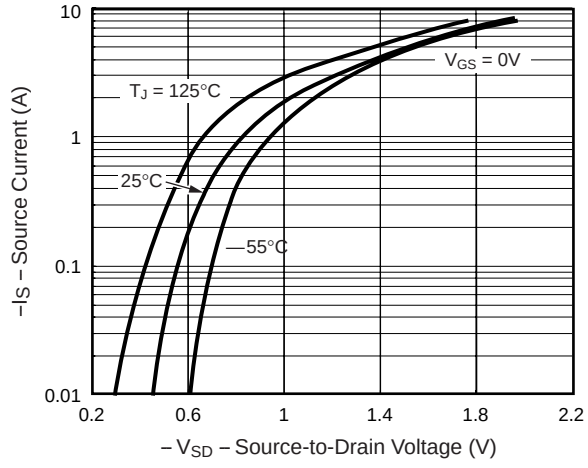


Fig. 10 – Thermal Impedance

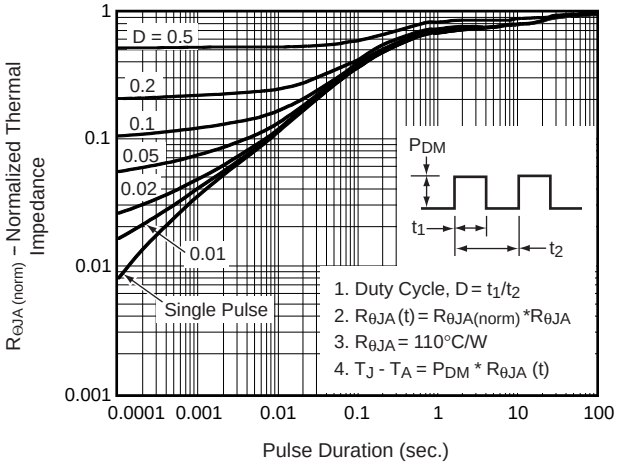


Fig. 11 – Power vs. Pulse Duration

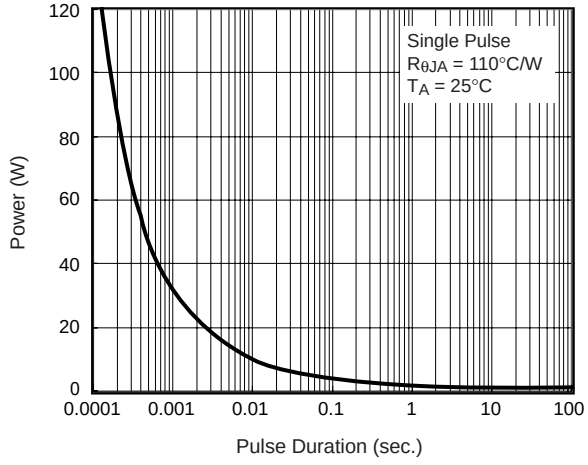


Fig. 12 – Maximum Safe Operating Area