

Transistors

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	±10	μA	$V_{GS}=\pm 10V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	–12	–	–	V	$I_D = -1mA, V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	–	–	–1	μA	$V_{DS} = -12V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	–0.3	–	–1.0	V	$V_{DS} = -6V, I_D = -1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	–	44	61	mΩ	$I_D = -2.5A, V_{GS} = -4.5V$
		–	60	84	mΩ	$I_D = -1.2A, V_{GS} = -2.5V$
		–	81	121	mΩ	$I_D = -1.2A, V_{GS} = -1.8V$
		–	110	220	mΩ	$I_D = -0.5A, V_{GS} = -1.5V$
Forward transfer admittance	$ Y_{fs} $ *	3.5	–	–	S	$V_{DS} = -6V, I_D = -2.5A$
Input capacitance	C_{iss}	–	1350	–	pF	$V_{DS} = -6V$
Output capacitance	C_{oss}	–	130	–	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	–	125	–	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$ *	–	9	–	ns	$I_D = -1.2A$
Rise time	t_r *	–	35	–	ns	$V_{DD} \approx -6V$ $V_{GS} = -4.5V$
Turn-off delay time	$t_{d(off)}$ *	–	130	–	ns	$R_L=5\Omega$
Fall time	t_f *	–	85	–	ns	$R_G=10\Omega$
Total gate charge	Q_g *	–	13	–	nC	$V_{DD} \approx -6V, I_D = -2.5A$
Gate-source charge	Q_{gs} *	–	2.5	–	nC	$V_{GS} = -4.5V$
Gate-drain charge	Q_{gd} *	–	2.0	–	nC	$R_L \approx 2.4\Omega, R_G=10\Omega$

*Pulsed

●Body diode characteristics(Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	–	–	–1.2	V	$I_S = -2.5A, V_{GS}=0V$

* Pulsed

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●Electrical characteristic curves

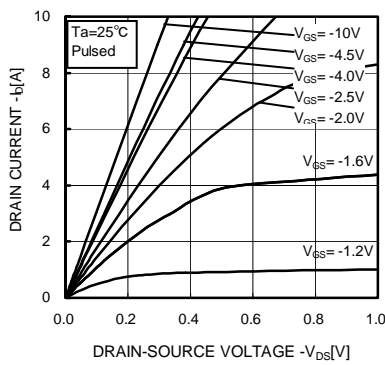


Fig.1 Typical Output Characteristics (I)

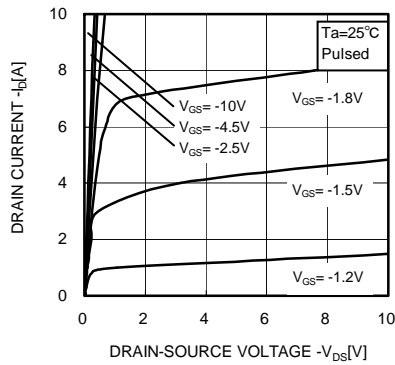


Fig.2 Typical Output Characteristics (II)

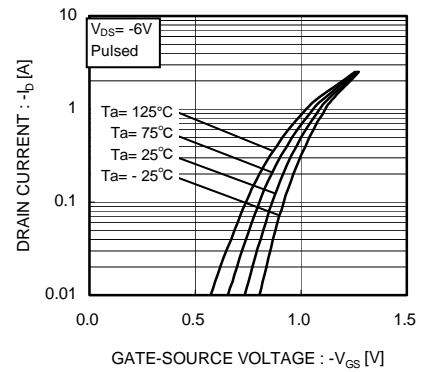


Fig.3 Typical Transfer Characteristics

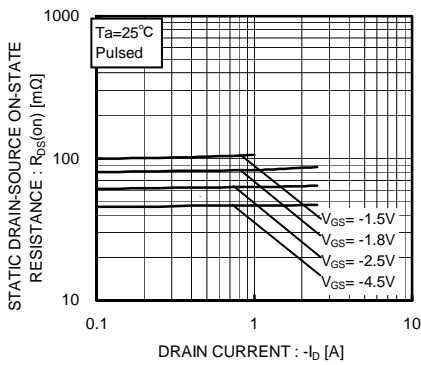


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (I)

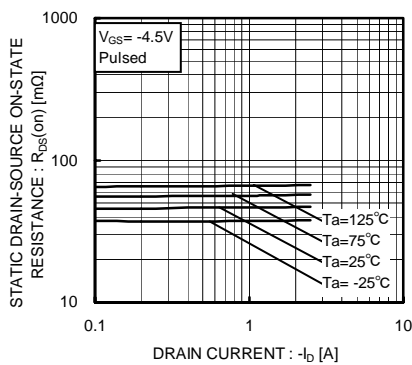


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current (II)

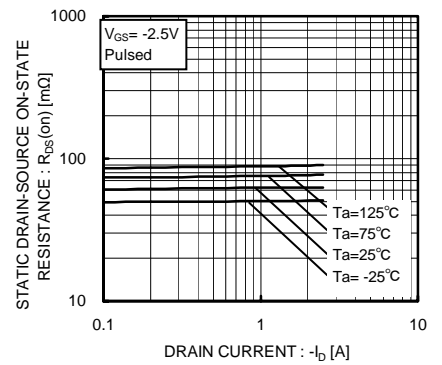


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current (III)

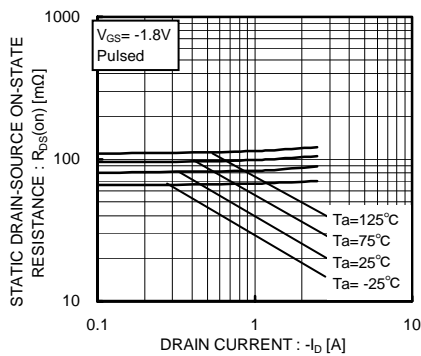


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (IV)

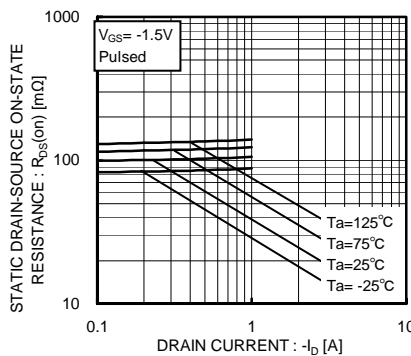


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (IV)

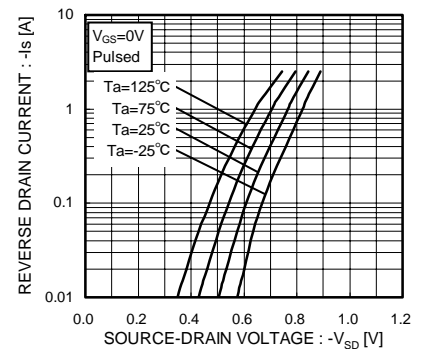


Fig.9 Reverse Drain Current vs. Source-Drain Voltage

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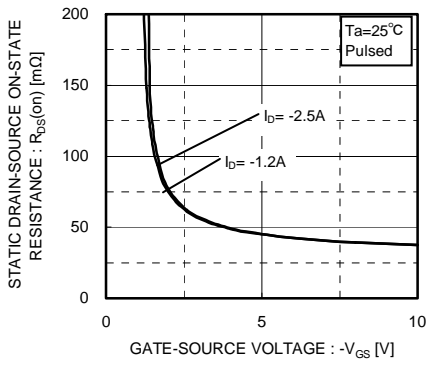


Fig.10 Static Drain-Source On-State Resistance vs. Gate Source Voltage

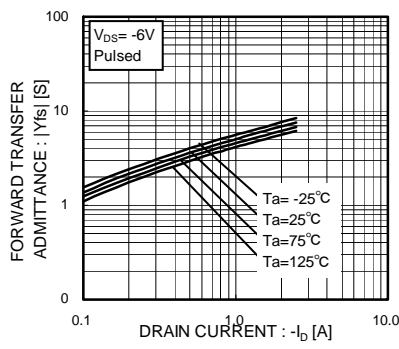


Fig.11 Forward Transfer Admittance vs. Drain Current

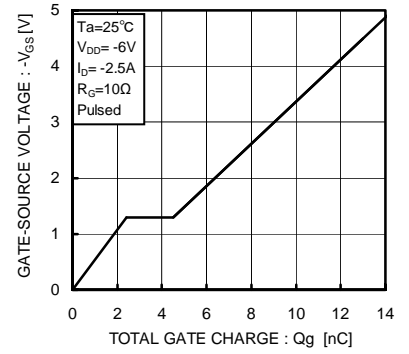


Fig.12 Dynamic Input Characteristics

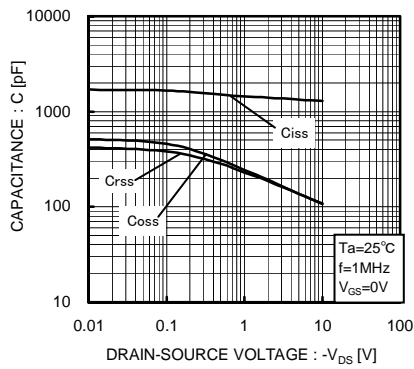


Fig.13 Typical Capacitance vs. Drain-Source Voltage

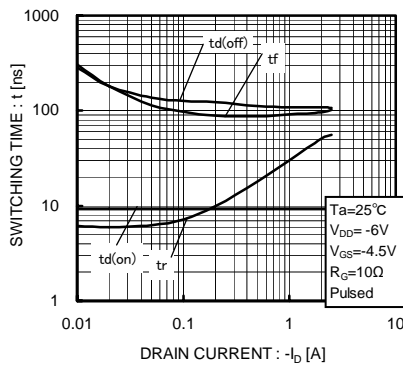


Fig.14 Switching Characteristics

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●Measurement circuits

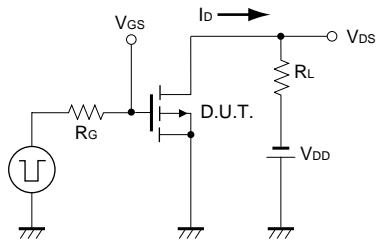


Fig.15 Switching Time Test Circuit

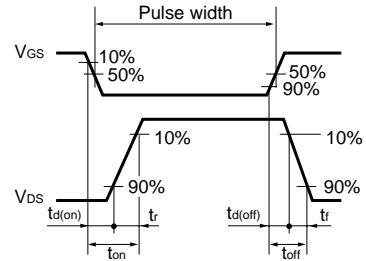


Fig.16 Switching Time Waveforms

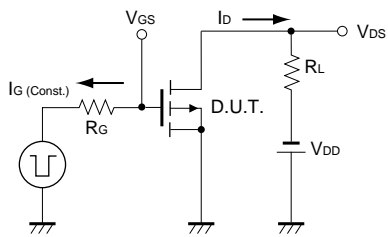


Fig.17 Gate Charge Test Circuit

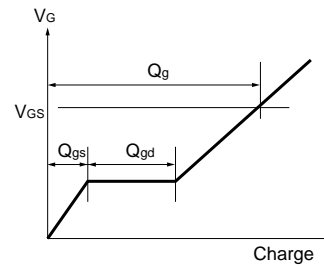


Fig.18 Gate Charge Waveform

●Notice

This product might cause chip aging and breakdown under the large electrified environment.
Please consider to design ESD protection circuit.

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