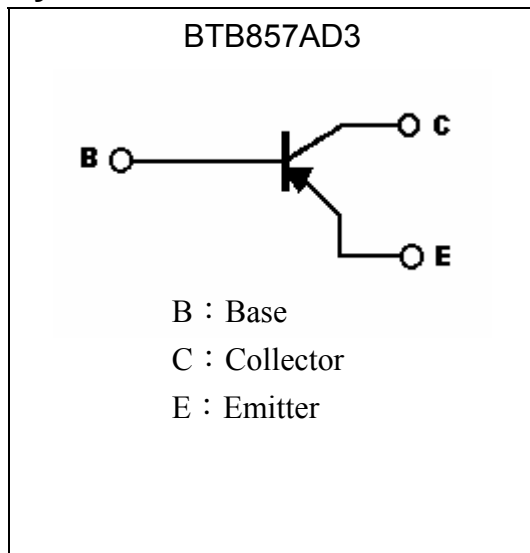
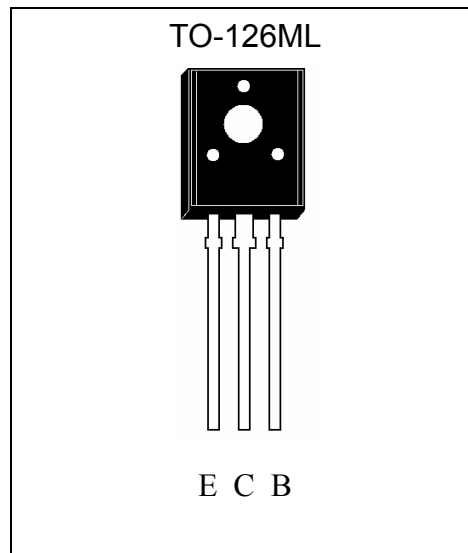


**Low Vcesat PNP Epitaxial Planar Transistor**

# BTB857AD3

**Features**

- Low  $V_{CE(sat)}$ ,  $V_{CE(sat)} = -0.15V$  (typical), at  $I_C / I_B = -2A / -0.2A$
- Excellent DC current gain characteristics
- Wide SOA
- RoHS compliant package

**Symbol**

**Outline**

**Absolute Maximum Ratings** ( $T_a = 25^\circ C$ )

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	$V_{CBO}$	-180	V
Collector-Emitter Voltage	$V_{CEO}$	-140	V
Emitter-Base Voltage	$V_{EBO}$	-6	V
Collector Current	$I_C(DC)$	-5	A
	$I_C(Pulse)$	-8 *1	
Power Dissipation	$P_d(T_a = 25^\circ C)$	1.5	W
	$P_d(T_c = 25^\circ C)$	20	
Junction Temperature	$T_j$	150	$^\circ C$
Storage Temperature	$T_{stg}$	-55~+150	$^\circ C$

 Note : \*1. Single Pulse  $P_w = 10ms$

**Characteristics (Ta=25°C)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV <sub>CBO</sub>	-180	-210	-	V	I <sub>C</sub> =-50μA, I <sub>E</sub> =0
BV <sub>CEO</sub>	-140	-170	-	V	I <sub>C</sub> =-10mA, I <sub>B</sub> =0
BV <sub>EBO</sub>	-6	-8	-	V	I <sub>E</sub> =-50μA, I <sub>C</sub> =0
I <sub>CBO</sub>	-	-	-50	nA	V <sub>CB</sub> =-150V, I <sub>E</sub> =0
I <sub>CEO</sub>	-	-	-10	μA	V <sub>CE</sub> =-140V, I <sub>B</sub> =0
I <sub>EBO</sub>	-	-	-50	nA	V <sub>EB</sub> =-6V, I <sub>C</sub> =0
*V <sub>CE(sat)</sub>	-	-0.11	-0.15	V	I <sub>C</sub> =-1A, I <sub>B</sub> =-100mA
*V <sub>CE(sat)</sub>	-	-0.15	-0.3	V	I <sub>C</sub> =-2A, I <sub>B</sub> =-200mA
*V <sub>CE(sat)</sub>	-	-0.27	-0.37	V	I <sub>C</sub> =-3A, I <sub>B</sub> =-300mA
*V <sub>BE(sat)</sub>	-	-	-1.2	V	I <sub>C</sub> =-2A, I <sub>B</sub> =-200mA
*h <sub>FE 1</sub>	180	-	390	-	V <sub>CE</sub> =-3V, I <sub>C</sub> =-500mA
*h <sub>FE 2</sub>	120	-	-	-	V <sub>CE</sub> =-2V, I <sub>C</sub> =-1A
f <sub>T</sub>	-	15	-	MHz	V <sub>CE</sub> =-5V, I <sub>C</sub> =-500mA, f=100MHz

\*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

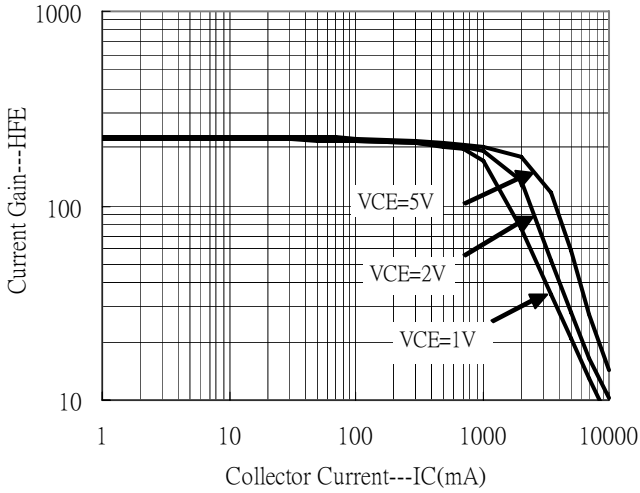
**Ordering Information**

Device	Package	Shipping
BTB857AD3	TO-126ML (RoHS compliant)	200 pcs / bag, 15 bags/box, 10 boxes/carton

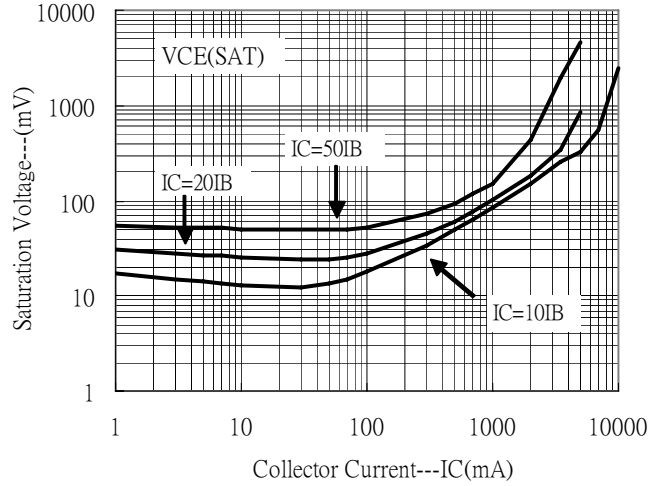


### Characteristic Curves

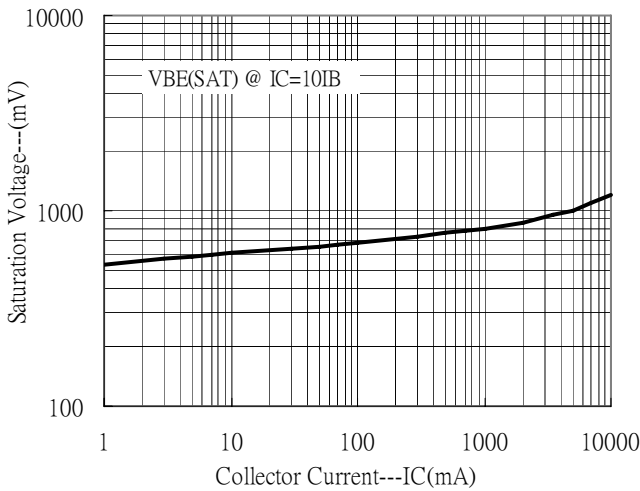
Current Gain vs Collector Current



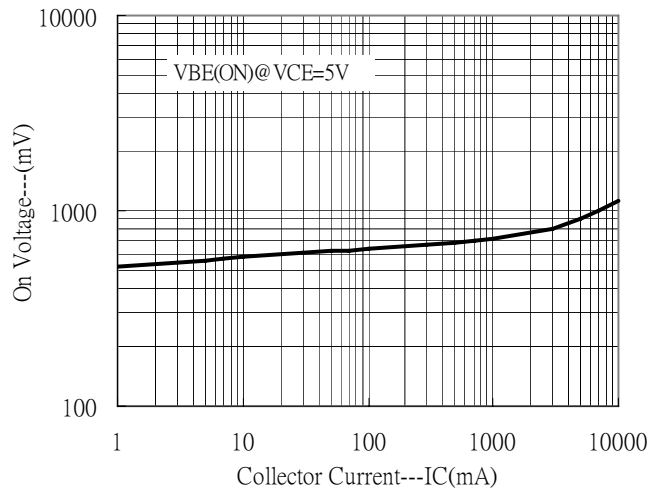
Saturation Voltage vs Collector Current



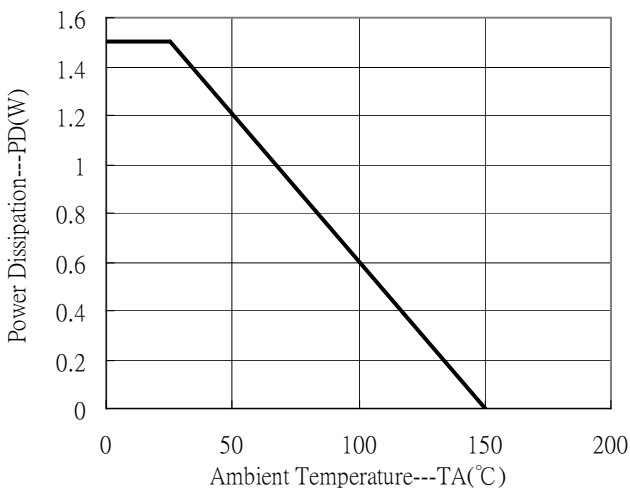
Saturation Voltage vs Collector Current



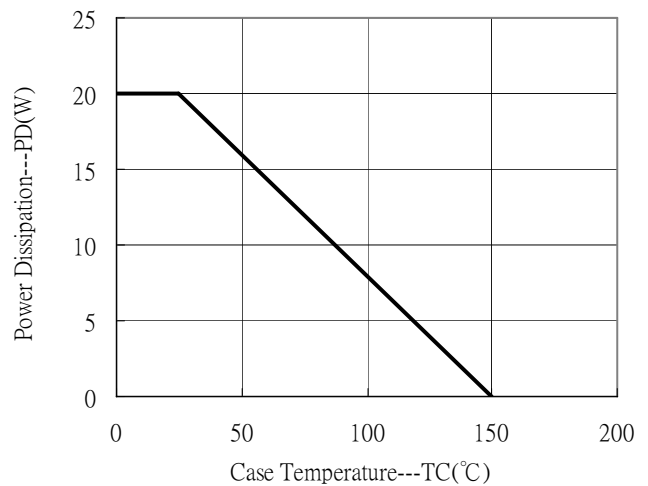
On Voltage vs Collector Current



Power Derating Curve



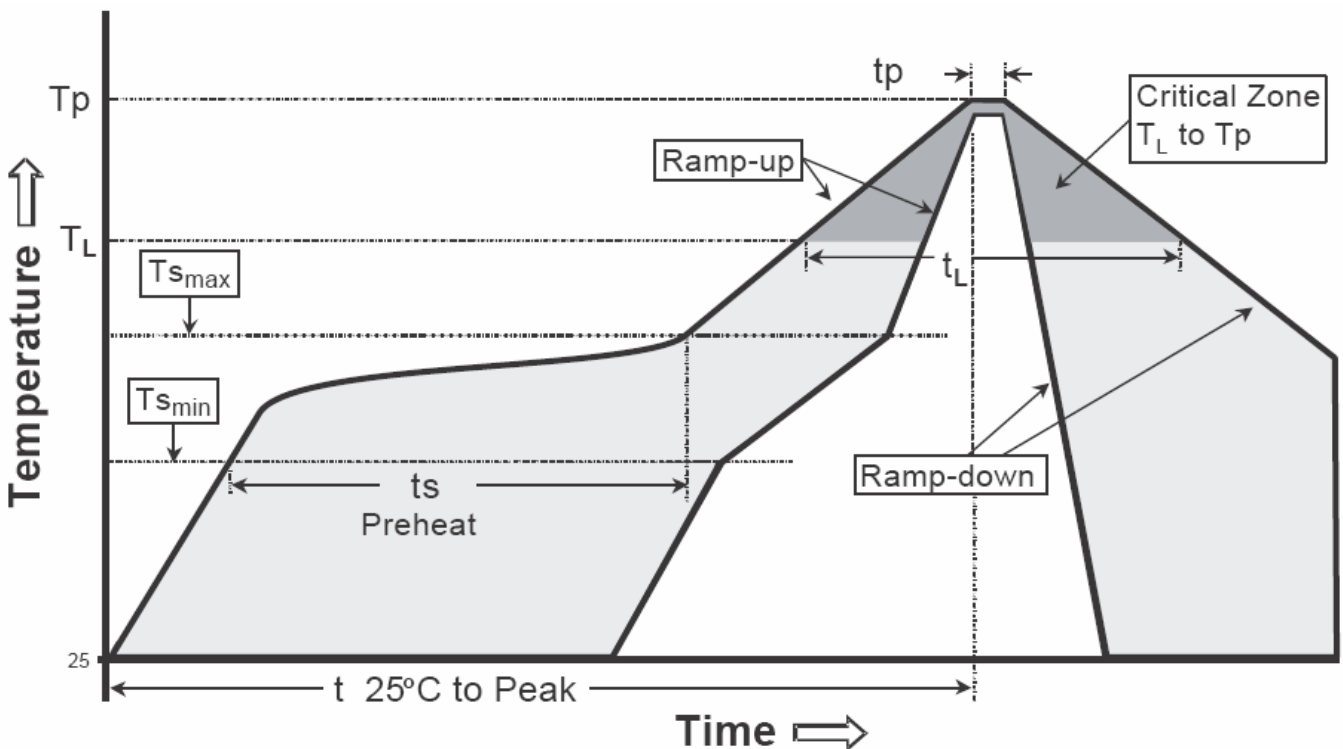
Power Derating Curve



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

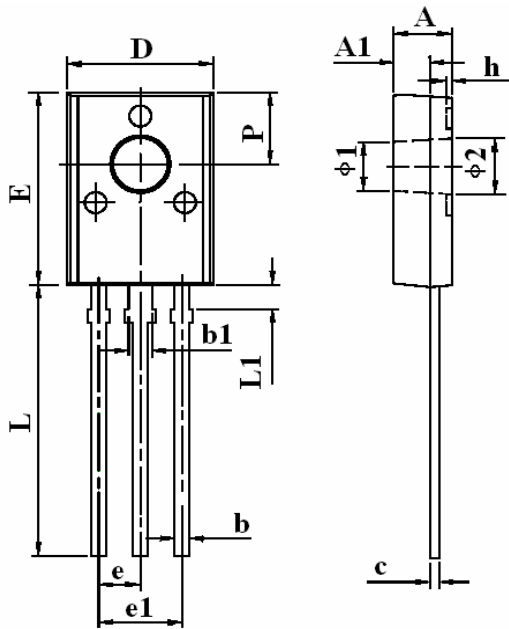
**Recommended temperature profile for IR reflow**



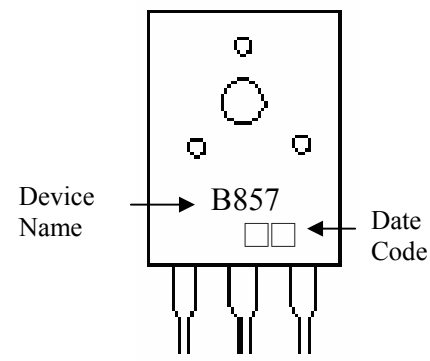
Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T <sub>s min</sub> )	100°C	150°C
-Temperature Max(T <sub>s max</sub> )	150°C	200°C
-Time(t <sub>s min</sub> to t <sub>s max</sub> )	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T <sub>L</sub> )	183°C	217°C
- Time (t <sub>L</sub> )	60-150 seconds	60-150 seconds
Peak Temperature(T <sub>P</sub> )	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

**TO-126ML Dimension**



Marking:



Device Name → B857 ← Date Code

Style: Pin 1. Emitter 2. Collector 3. Base

3-Lead TO-126ML Plastic Package  
 CYStek Package Code: D3

\*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.118	0.134	3.000	3.400	e	*0.090		*2.28	
A1	0.071	0.087	1.800	2.200	e1	0.176	0.183	4.460	4.660
b	0.026	0.034	0.660	0.860	L	0.594	0.610	15.100	15.500
b1	0.046	0.054	1.170	1.370	L1	0.051	0.059	1.300	1.500
c	0.018	0.024	0.450	0.600	P	0.159	0.167	4.040	4.240
D	0.307	0.323	7.800	8.200	Φ <sub>1</sub>	0.118	0.126	3.000	3.200
E	0.425	0.441	10.800	11.200	Φ <sub>2</sub>	0.122	0.130	3.100	3.300

Notes: 1. Controlling dimension: millimeters.  
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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