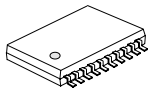
U74HC540

CMOS IC

OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS



TSSOP-20

*Pb-free plating product number:
U74HC540L

■ DESCRIPTION

The U74HC540 combines with octal buffers and line drivers with inverting 3-tate outputs. The 3-state output is controlled by output enable inputs $\overline{OE1}$ and $\overline{OE2}$, all eight outputs will be in high-impedance when either of the 2 inputs is applied with high voltage.

■ FEATURES

* Operation voltage range: 2V ~ 6V
* High-current 3-state outputs for bus driver
* Inverting outputs

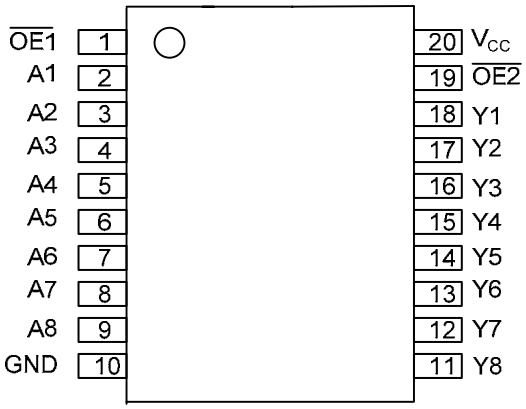
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Normal	Lead Free Plating		
U74HC540-P20-R	U74HC540L-P20-R	TSSOP-20	Tape Reel
U74HC540-P20-T	U74HC540L-P20-T	TSSOP-20	Tube

U74HC540L-P20-R
(1)Packing Type
(2)Package Type
(3)Lead Plating

(1) R: Tape Reel, T: Tube
(2) P20: TSSOP-20
(3) L: Lead Free Plating, Blank: Pb/Sn

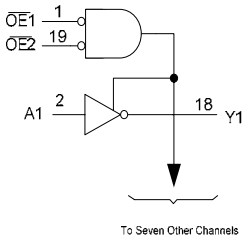
■ PIN CONFIGURATION

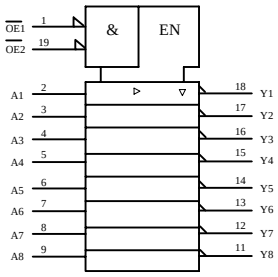


■ FUNCTION TABLE (each gate)

INPUT			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

■ LOGIC DIAGRAM (positive logic)





■ ABSOLUTE MAXIMUM RATINGS (unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5~7	V
Input Clamp Current	I_{IK}	±20	mA
Output Clamp Current	I_{OK}	±20	mA
Output Current	I_{OUT}	±35	mA
V_{CC} or GND Current	I_{CC}	±70	mA
Storage Temperature	T_{STG}	-65 ~ +150	℃

Note 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2	5	6	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise or Fall Rate	t_R, t_F	V_{CC}=2V	0		1000	ns
		V_{CC}=4.5V	0		500	
		V_{CC}=6V	0		400	
Operating Temperature	T_A		-40		85	℃

■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	T_A =25°C			-40~85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
High-Level Input Voltage	V_{IH}	V_{CC}=2V				1.5		V
		V_{CC}=4.5V				3.15		
		V_{CC}=6V				4.2		
Low-Level Input Voltage	V_{IL}	V_{CC}=2V					0.5	V
		V_{CC}=4.5V					1.35	
		V_{CC}=6V					1.8	
High-Level Output Voltage	V_{OH}	V_{CC}=2V, I_{OH}=-20μA	1.9	1.998		1.9		V
		V_{CC}=4.5V, I_{OH}=-20μA	4.4	4.499		4.4		
		V_{CC}=6V, I_{OH}=-20μA	5.9	5.999		5.9		
		V_{CC}=4.5V, I_{OH}=-6mA	3.98	4.3		3.84		
		V_{CC}=6V, I_{OH}=-7.8mA	5.48	5.8		5.34		
Low-Level Output Voltage	V_{OL}	V_{CC}=2V, I_{OH}=20μA		0.002	0.1		0.1	V
		V_{CC}=4.5V, I_{OH}=20μA		0.001	0.1		0.1	
		V_{CC}=6V, I_{OH}=20μA		0.001	0.1		0.1	
		V_{CC}=4.5V, I_{OL} =6mA		0.17	0.26		0.33	
		V_{CC}=6V, I_{OL} =7.8mA		0.15	0.26		0.33	
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=6V, V_{IN}=V_{CC} or GND		±0.1	±100		±1000	nA
Output Leakage Current	$I_{O(LEAK)}$	V_{CC}=6V, V_{OUT}=V_{CC} or GND		±0.01	±0.5		±5	uA
Quiescent Supply Current	I_Q	V_{CC}=6V, V_{IN}=V_{CC} or GND, I_{OUT}=0			8		80	μA
Input Capacitance	C_{IN}	V_{CC}=2V~6V		3	10		10	pF

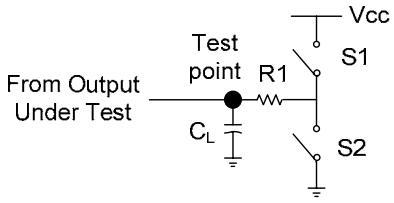
■ SWITCHING CHARACTERISTICS (t_R, t_F≤3ns)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A=25°C			-40~85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
Propagation delay from input (A) to output(Y)	t_{PLH}/ t_{PHL}	V_{CC}=2V, C_L=50 pF		35	100		125	ns
		V_{CC}=2V, C_L=150 pF		60	150		188	
		V_{CC}=4.5V, C_L=50 pF		10	20		25	
		V_{CC}=4.5V, C_L=150 pF		15	30		38	
		V_{CC}=6V, C_L=50 pF		8	17		21	
		V_{CC}=6V, C_L=150 pF		13	26		32	
3-state output enable time from $\overline{OE}$ to Yn	t_{PZH}/ t_{PZL}	V_{CC}=2V, C_L=50 pF		75	150		188	ns
		V_{CC}=2V, C_L=150 pF		100	200		250	
		V_{CC}=4.5V, C_L=50 pF		15	30		38	
		V_{CC}=4.5V, C_L=150 pF		20	40		50	
		V_{CC}=6V, C_L=50 pF		13	26		32	
		V_{CC}=6V, C_L=150 pF		17	34		43	
3-state output disable time from $\overline{OE}$ to Yn	t_{PHZ}/ t_{PLZ}	V_{CC}=2V, C_L=50 pF		40	150		188	ns
		V_{CC}=4.5V, C_L=50 pF		18	30		38	
		V_{CC}=6V, C_L=50 pF		17	26		32	

■ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	Cpd	No load, f=1MHz		35		pF

■ TEST CIRCUIT AND WAVEFORMS



Note: C_L includes probe and jig capacitance.