



SPN09T10

N-Channel Enhancement Mode MOSFET

DESCRIPTION	APPLICATIONS		
<p>The SPN09T10 is the N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPN09T10 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.</p>	<ul style="list-style-type: none"> ● Powered System ● DC/DC Converter ● Load Switch 		
FEATURES	PIN CONFIGURATION		
<ul style="list-style-type: none"> ◆ 100V/8A, $R_{DS(ON)} = 160m\Omega @ V_{GS} = 10V$ ◆ High density cell design for extremely low $R_{DS(ON)}$ ◆ Exceptional on-resistance and maximum DC current capability ◆ TO-252, TO-251, TO-263 package design 	TO-252	TO-251	TO-263
	PART MARKING		
	<p>A : Lot Code B : Date Code</p>	<p>A : Lot Code B : Date Code</p>	<p>A : Lot Code B : Date Code</p>



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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN09T10T252RGB	TO-252	SPN09T10
SPN09T10T251TGB	TO-251	SPN09T10
SPN09T10T263TGB	TO-263	SPN09T10

※ SPN09T10T252RGB : Tape Reel ; Pb – Free ; Halogen - Free

※ SPN09T10T251RGB : Tube ; Pb – Free ; Halogen - Free

※ SPN09T10T263RGB : Tube ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V_{DSS}	100	V
Gate –Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current($T_J=150^{\circ}\text{C}$)	I_D	$T_A=25^{\circ}\text{C}$	14
		$T_A=70^{\circ}\text{C}$	9.0
Pulsed Drain Current	I_{DM}	45	A
Avalanche Current	I_{AS}	14	A
Power Dissipation	P_D	$T_A=25^{\circ}\text{C}$ TO-252-2L	40
		TO-251	55
Avalanche Energy with Single Pulse ($T_J=25^{\circ}\text{C}$, $L = 0.14\text{mH}$, $I_{AS} = 20\text{A}$, $V_{DD} = 20\text{V}$.)	E_{AS}	28	mJ
Operating Junction Temperature	T_J	-55/150	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	-55/150	$^{\circ}\text{C}$
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	100	$^{\circ}\text{C}/\text{W}$



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ELECTRICAL CHARACTERISTICS

($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1		3	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V$			25	uA
		$V_{DS}=80V, V_{GS}=0V$ $T_J=125^{\circ}\text{C}$			250	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq 5V, V_{GS}=10V$	9			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=10A$		0.110	0.160	Ω
Forward Transconductance	g_{fs}	$V_{DS}=10V, I_D=5A$		5.6		S
Diode Forward Voltage	V_{SD}	$I_S=9A, V_{GS}=0V$			1.3	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=80V, V_{GS}=10V$ $I_D=5A$		10	16	nC
Gate-Source Charge	Q_{gs}			2.5		
Gate-Drain Charge	Q_{gd}			4.5		
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V$ $f=1\text{MHz}$		430		pF
Output Capacitance	C_{oss}			56		
Reverse Transfer Capacitance	C_{rss}			35		
Turn-On Time	$t_{d(on)}$	$V_{DD}=50V, R_L=10\Omega$ $I_D=5A, V_{GEN}=10V$ $R_G=3.3\Omega$		6.5		nS
	t_r			10		
Turn-Off Time	$t_{d(off)}$			13		
	t_f			3.4		



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TYPICAL CHARACTERISTICS

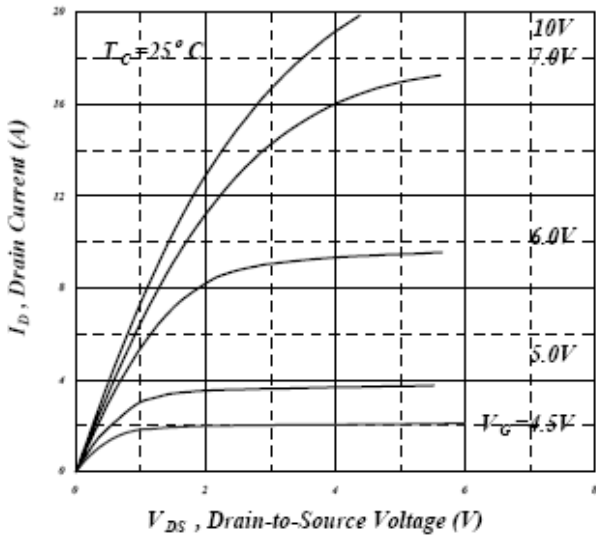


Fig 1. Typical Output Characteristics

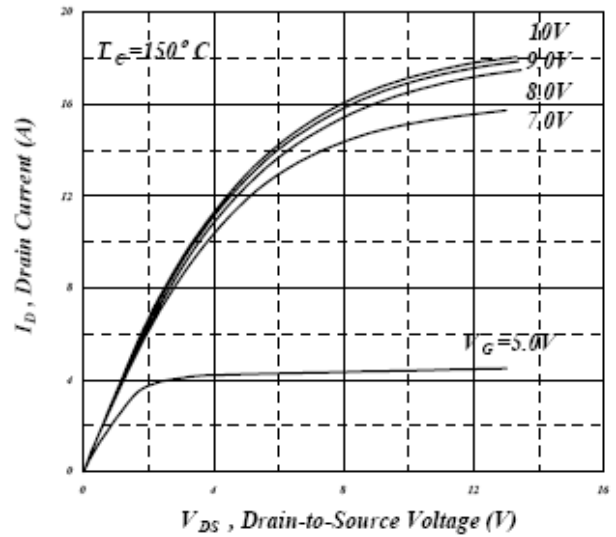


Fig 2. Typical Output Characteristics

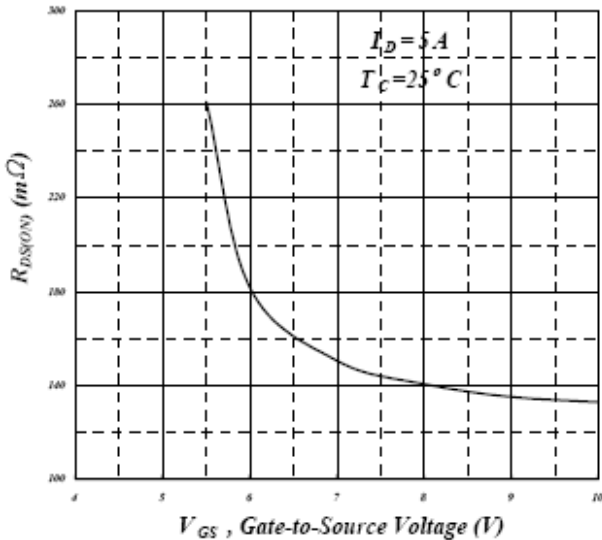


Fig 3. On-Resistance v.s. Gate Voltage

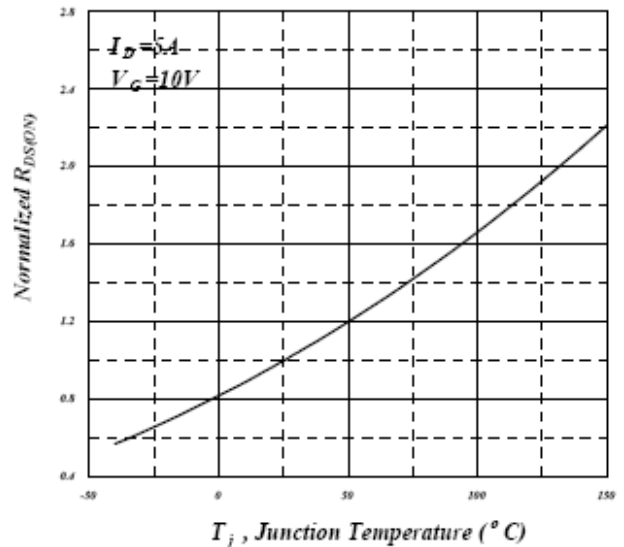


Fig 4. Normalized On-Resistance
v.s. Junction Temperature



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TYPICAL CHARACTERISTICS

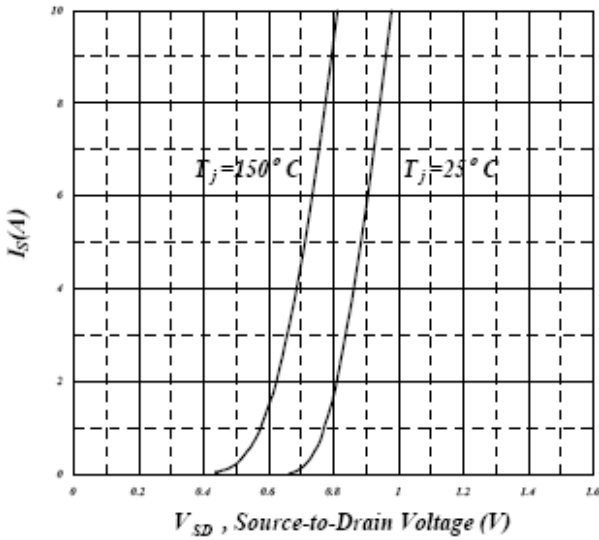


Fig 5. Forward Characteristic of Reverse Diode

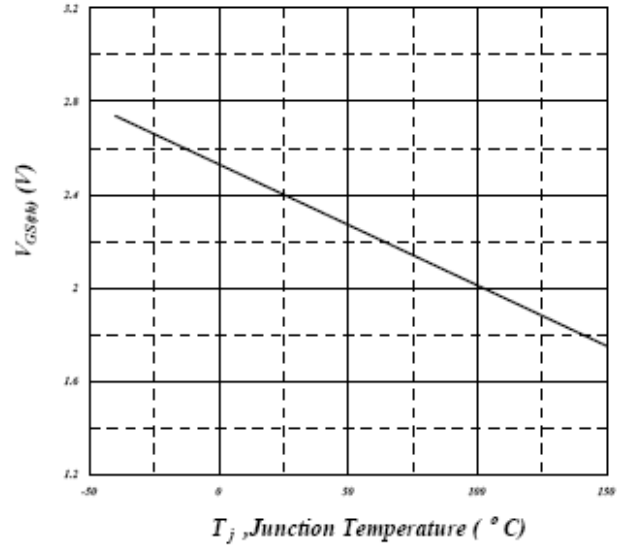


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

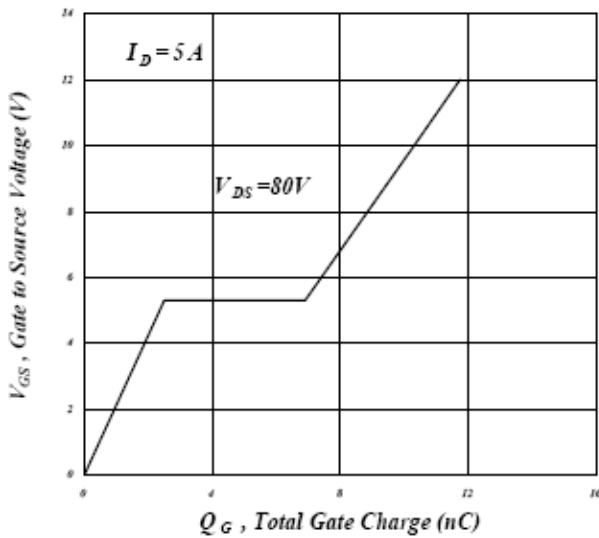


Fig 7. Gate Charge Characteristics

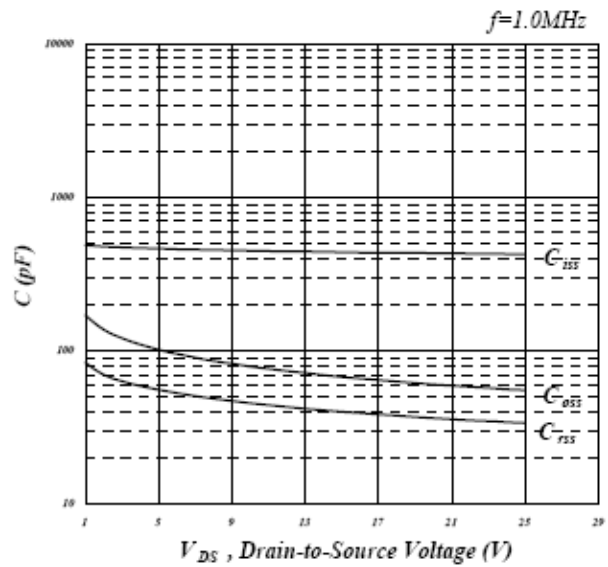


Fig 8. Typical Capacitance Characteristics



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TYPICAL CHARACTERISTICS

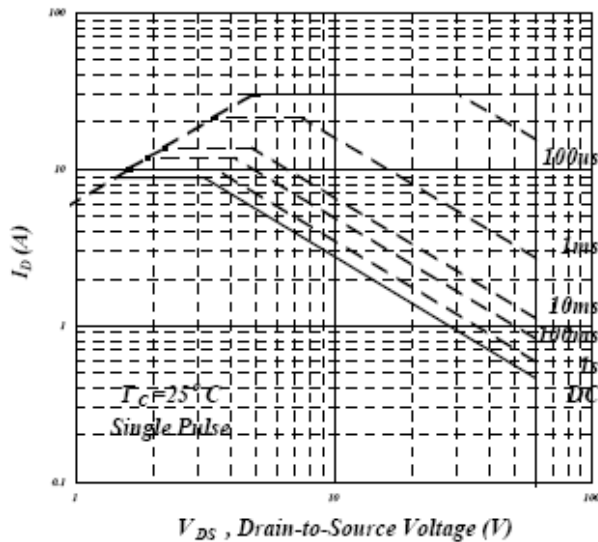


Fig 9. Maximum Safe Operating Area

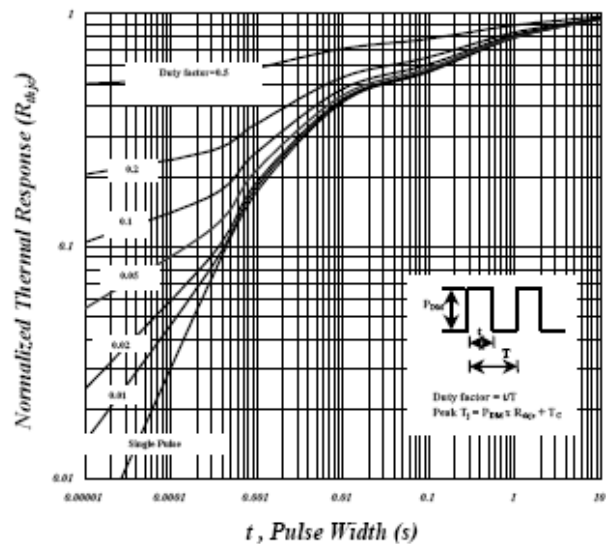


Fig 10. Effective Transient Thermal Impedance

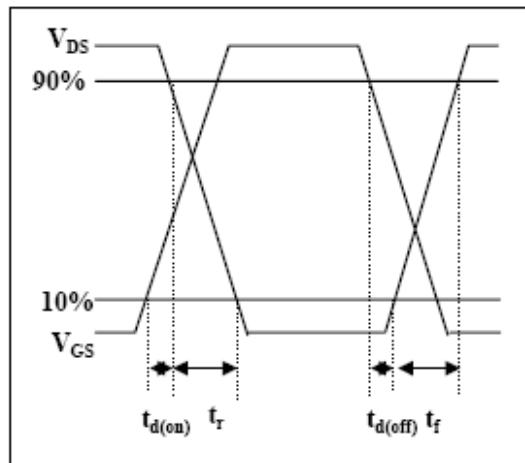


Fig 11. Switching Time Waveform

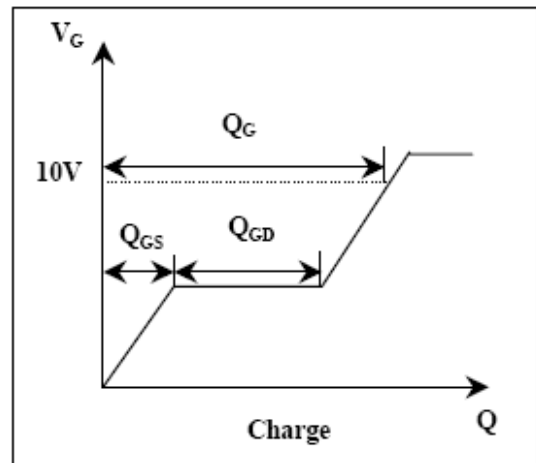


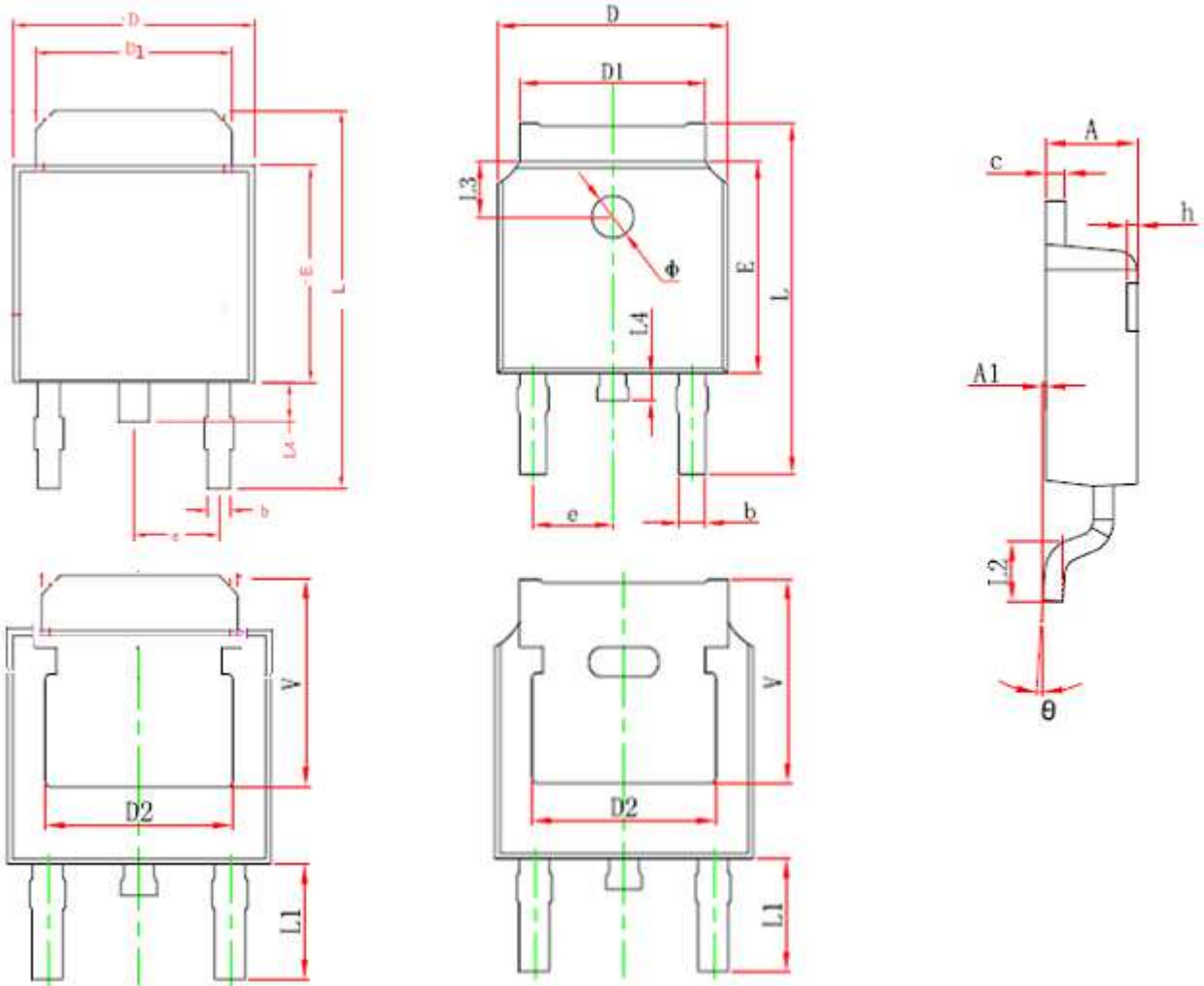
Fig 12. Gate Charge Waveform



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TO-252 PACKAGE OUTLINE



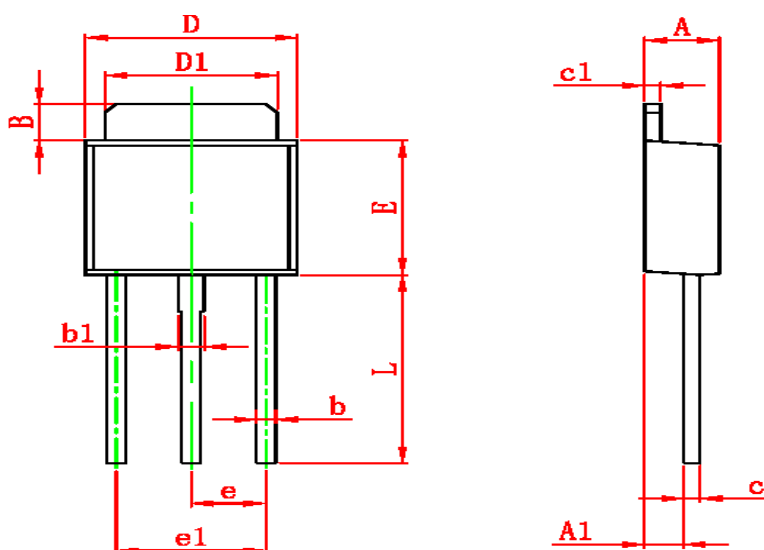
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 REF.		0.211 REF.	



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TO-251 PACKAGE OUTLINE



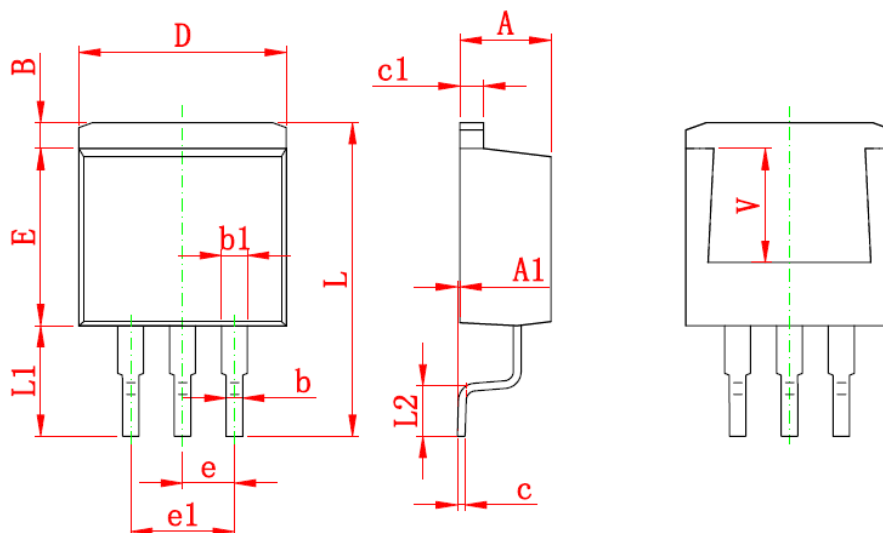
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	1.020	1.270	0.040	0.050
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP		0.091 TYP	
e1	4.500	4.700	0.177	0.185
L	7.500	7.900	0.295	0.311



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TO-263 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.470	4.670	0.176	0.184
A1	0.000	0.150	0.000	0.006
B	1.170	1.370	0.046	0.054
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	10.010	10.310	0.394	0.406
E	8.500	8.900	0.335	0.350
e	2.540 TYP		0.100 TYP	
e1	4.980	5.180	0.196	0.204
L	15.050	15.450	0.593	0.608
L1	5.080	5.480	0.200	0.216
L2	2.340	2.740	0.092	0.108
V	5.600 REF		0.220 REF	



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