SI1912EDH

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.280 @ V_{GS} = 4.5 V	1.28
	0.360 @ V_{GS} = 2.5 V	1.13
	0.450 @ V_{GS} = 1.8 V	1.0

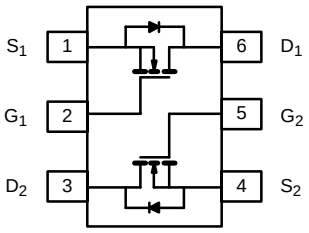
FEATURES

- TrenchFET® Power MOSFETS: 1.8-V Rated
- ESD Protected: 2000 V
- Thermally Enhanced SC-70 Package

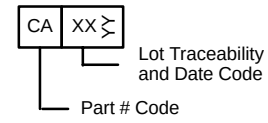
APPLICATIONS

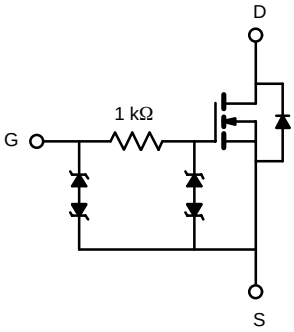
- Load Switching
- PA Switch
- Level Switch

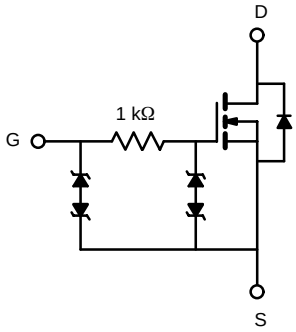
SOT-363
SC-70 (6-LEADS)



Top View







ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	5 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	20		V
Gate-Source Voltage		V_{GS}	±12		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	1.28	1.13	A
	T_A = 85°C		0.92	0.81	
Pulsed Drain Current		I_{DM}	4		
Continuous Diode Current (Diode Conduction)[a]		I_S	0.61	0.48	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	0.74	0.57	W
	T_A = 85°C		0.38	0.30	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 5 sec	R_{thJA}	130	170	°C/W
	Steady State		170	220	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	80	100	

Notes
a. Surface Mounted on 1” x 1” FR4 Board.

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SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 100 μA	0.45			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±4.5 V			±1	μA
		V_{DS} = 0 V, V_{GS} = ±12 V			±10	mA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V			1	μA
		V_{DS} = 16 V, V_{GS} = 0 V, T_J = 85°C			5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 4.5 V	2			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 1.13 A		0.220	0.280	Ω
		V_{GS} = 2.5 V, I_D = 0.99 A		0.281	0.360	
		V_{GS} = 1.8 V, I_D = 0.2 A		0.344	0.450	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 1.13 A		2.6		S
Diode Forward Voltage[a]	V_{SD}	I_S = 0.48 A, V_{GS} = 0 V		0.80	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 1.13 A		0.65	1.0	nC
Gate-Source Charge	Q_{gs}			0.2		
Gate-Drain Charge	Q_{gd}			0.23		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 20 Ω I_D ≅ 0.5 A, V_{GEN} = 4.5 V, R_G = 6 Ω		45	70	ns
Rise Time	t_r			85	130	
Turn-Off Delay Time	$t_{d(off)}$			350	530	
Fall Time	t_f			210	320	

Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.