NCV8508 Series

Advance Information

Low Dropout Linear Regulators with Watchdog, $\overline{\text{RESET}}$, and Wake Up

The NCV8508 is a precision micropower voltage regulator family. The part contains many of the required operational requirements for powering microprocessors. Its' robustness makes it suitable for severe automotive environments. The devices low dropout voltage ensures operation of loads (i.e. microprocessors) when the battery voltage is low such as during the cranking cycle of an automobile. In addition to being a good fit for the automotive environment, the NCV8508 is ideal for use in battery operated, microprocessor controlled equipment because of it's extremely low quiescent current.

Features

- Output Voltage Options: 3.3 V or 5.0 V
- ± 2.0% Output Voltage
- I_{OUT} Up to 250 mA
- Micropower Compatible Control Functions:
  - Wake Up
  - Watchdog
  - $\overline{\text{RESET}}$
- Low Dropout Voltage:
  - 250 mV @ 150 mV
- Low Quiescent Current (100 μA typ)
- Protection Features:
  - Thermal Shutdown
  - Short Circuit
  - 45 V Operation
- Internally Fused Leads in SO–16L Package

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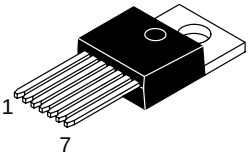
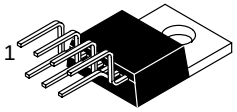
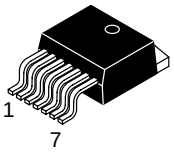


TO–220
SEVEN LEAD
T SUFFIX
CASE 821E

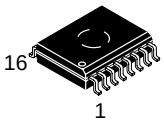


TO–220
SEVEN LEAD
TV SUFFIX
CASE 821J



D²PAK
7–PIN
D2T SUFFIX
CASE 936H

SO–8
D SUFFIX
CASE 751



SO–16L
DW SUFFIX
CASE 751G

ORDERING INFORMATION

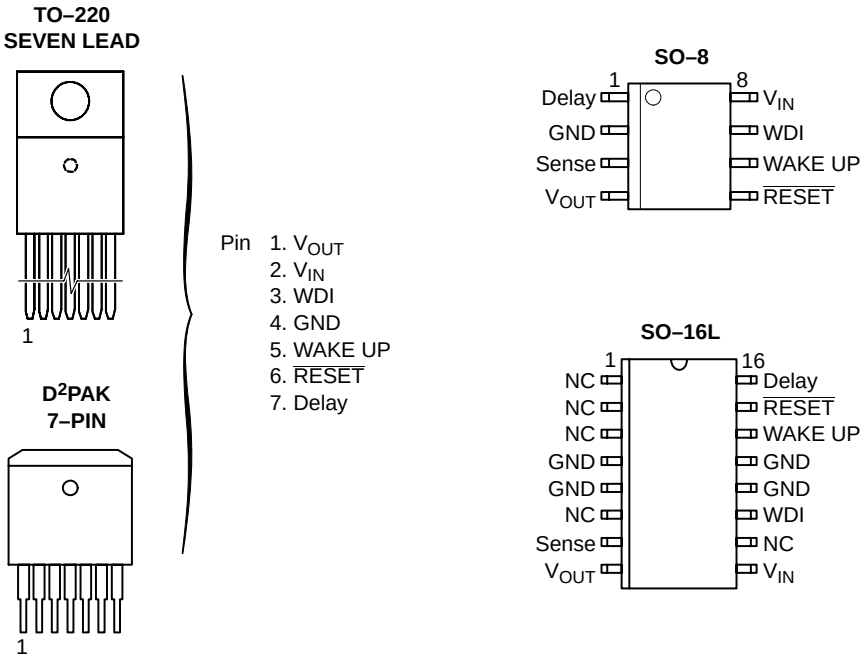
See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

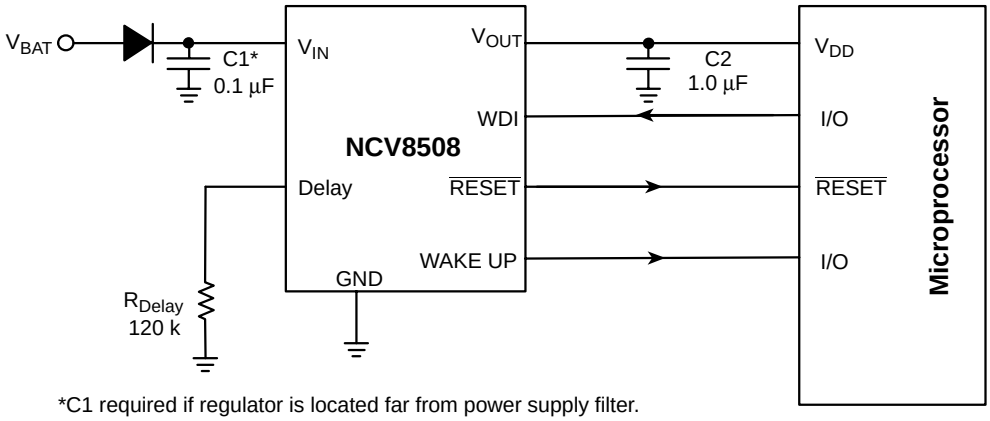
DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 9 of this data sheet.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

PIN CONNECTIONS





*C1 required if regulator is located far from power supply filter.

Figure 1. Application Circuit

MAXIMUM RATINGS*

Rating		Value	Unit
Input Voltage, V_{IN}		–0.3 to 45	V
Output Voltage, V_{OUT}		–0.3 to 18	V
ESD Susceptibility (Human Body Model)		2.0	kV
Logic Inputs/Outputs (Reset, WDI, Wakeup)		–0.3 to +7.0	V
Operating Junction Temperature, T_J		–40 to150	°C
Storage Temperature Range, T_S		–55 to +150	°C
Lead Temperature Soldering:	Wave Solder (through hole styles only) (Note 1.) Reflow: (SMD styles only) (Note 2.)	260 peak 230 peak	°C

1. 10 second maximum.
2. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS ($-40°C \le T_J \le 125°C$; $6.0\ V \le V_{IN} \le 28\ V$, $100\ \mu A \le I_{OUT} \le 150\ mA$, $C_2 = 1.0\ \mu F$, $R_{Delay} = 120\ k$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Output Selection					
Output Voltage, V_{OUT} for 3.3 V Option	–	3.234	3.300	3.366	V
Output Voltage, V_{OUT} for 5.0 V Option	–	4.90	5.00	5.10	V
Dropout Voltage ($V_{IN} - V_{OUT}$)	I_{OUT} = 150 mA. Note 3.	–	250	500	mV
Load Regulation	V_{IN} = 14 V, 5.0 mA < I_{OUT} < 150 mA	–	5.0	30	mV
Line Regulation	I_{OUT} = 5.0 mA	–	5.0	20	mV
Current Limit	–	250	400	–	mA
Thermal Shutdown	Guaranteed by Design	150	180	210	°C
Quiescent Current	V_{IN} = 12 V, I_{OUT} = 250 mA	–	100	150	μA
$\overline{\text{RESET}}$					
Threshold for 3.3 V Option	–	2.970	3.069	3.168	V
Threshold for 5.0 V Option	–	4.50	4.65	4.80	V
Output Low	R_{LOAD} = 10 k to V_{OUT}, $V_{OUT} \ge 1.0$ V	–	0.2	0.4	V
Output High	R_{LOAD} = 10 k to GND	–	V_{OUT} – 0.2	V_{OUT} – 0.4	V
Delay Time R_{Delay} = 60 k		3.0 1.5	5.0 2.5	7.0 3.5	ms
Watchdog Input					
Threshold High	–	70	–	–	%V_{OUT}
Threshold Low	–	–	–	30	%V_{OUT}
Hysteresis	–	25	100	–	mV
Input Current	0 < WDI < 6.0 V	–10	0	+10	μA
Pulse Width	50% WDI falling edge to 50% WDI rising edge and 50% WDI rising edge to 50% WDI falling edge, (see Figure 5)	5.0	–	–	μs
Wake Up Output					
Wake Up Period	See Figures 4 and 5. R_{DELAY} = 60 k	32 16	40 20	48 24	ms ms
Wake Up Duty Cycle Nominal	See Figure 3.	45	50	55	%
$\overline{\text{RESET}}$ HIGH to Wake Up Rising Delay Time	50% $\overline{\text{RESET}}$ rising edge to 50% Wake Up edge (see Figures 3 and 4) R_{DELAY} = 60 k	16 8	20 10	24 12	ms ms
Wake Up Response to Watchdog Input	50% WDI falling edge to 50% Wake Up falling edge	–	2.0	10	μs
Wake Up Response to $\overline{\text{RESET}}$	50% $\overline{\text{RESET}}$ falling edge to 50% Wake Up falling edge. V_{OUT} = 5.0 V→ 4.5 V	–	2.0	10	μs
Output Low	R_{LOAD} = 10 k	–	0.2	0.4	V
Output High	R_{LOAD} = 10 k	–	V_{OUT} – 0.2	V_{OUT} – 0.4	

3. Measured when the output voltage has dropped 100 mV from the nominal value

ELECTRICAL CHARACTERISTICS (continued) ($-40°C \le T_J \le 125°C$; $6.0\ V \le V_{IN} \le 28\ V$, $100\ \mu A \le I_{OUT} \le 150\ mA$, $C_2 = 1.0\ \mu F$, $R_{Delay} = 120\ k$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Delay					
Output Voltage	$I_{DELAY} = 50\ \mu A$. Note 4.	–	1.25	–	V

4. Current drain on the Delay pin directly affects the Delay Time, Wake Up Period, and the $\overline{\text{RESET}}$ to Wake Up Delay Time..

PACKAGE PIN DESCRIPTION

PACKAGE PIN #			PIN SYMBOL	FUNCTION
TO–220 & D^2PAK	SO–16L	SO–8		
1	8	4	V_{OUT}	Regulated output voltage ± 2.0%.
2	9	5	V_{IN}	Supply Voltage to the IC.
3	11	6	WDI	CMOS compatible input lead. The watchdog function monitors the falling edge of the incoming signal.
4	4, 5, 12, 13	2	GND	Ground connection.
5	14	7	WAKE UP	CMOS compatible output consisting of a continuously generated signal used to Wake Up the microprocessor from sleep mode.
6	15	8	$\overline{\text{RESET}}$	CMOS compatible output lead $\overline{\text{RESET}}$ goes low whenever V_{OUT} drops by more than 7.0% from nominal, or during the absence of a correct watchdog signal.
7	16	1	Delay	Buffered bandgap voltage used to create timing current for $\overline{\text{RESET}}$ and Wake Up from R_{Delay}.
–	1, 2, 3, 6, 10	–	NC	No Connection.
–	7	3	Sense	Kelvin connection which allows remote sensing of the output voltage for improved regulation. Connect to V_{OUT} if remote sensing is not required.

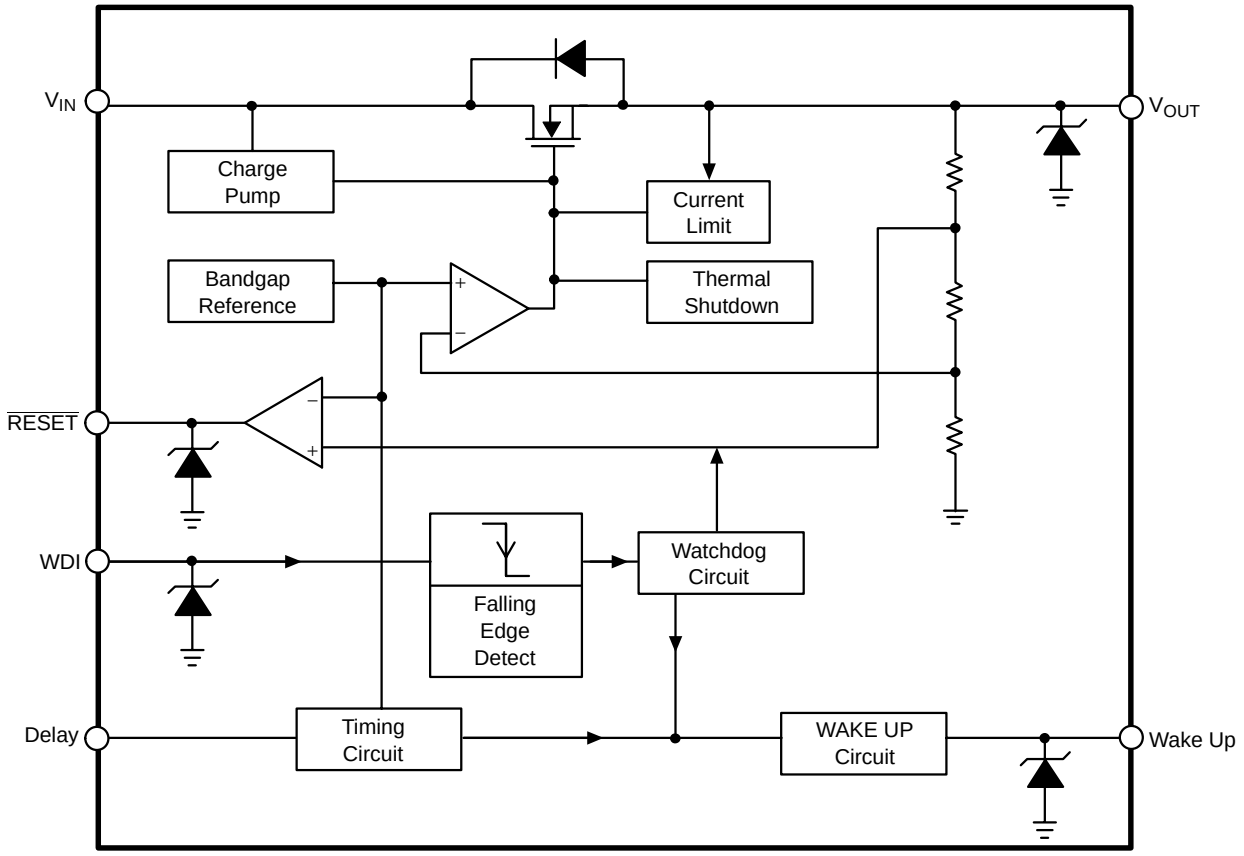


Figure 2. Block Diagram

TIMING DIAGRAMS

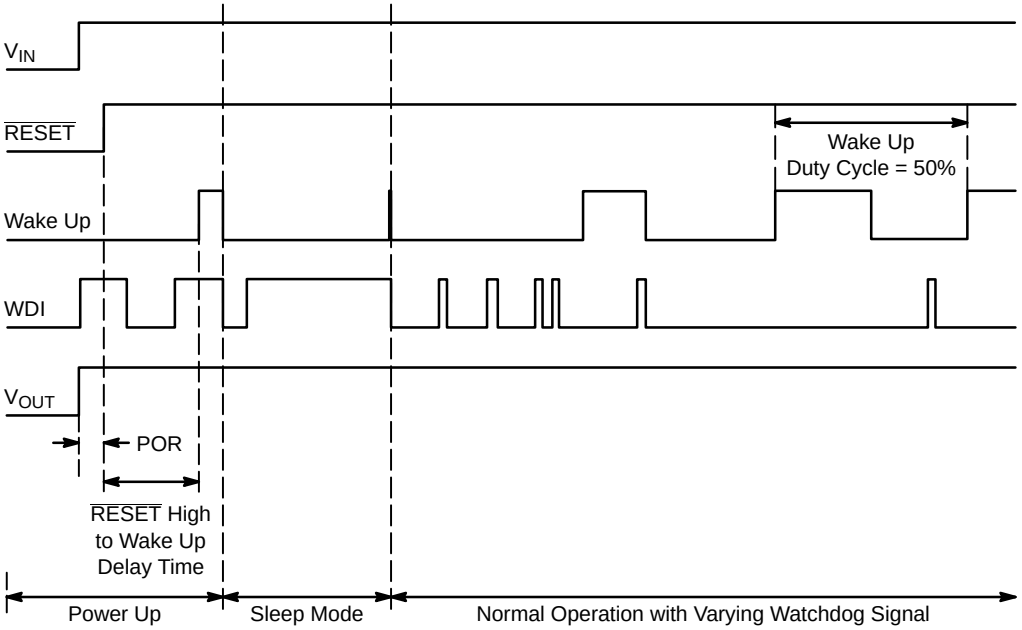


Figure 3. Power Up, Sleep Mode and Normal Operation

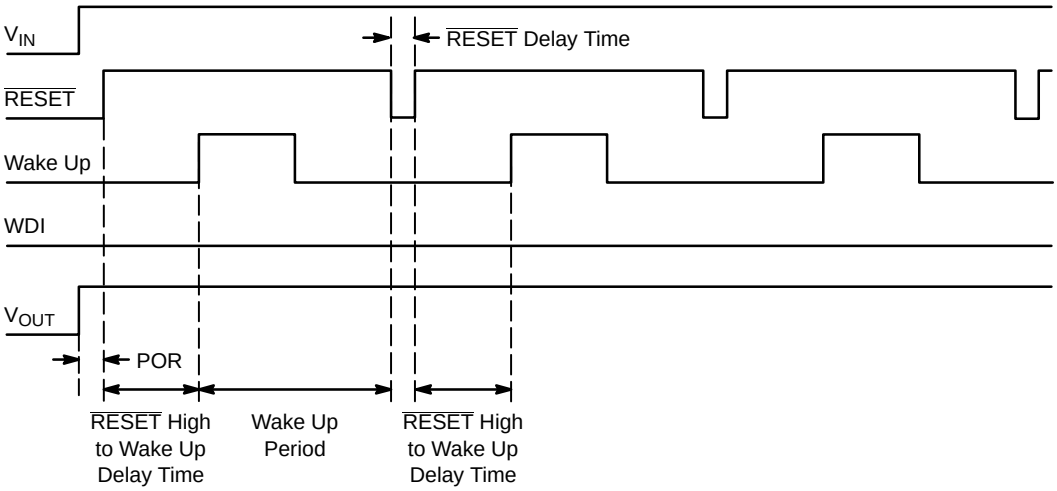


Figure 4. Error Condition: Watchdog Remains Low and a $\overline{\text{RESET}}$ Is Issued

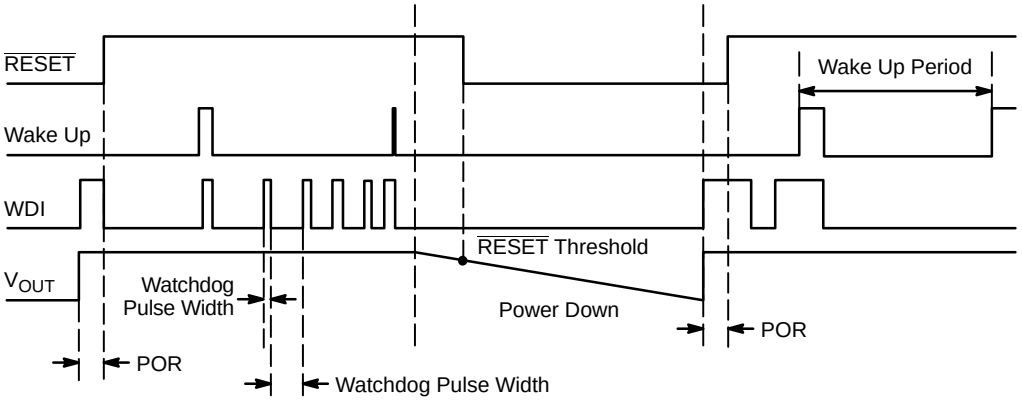


Figure 5. Power Down and Restart Sequence

DEFINITION OF TERMS

Dropout Voltage: The input–output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak–to–peak input ripple voltage to the peak–to–peak output ripple voltage.

Current Limit: Peak current that can be delivered to the output.

DETAILED OPERATING DESCRIPTION

The NCV8508 is a precision micro–power voltage regulator with very low quiescent current (100 μA typical at 250 mA load). A typical dropout voltage is 250 mV at 150 mA. Microprocessor control logic includes Watchdog, Wake Up and $\overline{\text{RESET}}$. This unique combination of extremely low quiescent current and full microprocessor control makes the NCV8508 ideal for use in battery operated, microprocessor controlled equipment in addition to being a good fit in the automotive environment.

The NCV8508 Wake Up function brings the microprocessor out of Sleep mode. The microprocessor in turn, signals its Wake Up status back to the NCV8508 by issuing a Watchdog signal.

The Watchdog logic function monitors an input signal (WDI) from the microprocessor. The NCV8508 responds to the falling edge of the Watchdog signal which it expects at least once during each wake–up period. When the correct Watchdog signal is received, a falling edge is issued on the wake–up signal line.

$\overline{\text{RESET}}$ is independent of V_{IN} and operates correctly to an output voltage as low as 1.0 V. A signal is issued in any of three situations. During power up the $\overline{\text{RESET}}$ is held low until the output voltage is in regulation. During operation if the output voltage shifts below the regulation limits, the $\overline{\text{RESET}}$ toggles low and remains low until proper output voltage regulation is restored. And finally, a $\overline{\text{RESET}}$ signal is issued if the regulator does not receive a Watchdog signal within the Wake Up period.

The $\overline{\text{RESET}}$ pulse width, Wake Up signal frequency, and Wake Up delay time are all set by one external resistor, R_{Delay}.

The Delay pin is a buffered bandgap voltage (1.25 V). It can be used as a reference for an external tracking regulator like the CS8182.

The regulator is protected against short circuit and thermal runaway conditions. The device runs through 45 volt transients, making it suitable for use in automotive environments.

CIRCUIT DESCRIPTION

Functional Description

To reduce the drain on the battery a system can go into a low current consumption mode when ever its not performing a main routine. The Wake Up signal is generated continuously and is used to interrupt a microcontroller that is in sleep mode. The nominal output is a 5.0 volt square wave with a duty cycle of 50% at a frequency that is determined by a timing resistor, R_{Delay}.

When the microprocessor receives a rising edge from the Wake Up output, it must issue a watchdog pulse and check its inputs to decide if it should resume normal operations or remain in the sleep mode.

The first falling edge of the watchdog signal causes the Wake Up to go low within 2.0 μs (typ) and remain low until the next Wake Up cycle (see Figure 6). Other watchdog pulses received within the same cycle are ignored (Figure 3).

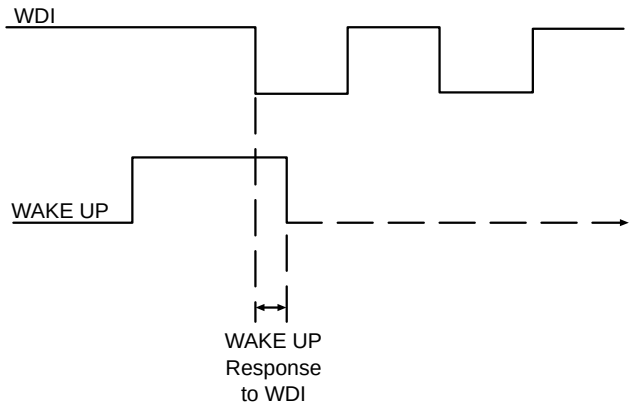


Figure 6. Wake Up Response to WDI

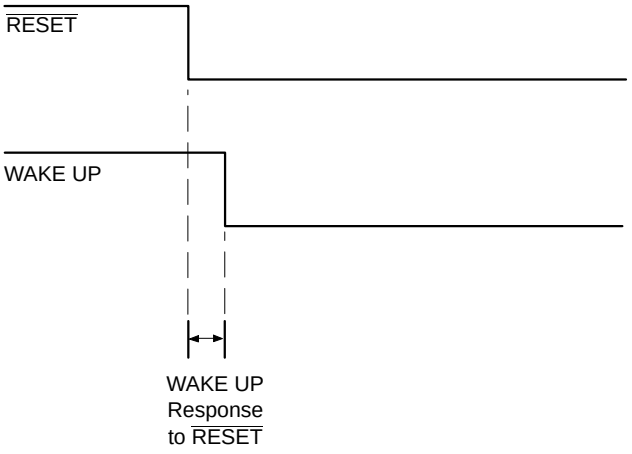


Figure 7. Wake Up Response to $\overline{\text{RESET}}$ (Low Voltage)

During power up, $\overline{\text{RESET}}$ is held low until the output voltage is in regulation. During operation, if the output voltage shifts below the regulation limits, the $\overline{\text{RESET}}$ toggles low and remains low until proper output voltage regulation is restored. After the $\overline{\text{RESET}}$ delay, $\overline{\text{RESET}}$ returns high.

The Watchdog circuitry continuously monitors the input watchdog signal (WDI) from the microprocessor. The absence of a falling edge on the Watchdog input during one Wake Up cycle will cause a $\overline{\text{RESET}}$ pulse to occur at the end of the Wake Up cycle. (see Figure 4).

The Wake Up output is pulled low during a $\overline{\text{RESET}}$ regardless of the cause of the $\overline{\text{RESET}}$. After the $\overline{\text{RESET}}$ returns high, the Wake Up cycle begins again (see Figure 4).

The $\overline{\text{RESET}}$ Delay Time, Wake Up signal frequency and $\overline{\text{RESET}}$ high to Wake Up delay time are all set by one external resistor R_{Delay}.

Wake Up period = $(3.33 \times 10^{-7})R_{Delay}$

$\overline{\text{RESET}}$ Delay Time = $(4.17 \times 10^{-8})R_{Delay}$

$\overline{\text{RESET}}$ HIGH to Wake Up Delay Time = $(1.67 \times 10^{-7})R_{Delay}$

Capacitor temperature coefficient and tolerance as well as the tolerance of the NCV8508 must be taken into account in order to get the correct system tolerance for each parameter.

APPLICATION NOTES

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 8) is:

$$P_{D(max)} = \{V_{IN(max)} - V_{OUT(min)}\} + V_{IN(max)}I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current for the application, and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

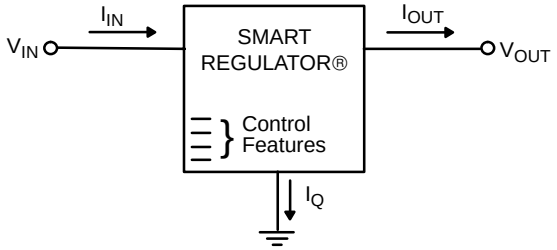


Figure 8. Single Output Regulator with Key Performance Parameters Labeled

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\Theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150^\circ C - T_A}{P_D} \quad (2)$$

The value of $R_{\Theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\Theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta JA}$:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \quad (3)$$

where:

$R_{\Theta JC}$ = the junction–to–case thermal resistance,

$R_{\Theta CS}$ = the case–to–heatsink thermal resistance, and

$R_{\Theta SA}$ = the heatsink–to–ambient thermal resistance.

$R_{\Theta JC}$ appears in the package section of the data sheet. Like $R_{\Theta JA}$, it too is a function of package type. $R_{\Theta CS}$ and $R_{\Theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

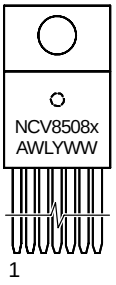
ORDERING INFORMATION

Device	Output Voltage	Package	Shipping
NCV8508T33	3.3 V	TO–220 STRAIGHT, 7–PIN	50 Units/Rail
NCV8508TV33		TO–220 VERTICAL, 7–PIN	50 Units/Rail
NCV8508D2T33		D^2PAK, 7–PIN	50 Units/Rail
NCV8508D2T33R4		D^2PAK, 7–PIN	750 Tape & Reel
NCV8508D33		SO–8	95 Units/Rail
NCV8508D33R2		SO–8	2500 Tape & Reel
NCV8508DW33		SO–16L	46 Units/Rail
NCV8508DW33R2		SO–16L	1000 Tape & Reel
NCV8508T50	5.0 V	TO–220 STRAIGHT, 7–PIN	50 Units/Rail
NCV8508TV50		TO–220 VERTICAL, 7–PIN	50 Units/Rail
NCV8508D2T50		D^2PAK, 7–PIN	50 Units/Rail
NCV8508D2T50R4		D^2PAK, 7–PIN	750 Tape & Reel
NCV8508D50		SO–8	95 Units/Rail
NCV8508D50R2		SO–8	2500 Tape & Reel
NCV8508DW50		SO–16L	46 Units/Rail
NCV8508DW50R2		SO–16L	1000 Tape & Reel

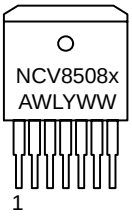
MARKING DIAGRAMS

TO–220
SEVEN LEAD
T SUFFIX
CASE 821E

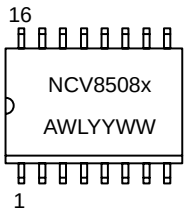
TO–220
SEVEN LEAD
TV SUFFIX
CASE 821J



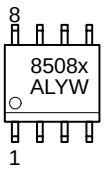
D^2PAK
7–PIN
D2T SUFFIX
CASE 936H



SO–16L
DW SUFFIX
CASE 751G



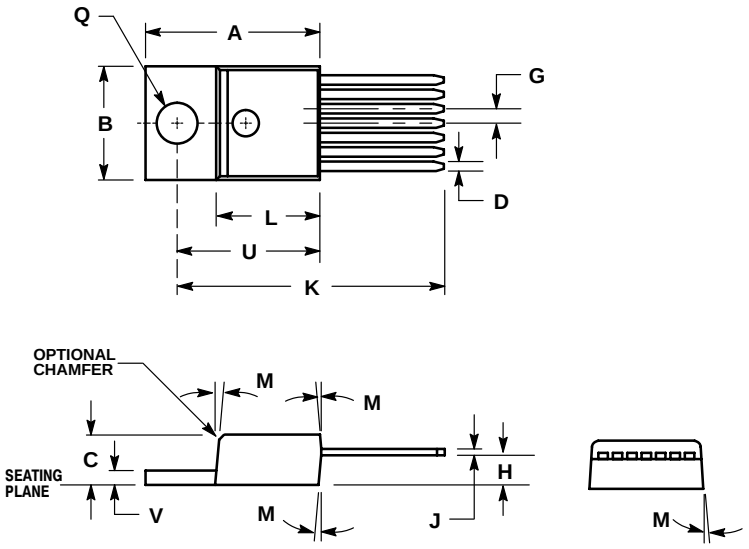
SO–8
D SUFFIX
CASE 751



x = Voltage Ratings as Indicated Below:
3 = 3.3 V
5 = 5.0 V
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PACKAGE DIMENSIONS

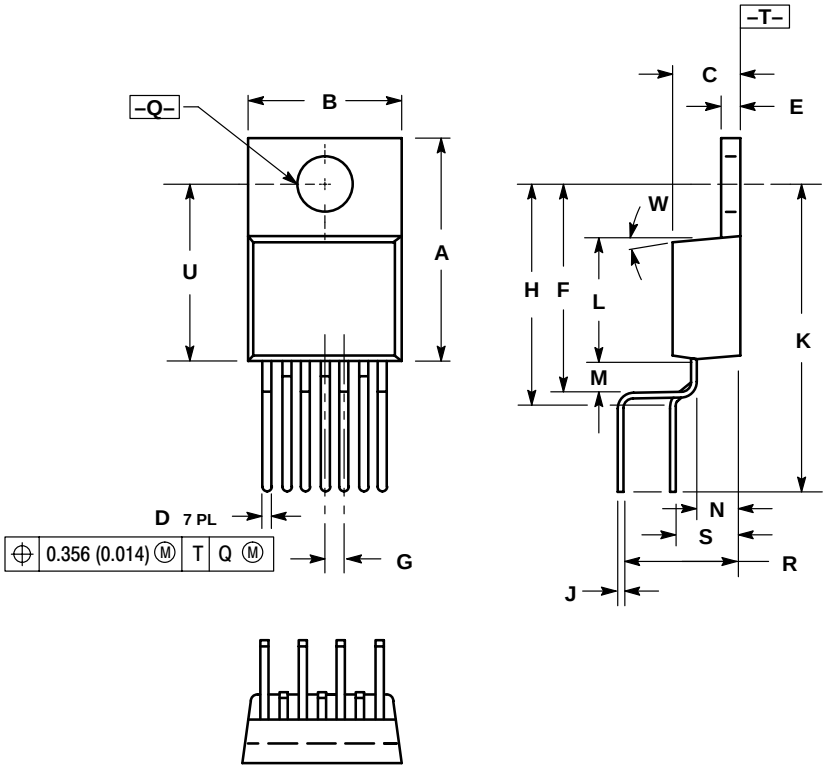
TO–220
SEVEN LEAD
T SUFFIX
CASE 821E–04
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.003 (0.076) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.600	0.610	15.24	15.49
B	0.386	0.403	9.80	10.23
C	0.170	0.180	4.32	4.56
D	0.028	0.037	0.71	0.94
G	0.045	0.055	1.15	1.39
H	0.088	0.102	2.24	2.59
J	0.018	0.026	0.46	0.66
K	1.028	1.042	26.11	26.47
L	0.355	0.365	9.02	9.27
M	5 ° NOM		5 ° NOM	
Q	0.142	0.148	3.61	3.75
U	0.490	0.501	12.45	12.72
V	0.045	0.055	1.15	1.39

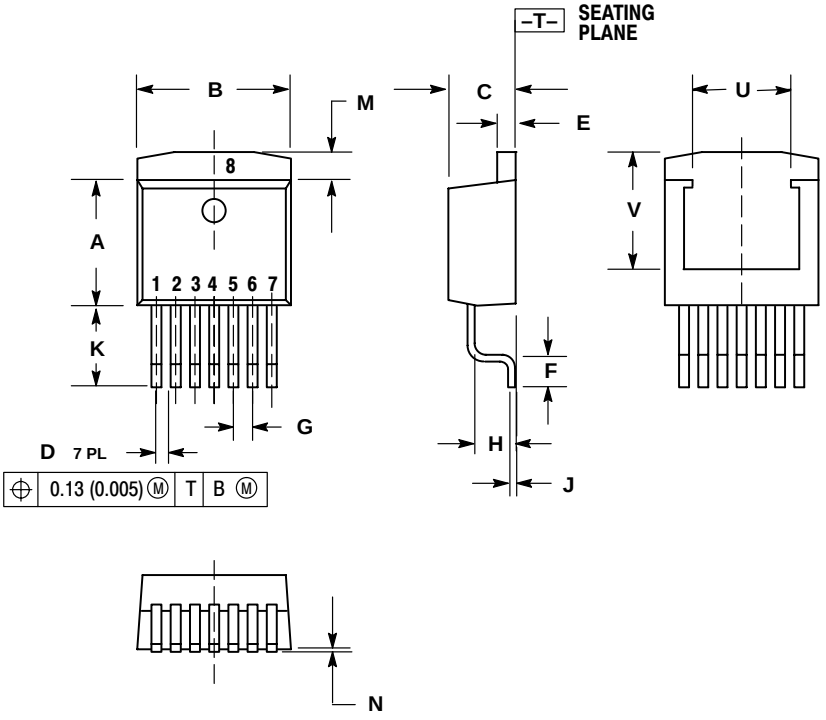
TO–220
SEVEN LEAD
TV SUFFIX
CASE 821J–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.560	0.590	14.22	14.99
B	0.385	0.415	9.77	10.54
C	0.160	0.190	4.06	4.82
D	0.023	0.037	0.58	0.94
E	0.045	0.055	1.14	1.40
F	0.540	0.555	13.72	14.10
G	0.050 BSC		1.27 BSC	
H	0.570	0.595	14.48	15.11
J	0.014	0.022	0.36	0.56
K	0.785	0.800	19.94	20.32
L	0.322	0.337	8.18	8.56
M	0.073	0.088	1.85	2.24
N	0.090	0.115	2.28	2.91
Q	0.146	0.156	3.70	3.95
R	0.289	0.304	7.34	7.72
S	0.164	0.179	4.17	4.55
U	0.460	0.475	11.68	12.07
W	3 °		3 °	

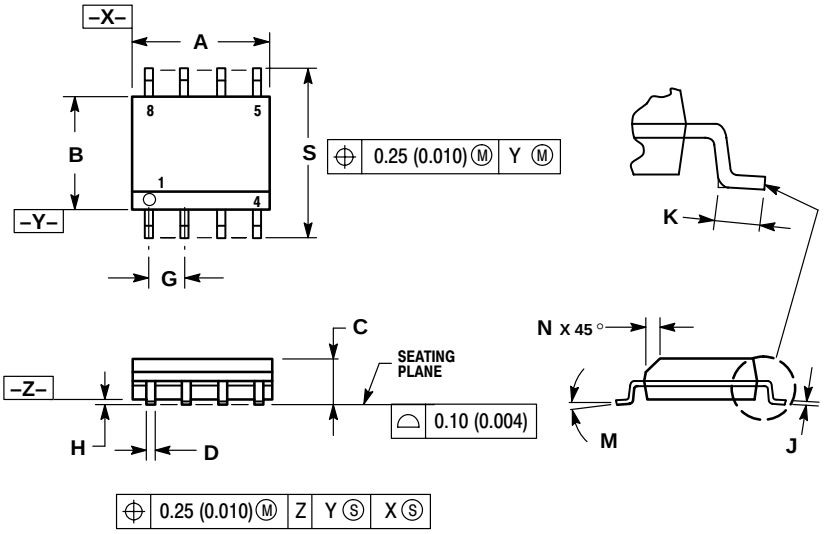
D²PAK
7–PIN
D2T SUFFIX
CASE 936H–01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS B AND M.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAX.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.326	0.336	8.28	8.53
B	0.396	0.406	10.05	10.31
C	0.170	0.180	4.31	4.57
D	0.026	0.036	0.66	0.91
E	0.045	0.055	1.14	1.40
F	0.058	0.078	1.41	1.98
G	0.050 BSC		1.27 BSC	
H	0.100	0.110	2.54	2.79
J	0.018	0.025	0.46	0.64
K	0.204	0.214	5.18	5.44
M	0.055	0.066	1.40	1.68
N	0.000	0.004	0.00	0.10
U	0.256 REF		6.50 REF	
V	0.305 REF		7.75 REF	

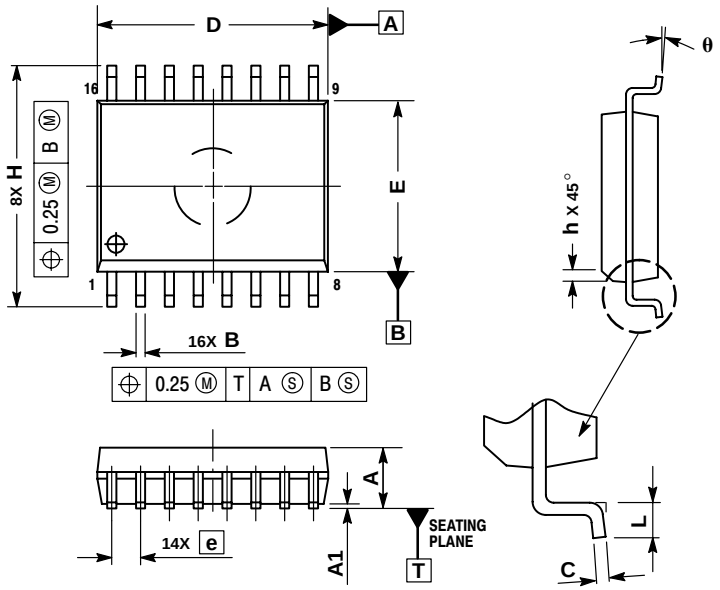
SO–8
D SUFFIX
CASE 751–07
ISSUE W



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SO–16L
DW SUFFIX
CASE 751G–03
ISSUE B



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

PACKAGE THERMAL DATA

Parameter		TO–220 7 LEAD	D^2PAK 7–Pin	SO–8	SO–16L	Unit
$R_{\Theta JC}$	Typical	1.8	1.8	45	18	°C/W
$R_{\Theta JA}$	Typical	50	10–50*	165	75	°C/W

*Depending on thermal properties of substrate. $R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CA}$.

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