AAT8401

General Description

The AAT8401 is a low threshold MOSFET designed for the battery, cell phone, and PDA markets. Using AnalogicTech™'s ultra high density proprietary TrenchDMOS™ technology, this product demonstrates high power handling and small size.

Features

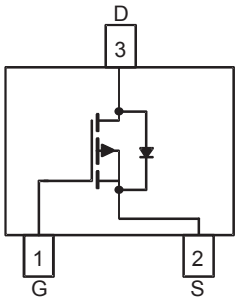
- $V_{DS(MAX)}$ = -20V
- $I_{D(MAX)}$ [1] = -2.4A @ 25°C
- Low $R_{DS(ON)}$:
  - 100 mΩ @ V_{GS} = -4.5V
  - 175 mΩ @ V_{GS} = -2.5V

Applications

- Battery Packs
- Cellular & Cordless Telephones
- Battery-powered portable equipment

SC59 Package

Top View



Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Symbol	Description		Value	Units
V_{DS}	Drain-Source Voltage		-20	V
V_{GS}	Gate-Source Voltage		±12	
I_D	Continuous Drain Current @ T_J=150°C [1]	T_A = 25°C	±2.4	A
		T_A = 70°C	±2.0	
I_{DM}	Pulsed Drain Current [2]		±9	
I_S	Continuous Source Current (Source-Drain Diode) [1]		-0.9	
P_D	Maximum Power Dissipation [1]	T_A = 25°C	1.0	W
		T_A = 70°C	0.6	
T_J, T_{STG}	Operating Junction and Storage Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	Description	Value	Units
$R_{\theta JA}$	Typical Junction-to-Ambient steady state [1]	145	°C/W
$R_{\theta JA2}$	Maximum Junction-to-Ambient t<5 seconds [1]	125	°C/W
$R_{\theta JF}$	Typical Junction-to-Foot [1]	50	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Description	Conditions	Min	Typ	Max	Units
DC Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-20			V
$R_{DS(ON)}$	Drain-Source ON-Resistance [2]	V_{GS}=-4.5V, I_D=-2.4A		88	100	mΩ
		V_{GS}=-2.5V, I_D=-1.8A		146	175	
$I_{D(ON)}$	On-State Drain Current [2]	V_{GS}=-4.5V, V_{DS}=-5V (Pulsed)	-9			A
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS}, I_D=-250μA	-0.6			V
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±12V, V_{DS}=0V			±100	nA
I_{DSS}	Drain Source Leakage Current	V_{GS}=0V, V_{DS}=-20V			-1	μA
		V_{GS}=0V, V_{DS}=-16V, T_J=70°C [3]			-5	
g_{fs}	Forward Transconductance [2]	V_{DS}=-5V, I_D=-2.4A		4		S
Dynamic Characteristics [3]						
Q_G	Total Gate Charge	V_{DS}=-15V, R_D=5.6Ω, V_{GS}=-4.5V		4		nC
Q_{GS}	Gate-Source Charge	V_{DS}=-15V, R_D=5.6Ω, V_{GS}=-4.5V		0.6		
Q_{GD}	Gate-Drain Charge	V_{DS}=-15V, R_D=5.6Ω, V_{GS}=-4.5V		1.4		
$t_{D(ON)}$	Turn-ON Delay	V_{DS}=-15V, R_D=5.6Ω, V_{GS}=-4.5V, R_G=6Ω		6.5		ns
t_R	Turn-ON Rise Time	V_{DS}=-15V, R_D=5.6Ω, V_{GS}=-4.5V, R_G=6Ω		13		
$t_{D(OFF)}$	Turn-OFF Delay	V_{DS}=-15V, R_D=5.6Ω, V_{GS}=-4.5V, R_G=6Ω		15		
t_F	Turn-OFF Fall Time	V_{DS}=-15V, R_D=5.6Ω, V_{GS}=-4.5V, R_G=6Ω		20		
Source-Drain Diode Characteristics						
V_{SD}	Source-Drain Forward Voltage [2]	V_{GS}=0, I_S=-2.4A			-1.3	V
I_S	Continuous Diode Current [1]				-0.9	A

Note 1: Based on thermal dissipation from junction to ambient while mounted on a 1" x 1" PCB with optimized layout. A 5 second pulse on a 1" x 1" PCB approximates testing a device mounted on a large multi-layer PCB as in most applications. $R_{\theta JF}$ + $R_{\theta FA}$ = $R_{\theta JA}$ where the foot thermal reference is defined as the normal solder mounting surface of the device's leads. $R_{\theta JF}$ is guaranteed by design, however $R_{\theta CA}$ is determined by the PCB design. Actual maximum continuous current is limited by the application's design.

Note 2: Pulse test: Pulse Width = 300 μs

Note 3: Guaranteed by design. Not subject to production testing.