



Dear customers,

**About the change in the name such as "Oki Electric Industry Co. Ltd." and "OKI" in documents to OKI Semiconductor Co., Ltd.**

The semiconductor business of Oki Electric Industry Co., Ltd. was succeeded to OKI Semiconductor Co., Ltd. on October 1, 2008. Therefore, please accept that although the terms and marks of "Oki Electric Industry Co., Ltd.", "Oki Electric", and "OKI" remain in the documents, they all have been changed to "OKI Semiconductor Co., Ltd.". It is a change of the company name, the company trademark, and the logo, etc. , and NOT a content change in documents.

October 1, 2008  
OKI Semiconductor Co., Ltd.

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# OKI Semiconductor

## MD56V62800A

**4-Bank × 2,097,152-Word × 8-Bit SYNCHRONOUS DYNAMIC RAM**

### DESCRIPTION

The MD56V62800A is a 4-bank × 2,097,152-word × 8-bit synchronous dynamic RAM, fabricated in Oki's CMOS silicon-gate process technology. The device operates at 3.3 V. The inputs and outputs are LVTTTL compatible.

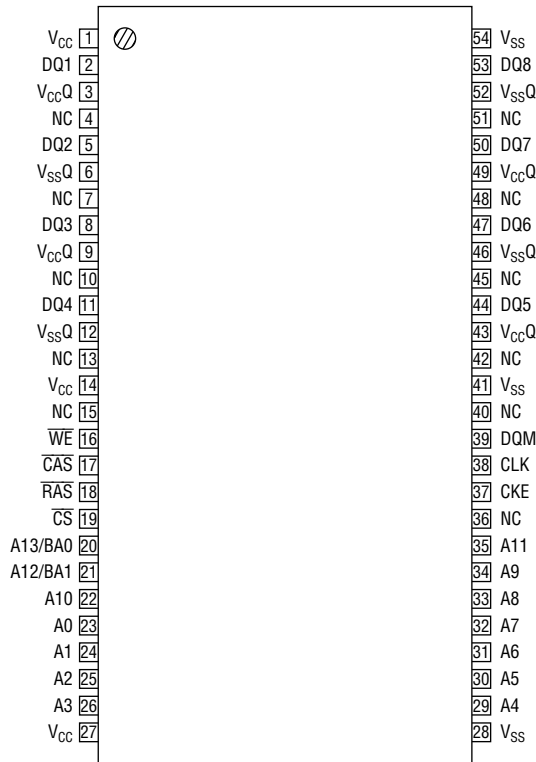
### FEATURES

- Silicon gate, quadruple polysilicon CMOS, 1-transistor memory cell
- 4-bank × 2,097,152-word × 8-bit configuration
- 3.3 V power supply, ±0.3 V tolerance
- Input : LVTTTL compatible
- Output : LVTTTL compatible
- Refresh : 4096 cycles/64 ms
- Programmable data transfer mode
  - $\overline{\text{CAS}}$  latency (1, 2, 3)
  - Burst length (1, 2, 4, 8, full page)
  - Data scramble (sequential, interleave)
- Burst read single bit write capability
- CBR auto-refresh, Self-refresh capability
- Package:
  - 54-pin 400 mil plastic TSOP (Type II) (TSOPII54-P-400-0.80-K) (Product : MD56V62800A-xxTA)
  - xx indicates speed rank.

### PRODUCT FAMILY

Family	Max. Frequency	Access Time (Max.)	
		t <sub>AC2</sub>	t <sub>AC3</sub>
MD56V62800A-8	125 MHz	10 ns	6 ns
MD56V62800A-10	100 MHz	9 ns	9 ns

**PIN CONFIGURATION (TOP VIEW)**



54-Pin Plastic TSOP (II)  
(K Type)

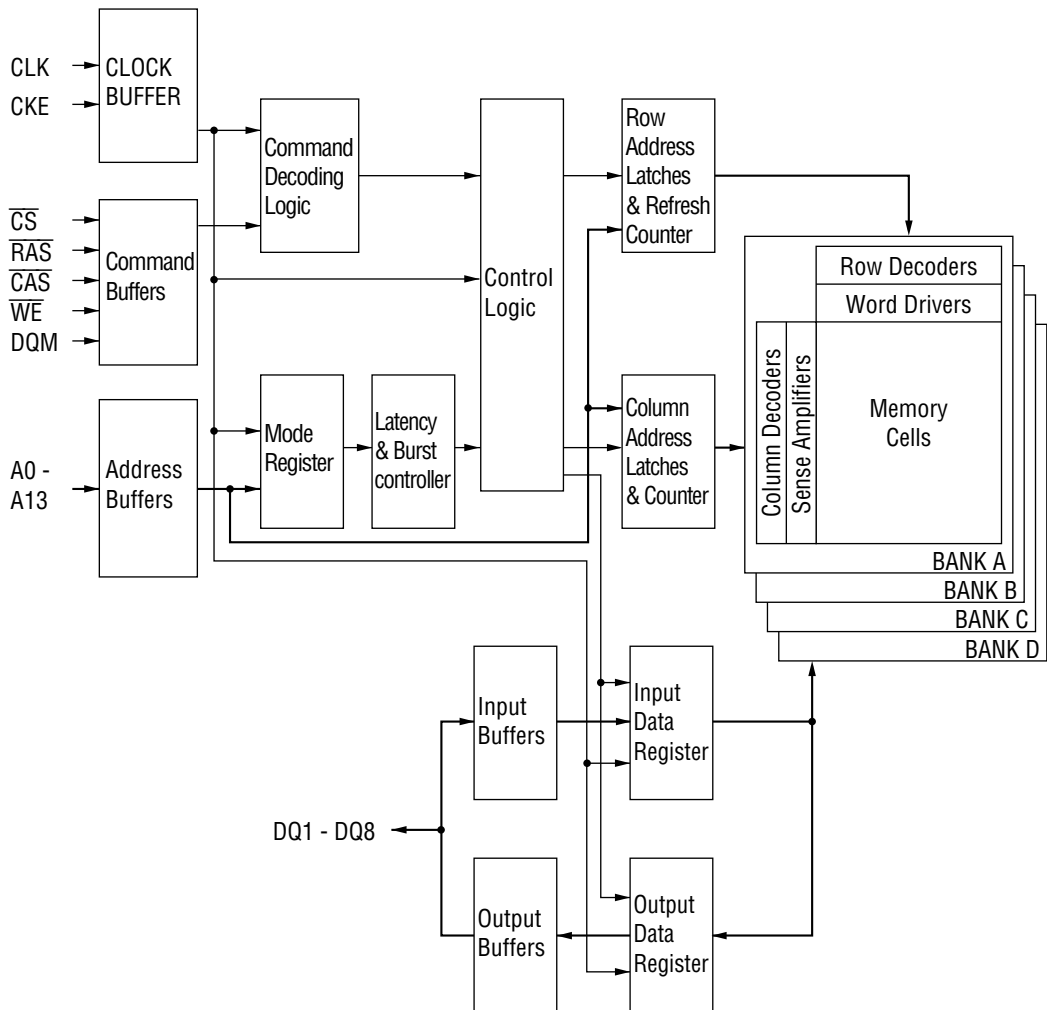
Pin Name	Function	Pin Name	Function
CLK	System Clock	DQM	Data Input/Output Mask
CS	Chip Select	DQi	Data Input/Output
CKE	Clock Enable	VCC	Power Supply (3.3 V)
A0 - A11	Address	VSS	Ground (0 V)
A12, A13	Bank Select Address	VCCQ	Data Output Power Supply (3.3 V)
RAS	Row Address Strobe	VSSQ	Data Output Ground (0 V)
CAS	Column Address Strobe	NC	No Connection
WE	Write Enable		

Note: The same power supply voltage must be provided to every VCC pin and VCCQ pin. The same GND voltage level must be provided to every VSS pin and VSSQ pin.

**PIN DESCRIPTION**

CLK	Fetches all inputs at the "H" edge.
$\overline{CS}$	Disables or enables device operation by asserting or deactivating all inputs except CLK, CKE and DQM.
CKE	Masks system clock to deactivate the subsequent CLK operation. If CKE is deactivated, system clock will be masked so that the subsequent CLK operation is deactivated. CKE should be asserted at least one cycle prior to a new command.
Address	Row & column multiplexed. Row address: RA0 – RA11 Column address: CA0 – CA8
A12, A13 (BA1, BA0)	Bank Access pins. These pins are dedicated to select one of 4 banks.
$\overline{RAS}$ $\overline{CAS}$ $\overline{WE}$	Functionality depends on the combination. For details, see the function truth table.
DQM	Masks the read data of two clocks later when DQM is set "H" at the "H" edge of the clock signal. Masks the write data of the same clock when DQM is set "H" at the "H" edge of the clock signal.
DQi	Data inputs/outputs are multiplexed on the same pin.

**BLOCK DIAGRAM**



## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

(Voltages referenced to  $V_{SS}$ )

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
$V_{CC}$ Supply Voltage	$V_{CC}, V_{CCQ}$	-0.5 to 4.6	V
Storage Temperature	$T_{stg}$	-55 to 150	°C
Power Dissipation	$P_D^*$	1	W
Short Circuit Current	$I_{OS}$	50	mA
Operating Temperature	$T_{opr}$	0 to 70	°C

\*:  $T_a = 25^\circ\text{C}$ 

### Recommended Operating Conditions

(Voltages referenced to  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{CC}, V_{CCQ}$	3.0	3.3	3.6	V
Input High Voltage	$V_{IH}$	2.0	—	$V_{CC} + 0.3$	V
Input Low Voltage	$V_{IL}$	-0.3	—	0.8	V

### Capacitance

( $V_{CC} = 3.3\text{ V}$ ,  $V_{bias} = 1.4\text{ V}$ ,  $T_a = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance (CLK)	$C_{CLK}$	2.5	4	pF
Input Capacitance (CKE, $\overline{CS}$ , RAS, $\overline{CAS}$ , $\overline{WE}$ , DQM, A0 - A13)	$C_{IN}$	2.5	5	pF
Input/Output Capacitance (DQ1 - DQ8)	$C_{OUT}$	4	6.5	pF

DC Characteristics

Parameter	Symbol	Condition			Version				Unit	Note
		Bank	CKE	Others	-8		-10			
					Min.	Max.	Min.	Max.		
Output High Voltage	V <sub>OH</sub>	—	—	I <sub>OH</sub> = -2 mA	2.4	—	2.4	—	V	
Output Low Voltage	V <sub>OL</sub>	—	—	I <sub>OL</sub> = 2 mA	—	0.4	—	0.4	V	
Input Leakage Current	I <sub>LI</sub>	—	—	—	-5	5	-5	5	μA	
Output Leakage Current	I <sub>LO</sub>	—	—	—	-5	5	-5	5	μA	
Average Power Supply Current (Operating)	I <sub>CC1</sub>	One Bank Active	CKE ≥ V <sub>IH</sub>	t <sub>CC</sub> = min t <sub>RC</sub> = min No Burst	—	125	—	115	mA	1, 2
	I <sub>CC1D</sub>	Both Banks Active	CKE ≥ V <sub>IH</sub>	t <sub>CC</sub> = min t <sub>RC</sub> = min t <sub>R RD</sub> = min No Burst	—	175	—	165	mA	1, 2
Power Supply Current (Stand by)	I <sub>CC2</sub>	Both Banks Precharge	CKE ≥ V <sub>IH</sub>	t <sub>CC</sub> = min	—	30	—	30	mA	3
Average Power Supply Current (Clock Suspension)	I <sub>CC3S</sub>	Both Banks Active	CKE ≤ V <sub>IL</sub>	t <sub>CC</sub> = min	—	6	—	6	mA	2
Average Power Supply Current (Active Stand by)	I <sub>CC3</sub>	One Bank Active	CKE ≥ V <sub>IH</sub> , CS ≥ V <sub>IH</sub>	t <sub>CC</sub> = min	—	60	—	50	mA	3
Power Supply Current (Burst)	I <sub>CC4</sub>	Both Banks Active	CKE ≥ V <sub>IH</sub>	t <sub>CC</sub> = min	—	165	—	155	mA	1, 2
Power Supply Current (Auto-Refresh)	I <sub>CC5</sub>	One Bank Active	CKE ≥ V <sub>IH</sub>	t <sub>CC</sub> = min t <sub>RC</sub> = min	—	185	—	185	mA	2
Average Power Supply Current (Self-Refresh)	I <sub>CC6</sub>	Both Banks Precharge	CKE ≤ 0.2 V	t <sub>CC</sub> = min	—	2	—	2	mA	
Average Power Supply Current (Power down)	I <sub>CC7</sub>	Both Banks Precharge	CKE ≤ V <sub>IL</sub>	t <sub>CC</sub> = min	—	2	—	2	mA	

- Notes:
1. Measured with outputs open.
  2. The address and data can be changed once or left unchanged during one cycle.
  3. The address and data can be changed once or left unchanged during two cycles.

**Mode Set Address Keys**

Write Burst Length		$\overline{\text{CAS}}$ Latency				Burst Type		Burst Length				
A9	Write Burst Length	A6	A5	A4	CL	A3	BT	A2	A1	A0	BT = 0	BT = 1
0	Burst Write	0	0	0	Reserved	0	Sequential	0	0	0	1	1
1	Single Bit Write	0	0	1	1	1	Interleave	0	0	1	2	2
		0	1	0	2			0	1	0	4	4
		0	1	1	3			0	1	1	8	8
		1	0	0	Reserved			1	0	0	Reserved	Reserved
		1	0	1	Reserved			1	0	1	Reserved	Reserved
		1	1	0	Reserved			1	1	0	Reserved	Reserved
		1	1	1	Reserved			1	1	1	Full Page	Reserved

- Notes:
1. A7, A8, A10, A11, A12 and A13 should stay "L" during mode set cycle.
  2. When A9 = 1, a burst length for write operation is always 1 regardless of the burst lengths set by A0, A1 and A2.

**POWER ON SEQUENCE**

1. With inputs in NOP state, turn on the power supply and start the system clock.
2. After the V<sub>CC</sub> voltage has reached the specified level, pause for 200 μs or more with the input kept in NOP state.
3. Issue the precharge all bank command.
4. Apply a CBR auto-refresh eight or more times.
5. Enter the mode register setting command.

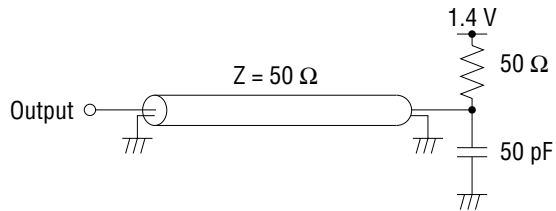


AC Characteristics

Note 1, 2

Parameter		Symbol	MD56V62800A-8		MD56V62800A-10		Unit	Note
			Min.	Max.	Min.	Max.		
Clock Cycles Time	CL = 3	t <sub>CC</sub>	8	—	10	—	ns	
	CL = 2		12	—	15	—	ns	
	CL = 1		24	—	30	—	ns	
Access Time from Clock	CL = 3	t <sub>AC</sub>	—	6	—	9	ns	3, 4
	CL = 2		—	10	—	9	ns	3, 4
	CL = 1		—	22	—	27	ns	3, 4
Clock "H" Pulse Time		t <sub>CH</sub>	3	—	3	—	ns	
Clock "L" Pulse Time		t <sub>CL</sub>	3	—	3	—	ns	
Input Setup Time		t <sub>SI</sub>	2	—	3	—	ns	
Input Hold Time		t <sub>HI</sub>	1	—	1	—	ns	
Output Low Impedance Time from Clock		t <sub>OLZ</sub>	3	—	3	—	ns	
Output High Impedance Time from Clock		t <sub>OHZ</sub>	—	8	—	8	ns	
Output Hold from Clock		t <sub>OH</sub>	3	—	3	—	ns	3
RAS Cycle Time		t <sub>RC</sub>	80	—	90	—	ns	
RAS Precharge Time		t <sub>RP</sub>	30	—	30	—	ns	
RAS Active Time		t <sub>RAS</sub>	50	100,000	60	100,000	ns	
RAS to CAS Delay Time		t <sub>RCD</sub>	20	—	30	—	ns	
Write Recovery Time		t <sub>WR</sub>	8	—	10	—	ns	
RAS to RAS Bank Active Delay Time		t <sub>RRD</sub>	16	—	20	—	ns	
Refresh Time		t <sub>REF</sub>	—	64	—	64	ms	
Power-down Exit Set-up Time		t <sub>PDE</sub>	t <sub>SI</sub> + 1 CLK	—	t <sub>SI</sub> + 1 CLK	—	ns	
Input Level Transition Time		t <sub>T</sub>	—	3	—	3	ns	
CAS to CAS Delay Time (Min.)		t <sub>CCD</sub>	1		1		Cycle	
Clock Disable Time from CKE		t <sub>CKE</sub>	1		1		Cycle	
Data Output High Impedance Time from DQM		t <sub>DOZ</sub>	2		2		Cycle	
Data Input Mask Time from DQM		t <sub>DOD</sub>	0		0		Cycle	
Data Input Time from Write Command		t <sub>DWD</sub>	0		0		Cycle	
Data Output High Impedance Time from Precharge Command	CL = 3	t <sub>ROH</sub>	3		3		Cycle	
	CL = 2		2		2		Cycle	
	CL = 1		1		1		Cycle	
Active Command Input Time from Mode Register Set Command Input (Min.)		t <sub>MRD</sub>	3		3		Cycle	
Write Command Input Time from Output		t <sub>OWD</sub>	2		2		Cycle	

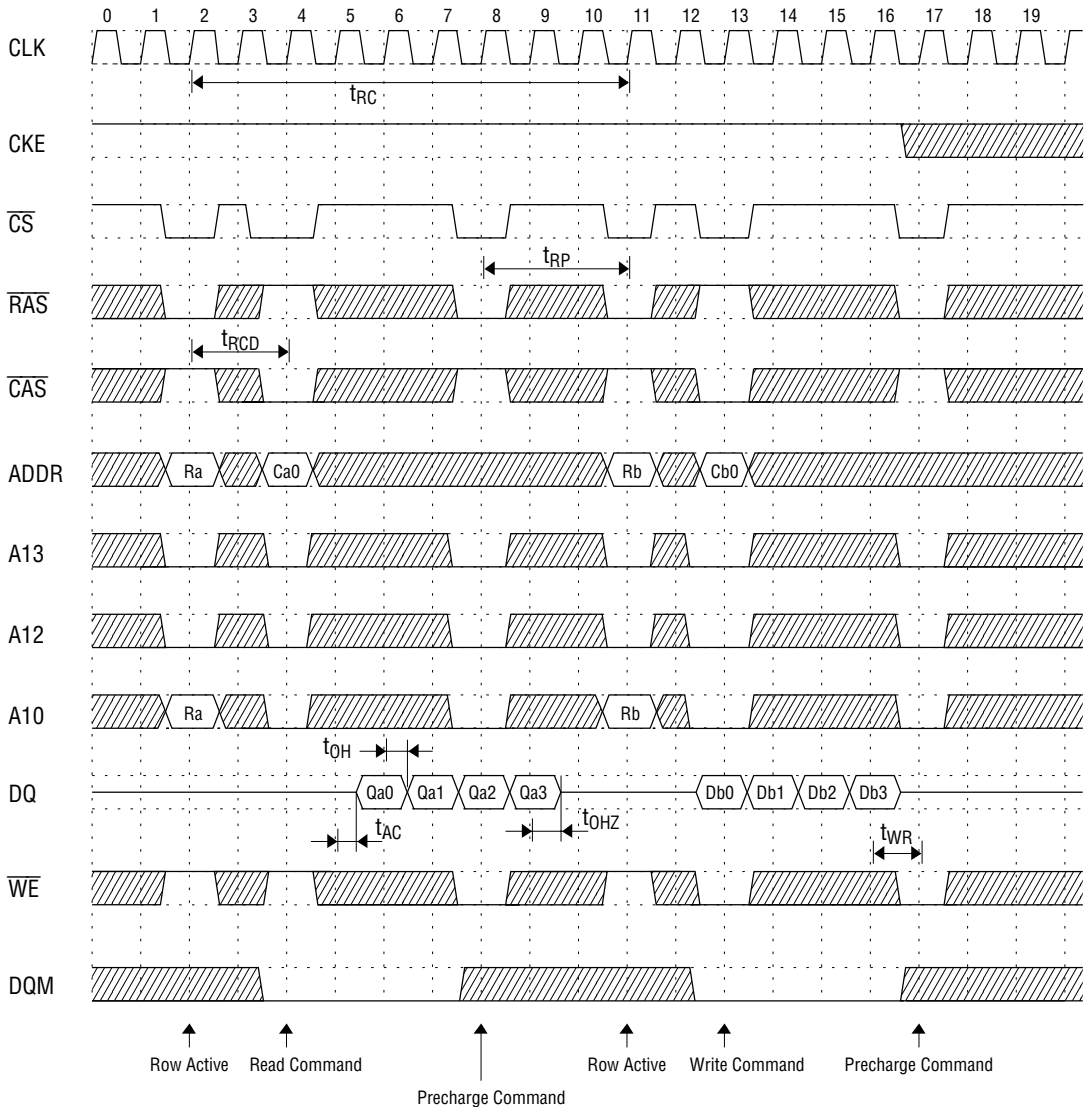
- Notes :
1. AC measurements assume that  $t_T = 1$  ns.
  2. The reference level for timing of input signals is 1.4 V.
  3. Output load.



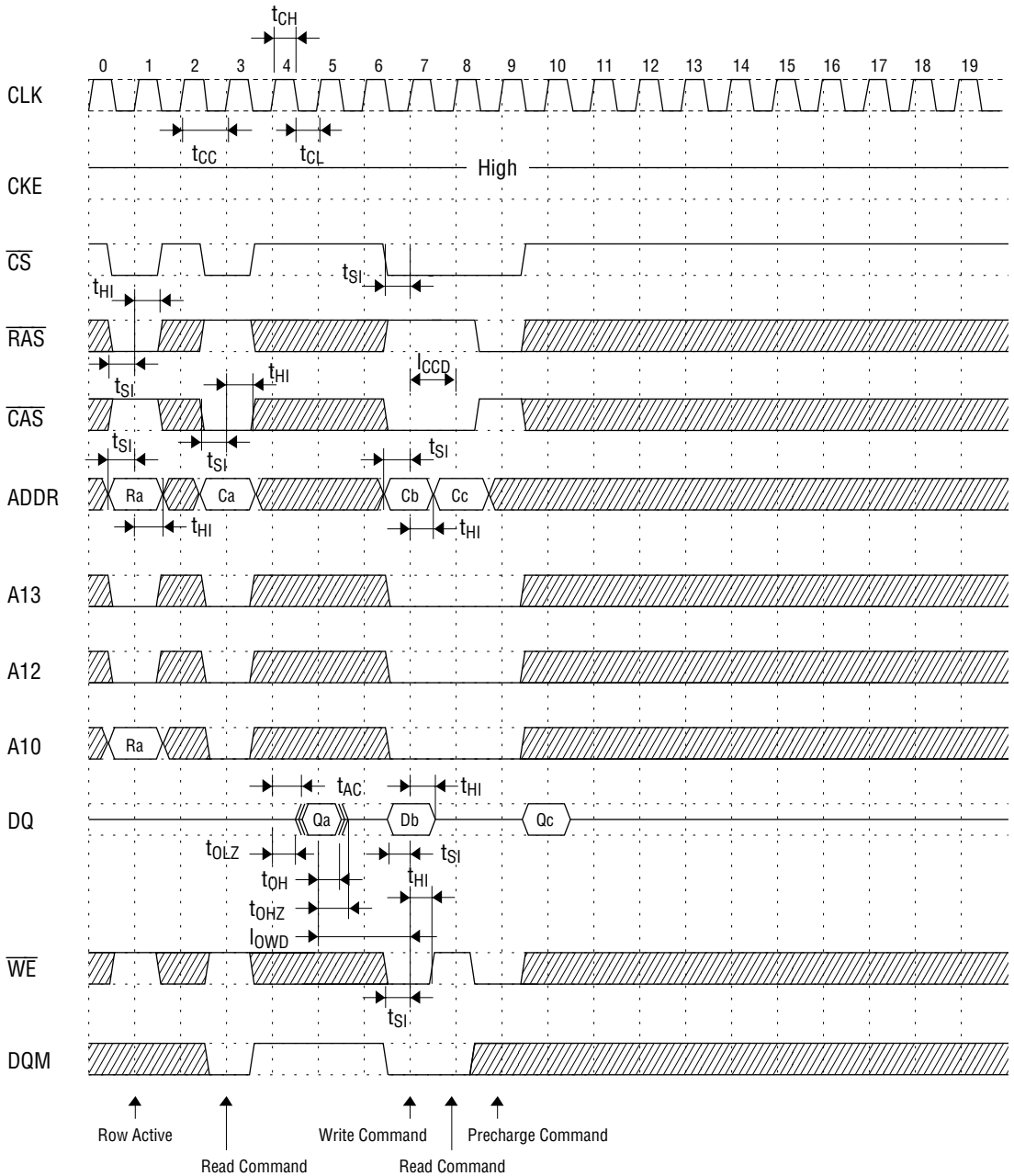
4. The access time is defined at 1.4 V.
5. If  $t_T$  is longer than 1 ns, then the reference level for timing of input signals is  $V_{IH}$  and  $V_{IL}$ .

**TIMING WAVEFORM**

**Read & Write Cycle (Same Bank) @  $\overline{\text{CAS}}$  Latency = 2, Burst Length = 4**



Single Bit Read-Write-Read Cycle (Same Page) @  $\overline{\text{CAS}}$  Latency = 2, Burst Length = 4



- \*Notes:**
1. When  $\overline{CS}$  is set "High" at a clock transition from "Low" to "High", all inputs except CKE and DQM are invalid.
  2. When issuing an active, read or write command, the bank is selected by A12 and A13.

A12	A13	Active, read or write
0	0	Bank A
0	1	Bank B
1	0	Bank C
1	1	Bank D

3. The auto precharge function is enabled or disabled by the A10 input when the read or write command is issued.

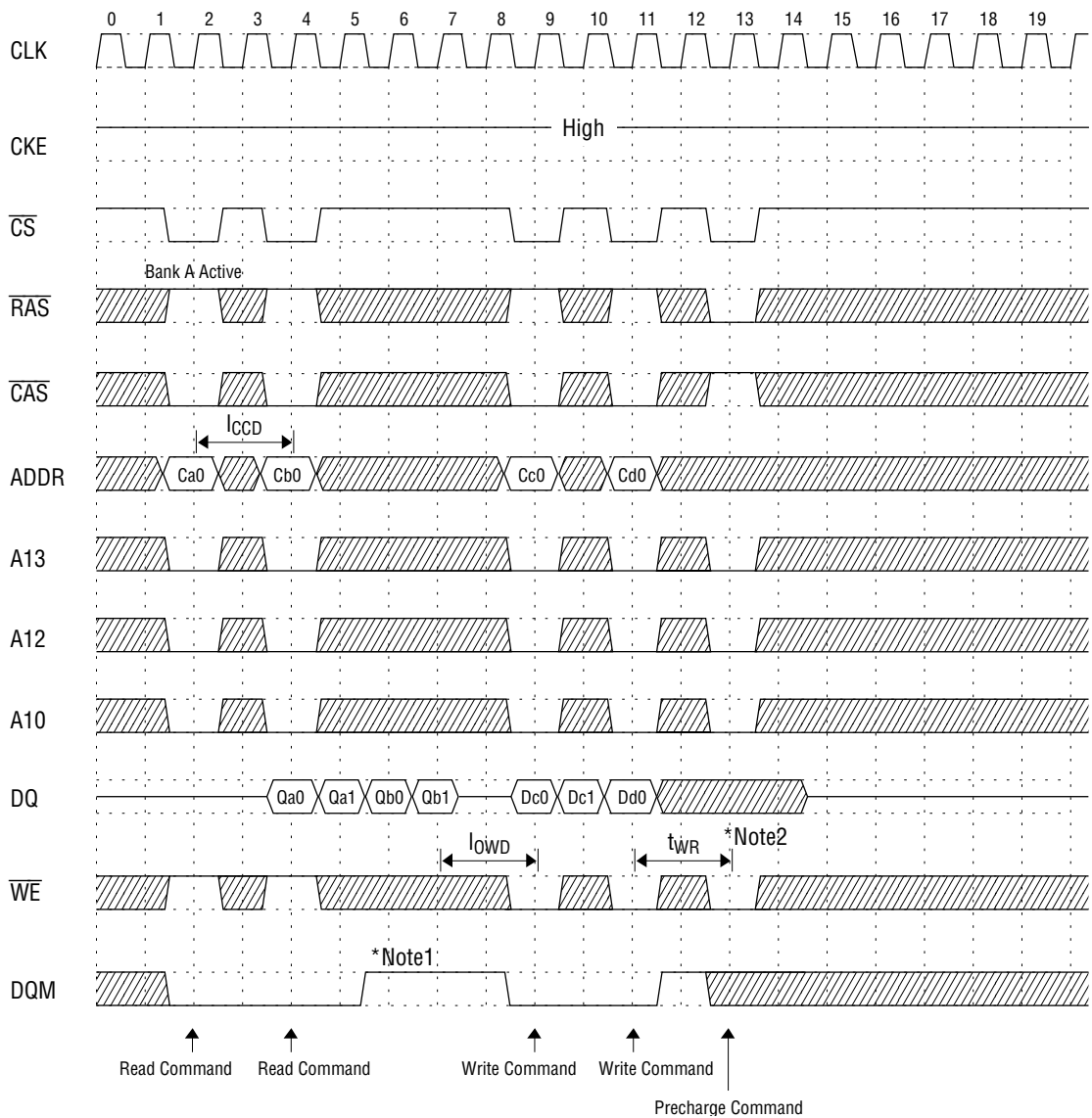
A10	A12	A13	Operation
0	0	0	After the end of burst, bank A holds the idle status.
1	0	0	After the end of burst, bank A is precharged automatically.
0	0	1	After the end of burst, bank B holds the idle status.
1	0	1	After the end of burst, bank B is precharged automatically.
0	1	0	After the end of burst, bank C holds the idle status.
1	1	0	After the end of burst, bank C is precharged automatically.
0	1	1	After the end of burst, bank D holds the idle status.
1	1	1	After the end of burst, bank D is precharged automatically.

4. When issuing a precharge command, the bank to be precharged is selected by the A10, A12 and A13 inputs.

A10	A12	A13	Operation
0	0	0	Bank A is precharged.
0	0	1	Bank B is precharged.
0	1	0	Bank C is precharged.
0	1	1	Bank D is precharged.
1	X	X	All banks are precharged.

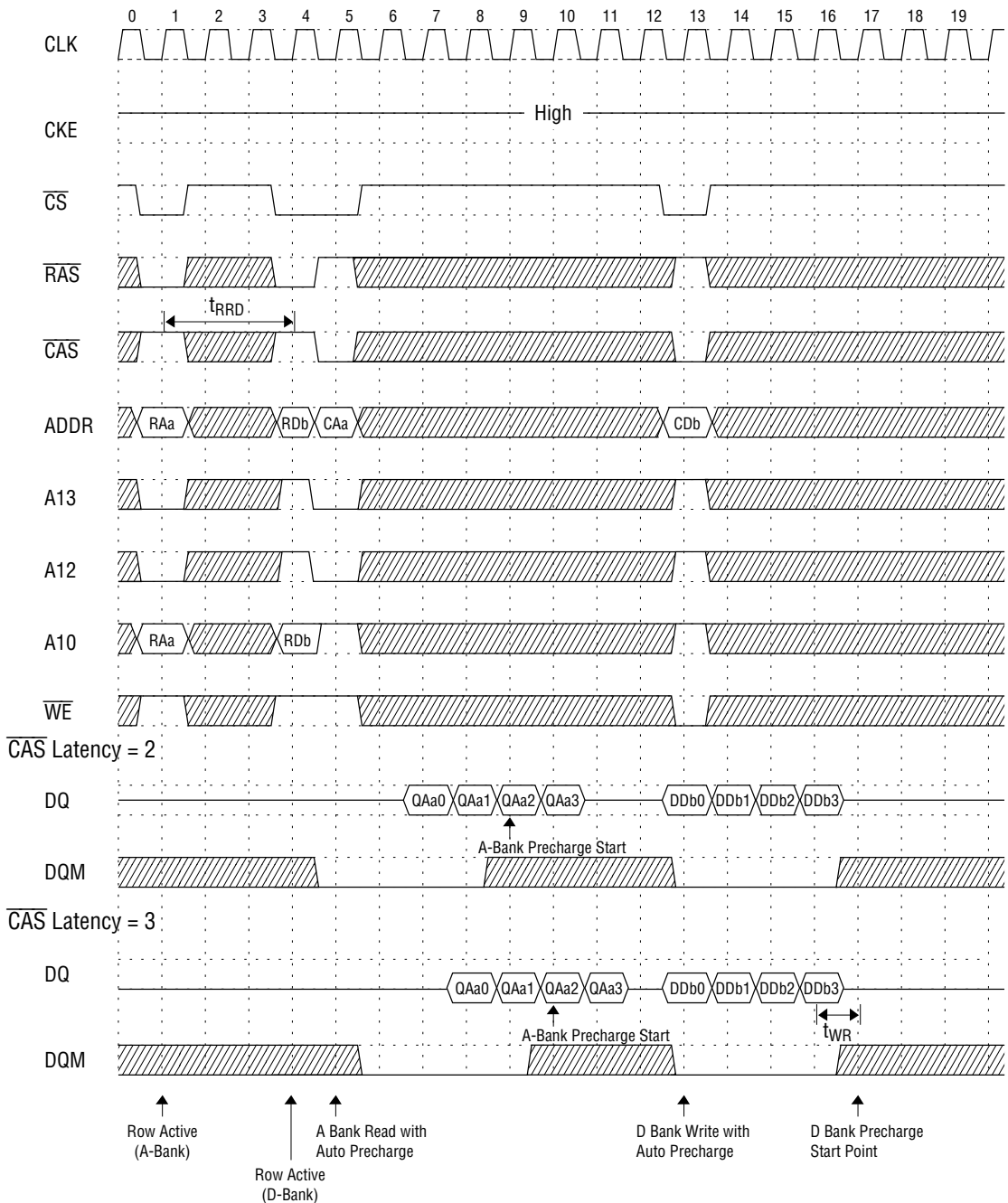
5. The input data and the write command are latched by the same clock (Write latency = 0).
6. The output is forced to high impedance by (1 CLK +  $t_{OHZ}$ ) after DQM entry.

Page Read & Write Cycle (Same Bank) @  $\overline{\text{CAS}}$  Latency = 2, Burst Length = 4

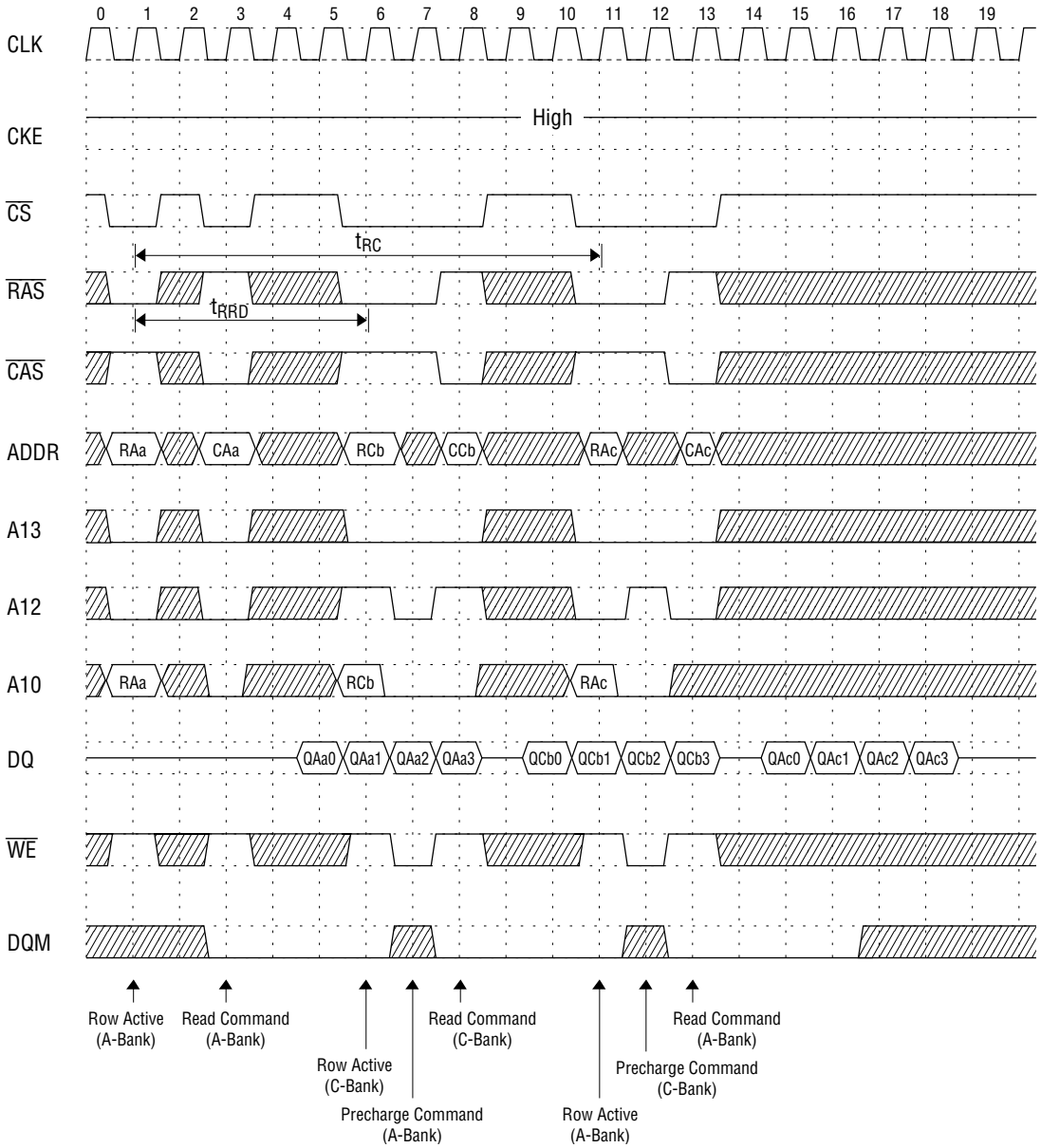


- \*Notes:**
1. To write data before a burst read ends, DQM should be asserted three cycles prior to the write command to avoid bus contention.
  2. To assert row precharge before a burst write ends, wait  $t_{\text{WR}}$  after the last write data input. Input data during the precharge input cycle will be masked internally.

Read & Write Cycle with Auto Precharge @ Burst Length = 4

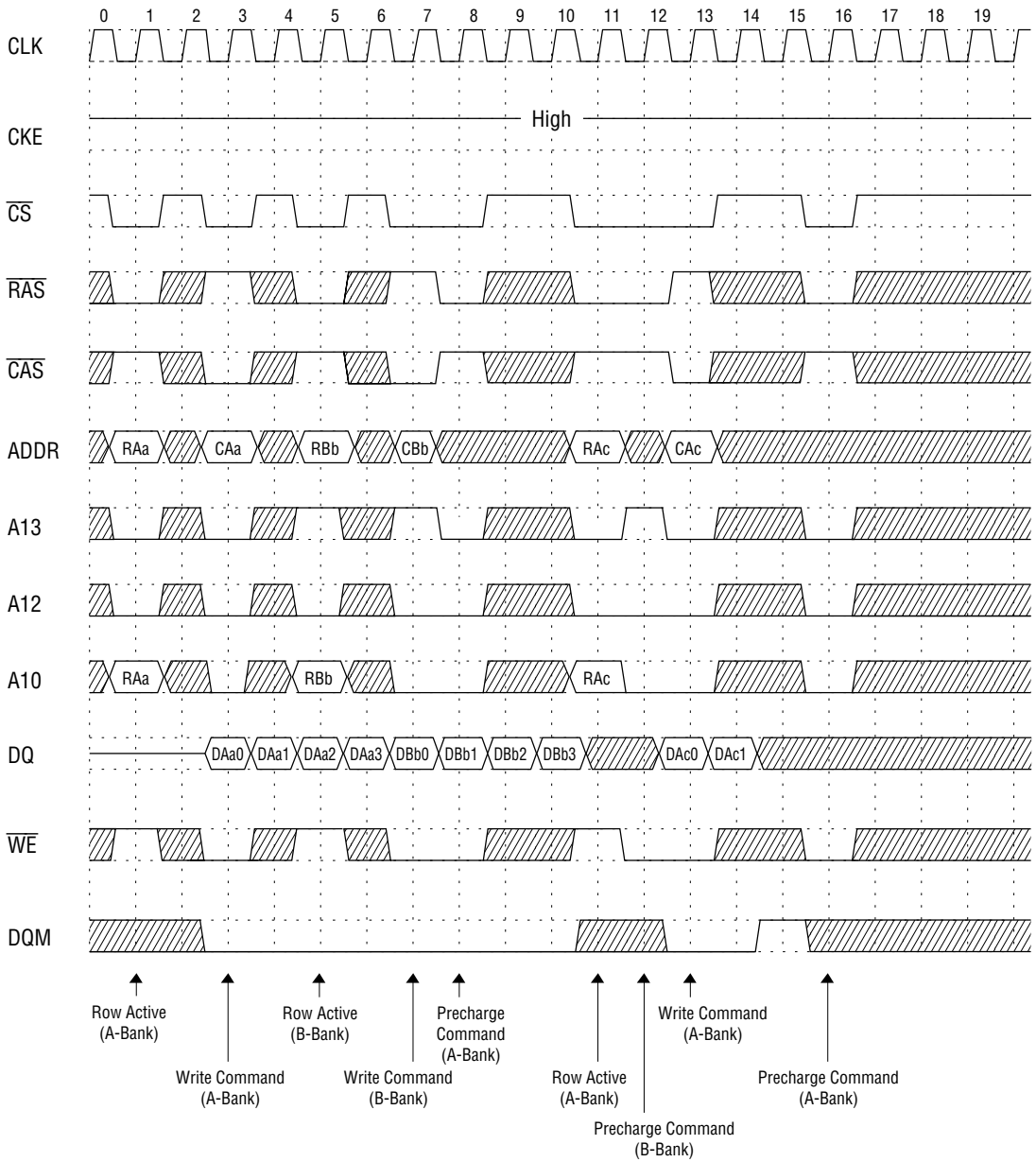


Bank Interleave Random Row Read Cycle @  $\overline{\text{CAS}}$  Latency = 2, Burst Length = 4

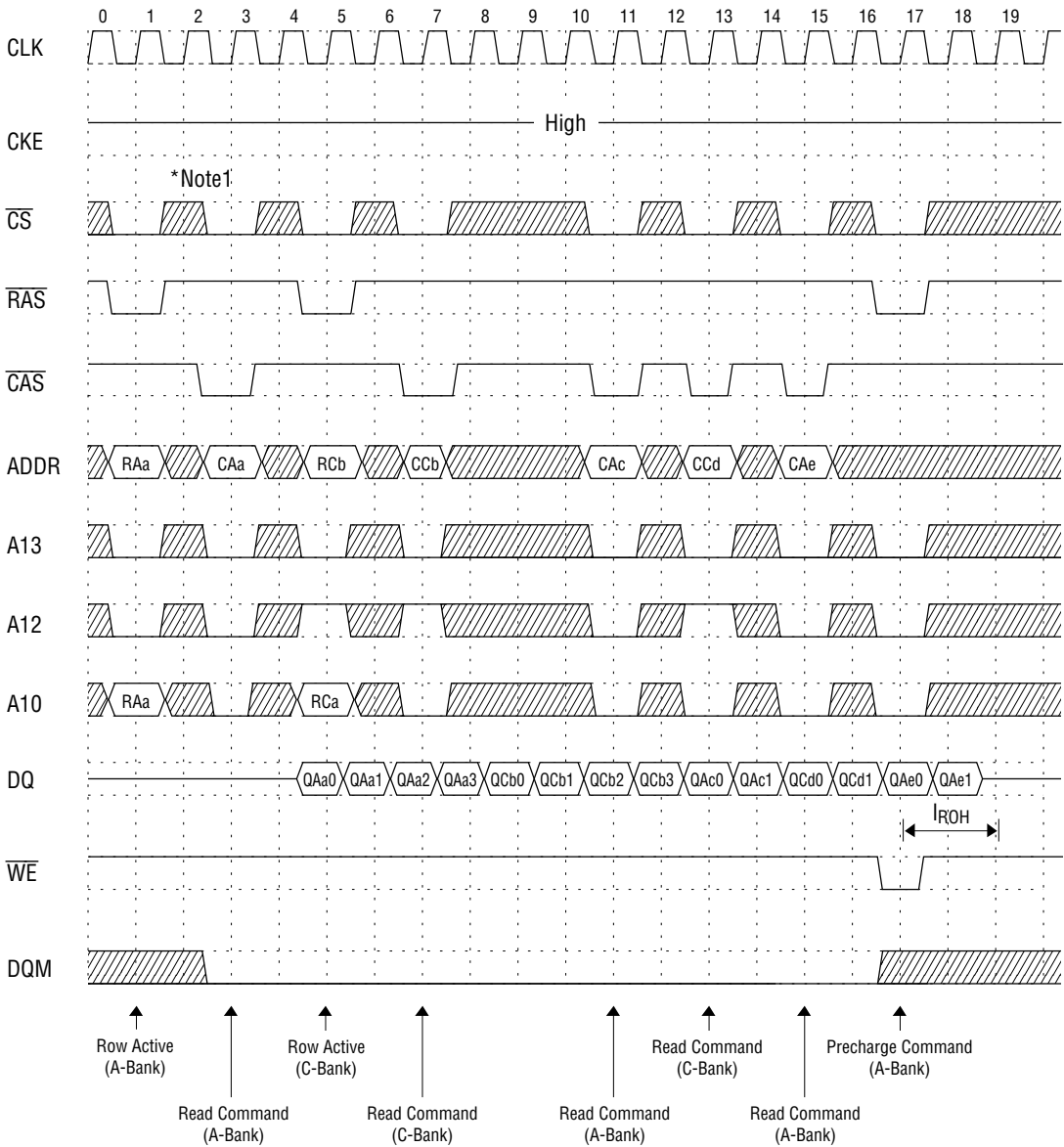




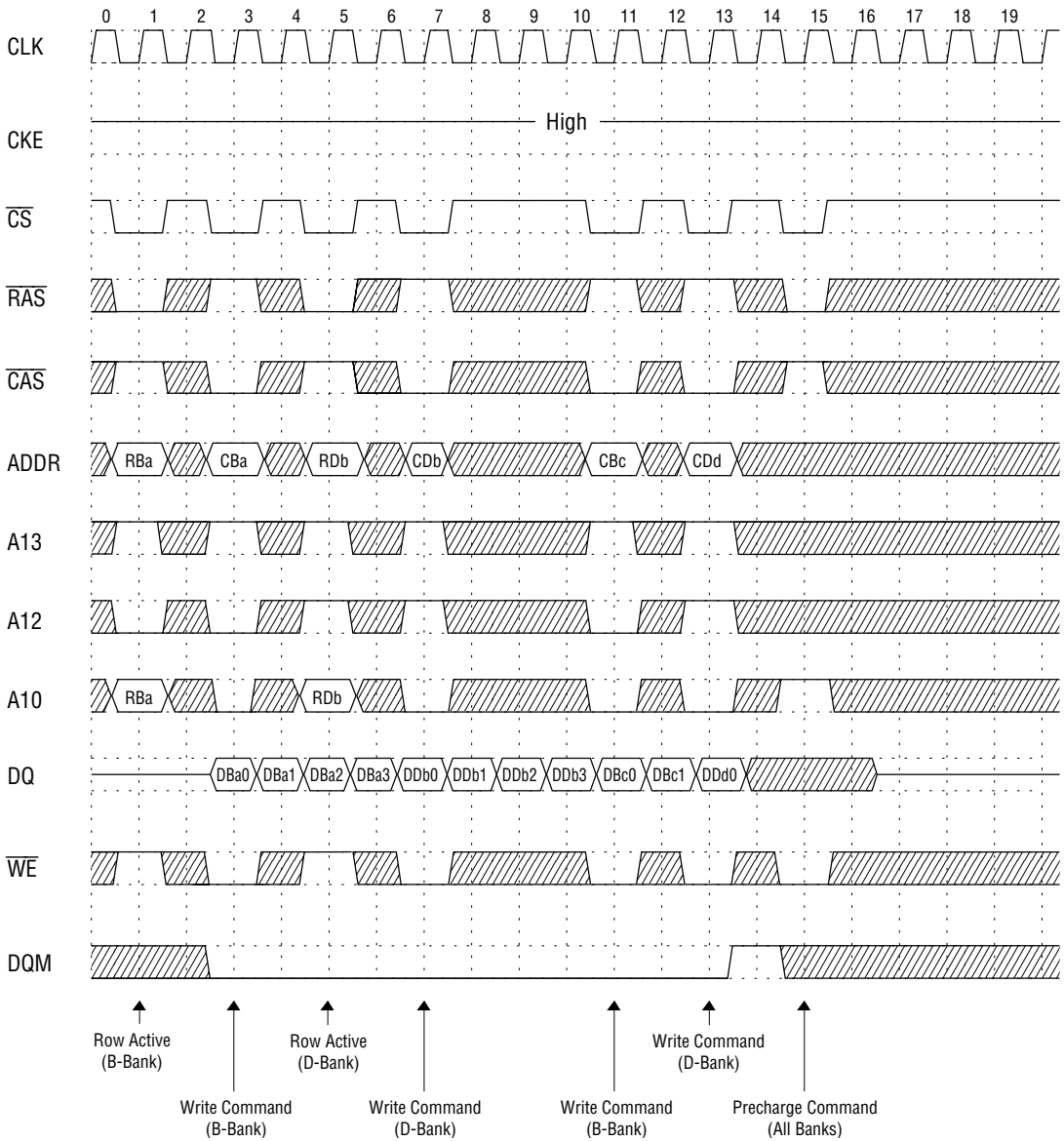
**Bank Interleave Random Row Write Cycle @  $\overline{\text{CAS}}$  Latency = 2, Burst Length = 4**



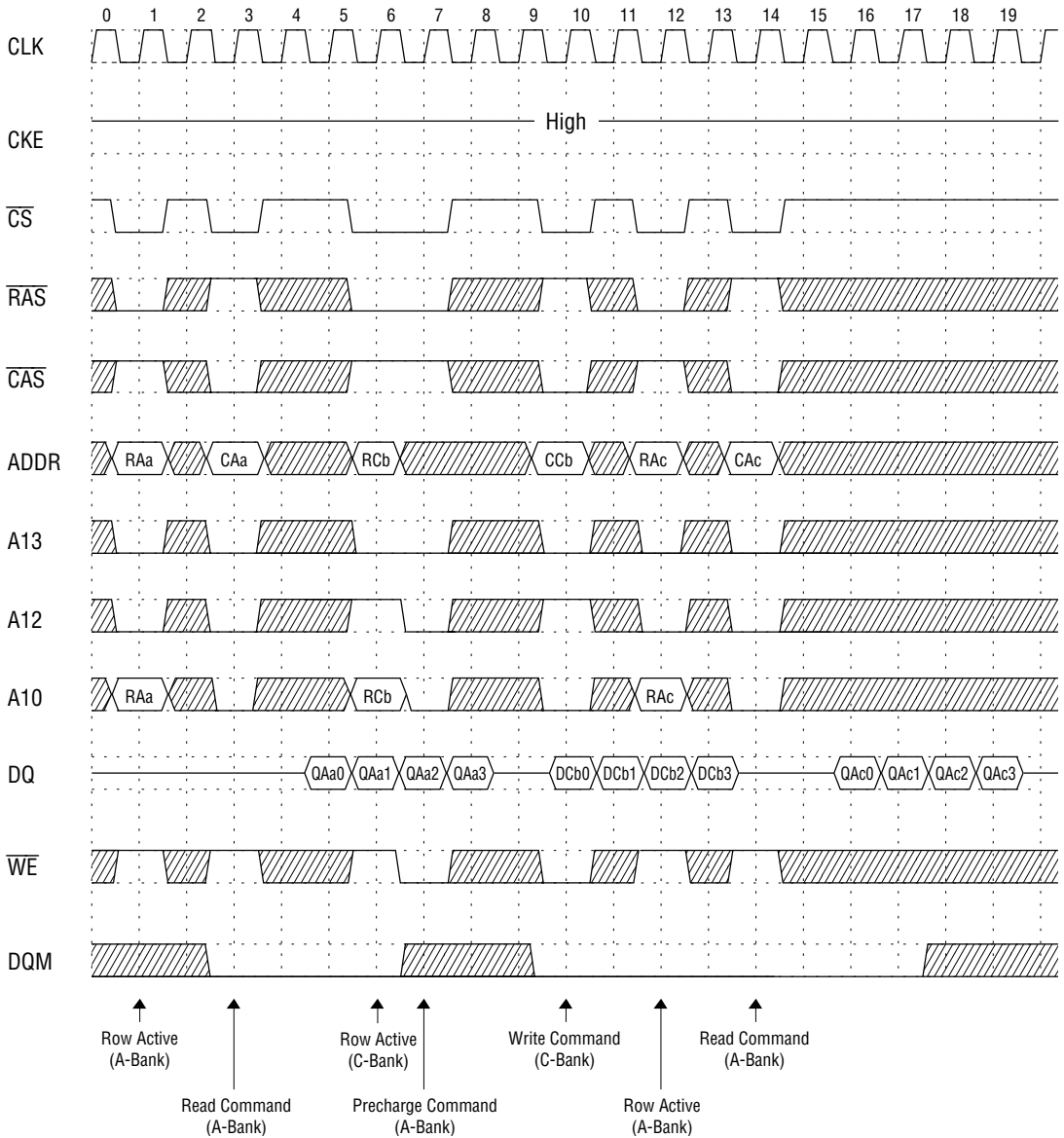
**Bank Interleave Page Read Cycle @  $\overline{\text{CAS}}$  Latency = 2, Burst Length = 4**



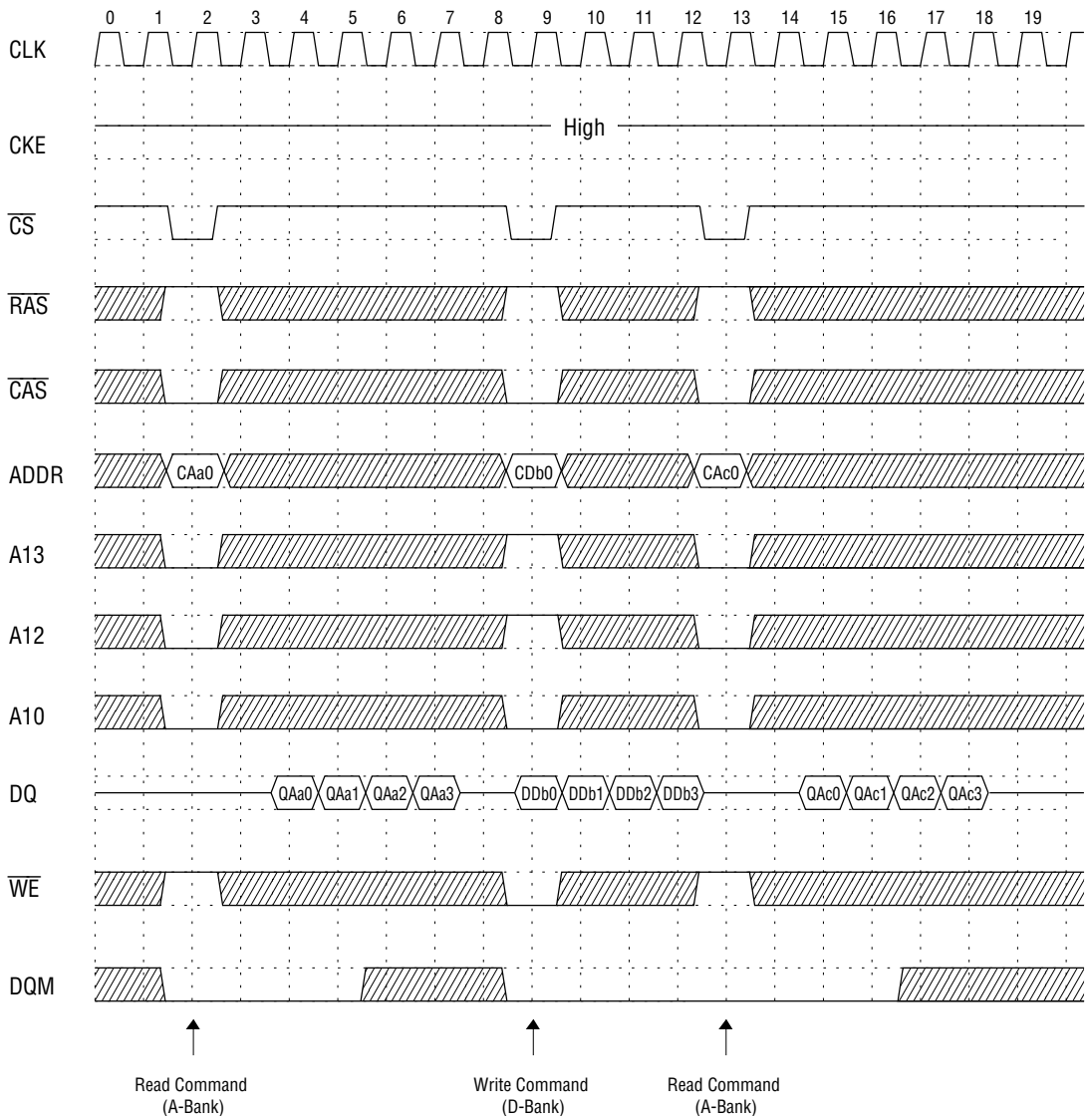
**Bank Interleave Page Write Cycle @  $\overline{\text{CAS}}$  Latency = 2, Burst Length = 4**



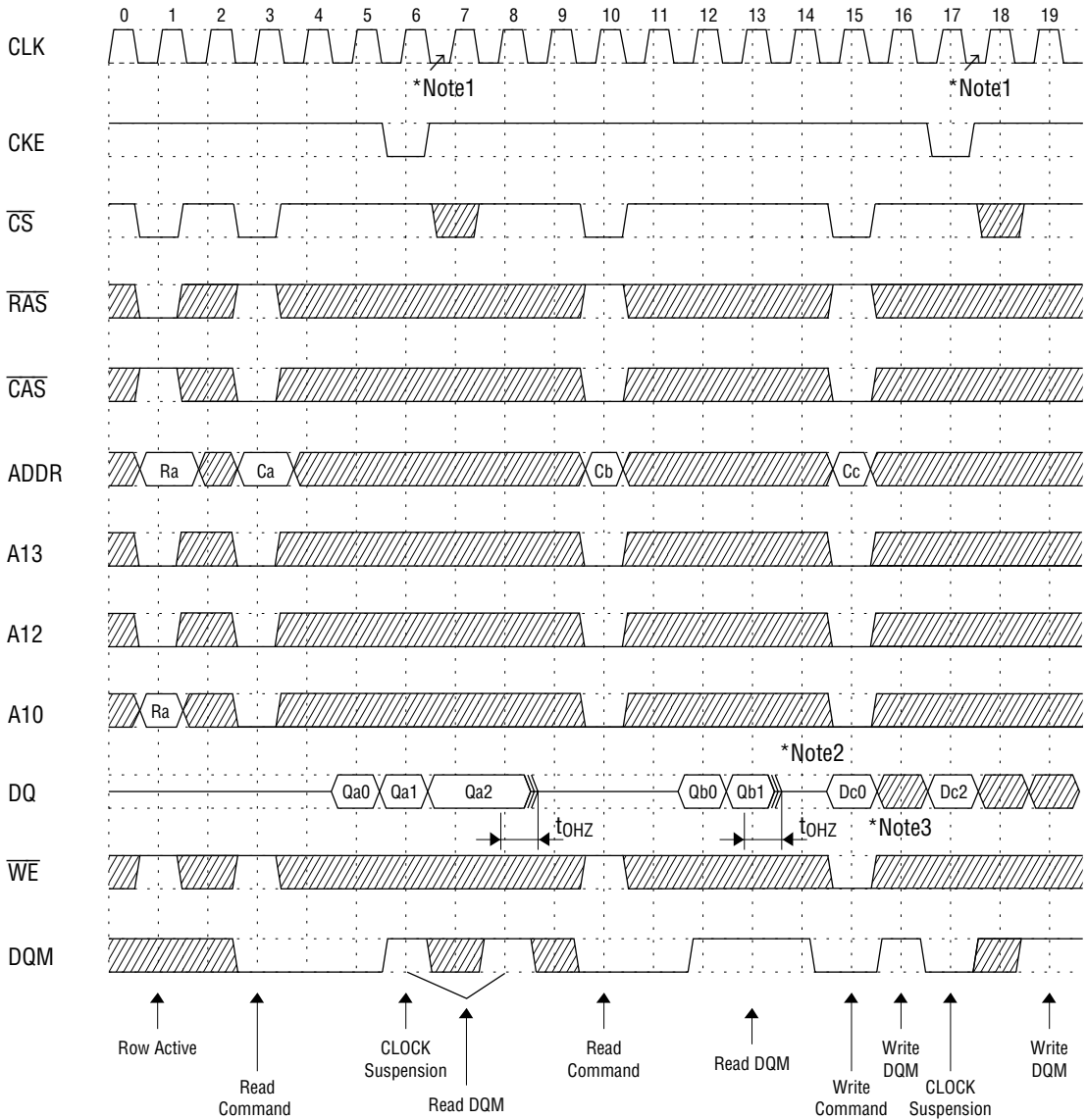
**Bank Interleave Random Row Read/Write Cycle @  $\overline{\text{CAS}}$  Latency = 2, Burst Length = 4**



Bank Interleave Page Read/Write Cycle @  $\overline{\text{CAS}}$  Latency = 2, Burst Length = 4

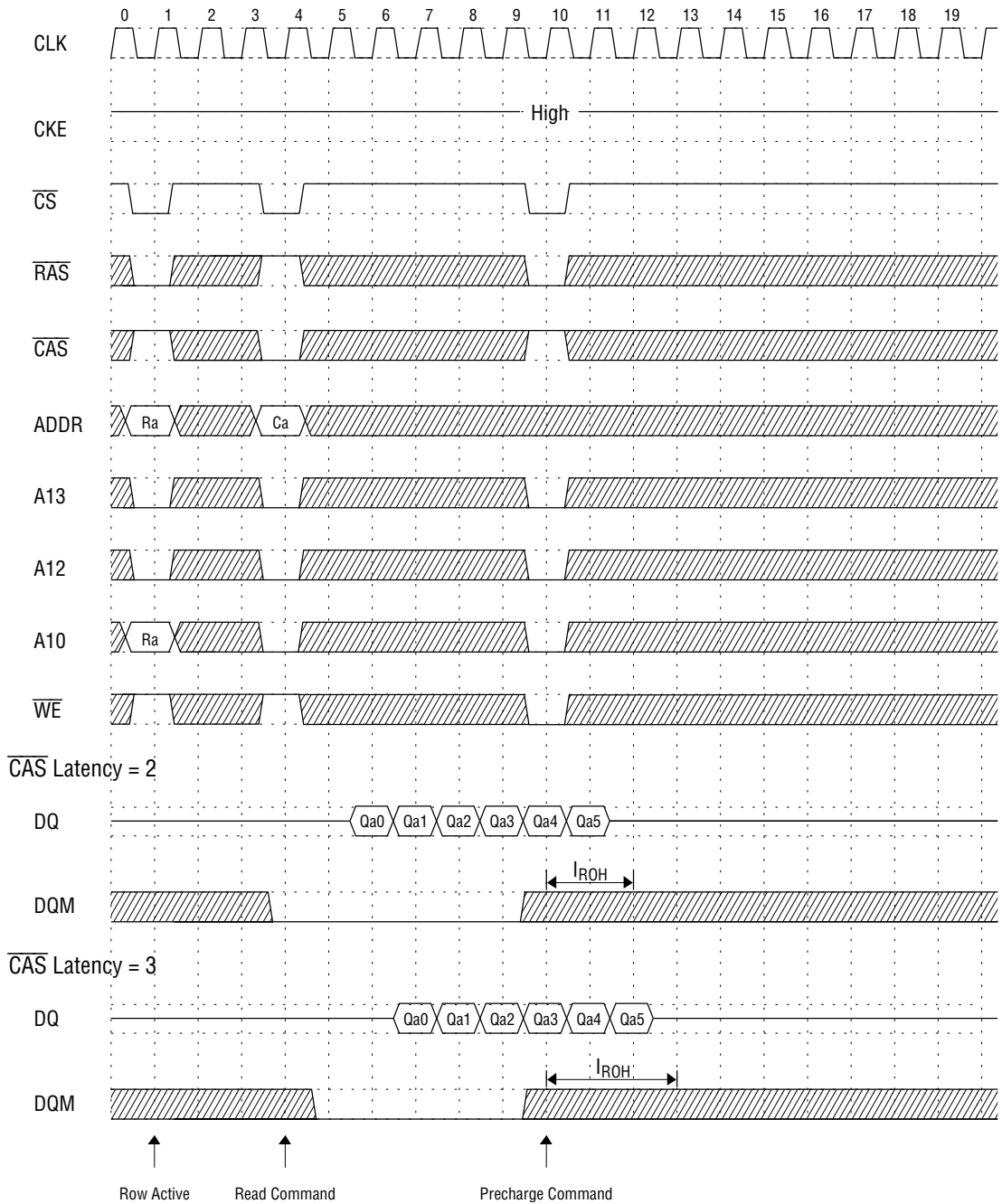


**Clock Suspension & DQM Operation Cycle @  $\overline{\text{CAS}}$  Latency = 2, Burst Length = 4**

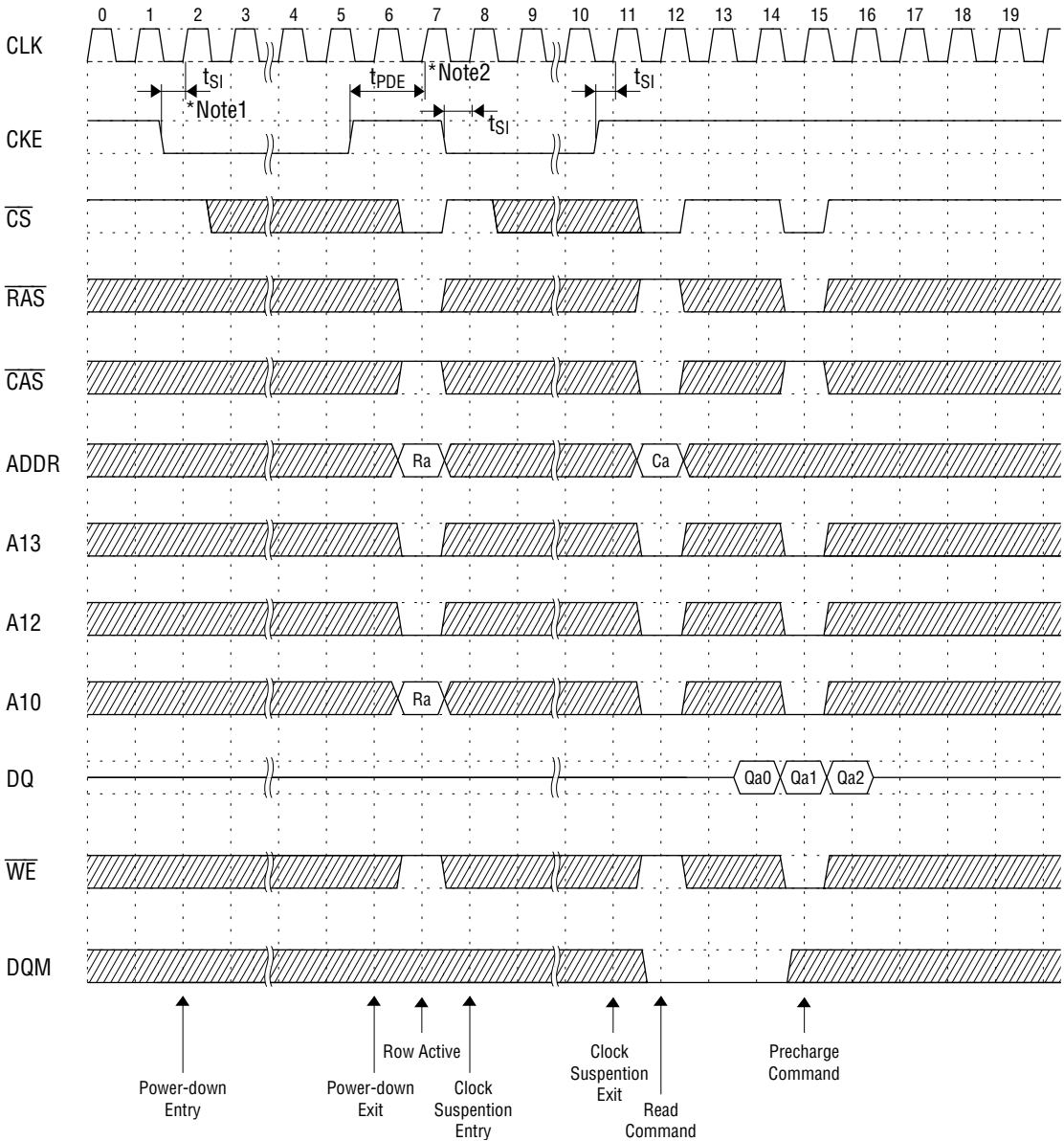


- \*Notes:**
1. When Clock Suspension is asserted, the next clock cycle is ignored.
  2. When DQM is asserted, the read data after two clock cycles is masked.
  3. When DQM is asserted, the write data in the same clock cycle is masked.

Read Interruption by Precharge Command @ Burst Length = 8



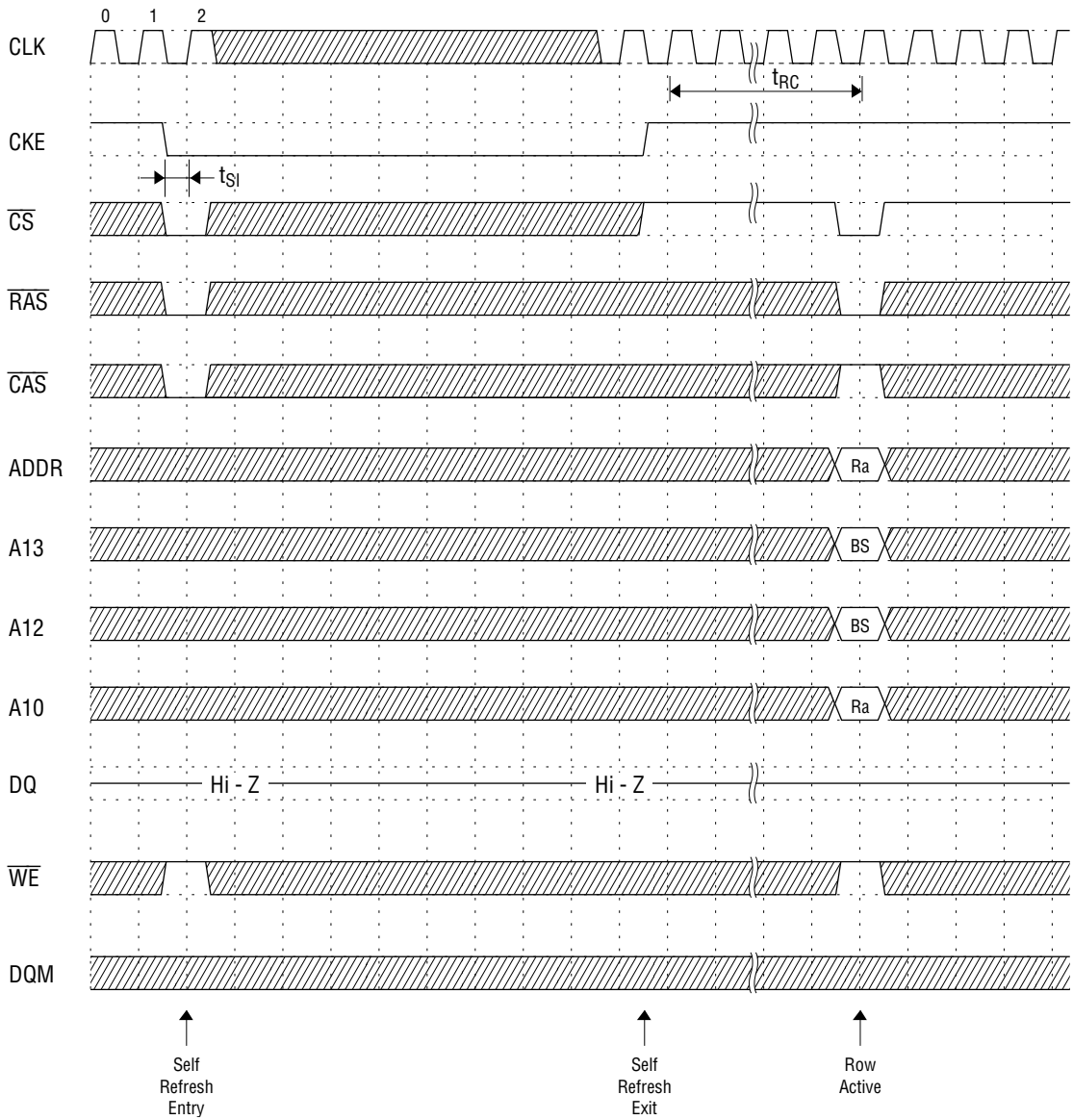
**Power Down Mode @  $\overline{\text{CAS}}$  Latency = 2, Burst Length = 4**



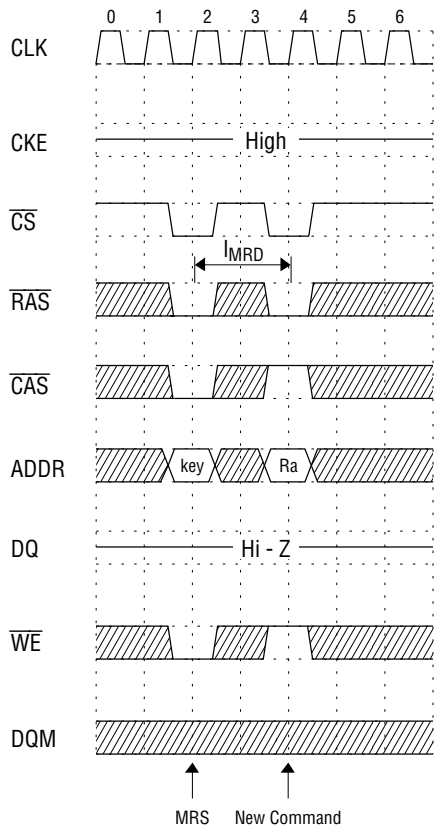
- \*Notes:**
1. When all banks are in precharge state, and if CKE is set low, then the MD56V62800A enters power-down mode and maintains the mode while CKE is low.
  2. To release the circuit from power-down mode, CKE has to be set high for  $t_{PDE}$  ( $t_{SI} + 1 \text{ CLK}$ ) or more.



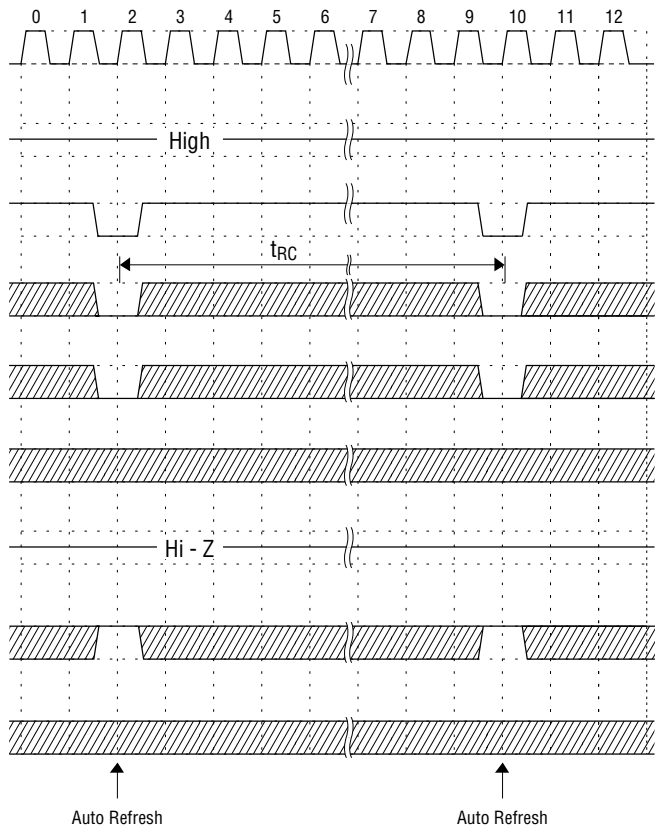
Self Refresh Cycle



Mode Register Set Cycle



Auto Refresh Cycle



**FUNCTION TRUTH TABLE (Table 1) (1/2)**

Current State <sup>1</sup>	CS	RAS	CAS	WE	BA	ADDR	Action
Idle	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	X	BA	CA	ILLEGAL <sup>2</sup>
	L	L	H	H	BA	RA	Row Active
	L	L	H	L	BA	A10	NOP <sup>4</sup>
	L	L	L	H	X	X	Auto-Refresh or Self-Refresh <sup>5</sup>
	L	L	L	L	L	OP Code	Mode Register Write
Row Active	H	X	X	X	X	X	NOP
	L	H	H	X	X	X	NOP
	L	H	L	H	BA	CA, A10	Read
	L	H	L	L	BA	CA, A10	Write
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A10	Precharge
	L	L	L	X	X	X	ILLEGAL
Read	H	X	X	X	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	H	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	L	BA	X	Term Burst
	L	H	L	H	BA	CA, A10	Term Burst, start new Burst Read
	L	H	L	L	BA	CA, A10	Term Burst, start new Burst Write
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A10	Term Burst, execute Row Precharge
	L	L	L	X	X	X	ILLEGAL
Write	H	X	X	X	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	H	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	L	BA	X	Term Burst
	L	H	L	H	BA	CA, A10	Term Burst, start new Burst Read
	L	H	L	L	BA	CA, A10	Term Burst, start new Burst Write
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A10	Term Burst, execute Row Precharge
	L	L	L	X	X	X	ILLEGAL
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	H	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	H	BA	CA, A10	ILLEGAL <sup>2</sup>
	L	H	L	L	X	X	ILLEGAL
	L	L	H	X	BA	RA, A10	ILLEGAL <sup>2</sup>
	L	L	L	X	X	X	ILLEGAL
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	H	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	H	BA	CA, A10	ILLEGAL <sup>2</sup>
	L	H	L	L	X	X	ILLEGAL
	L	L	H	X	BA	RA, A10	ILLEGAL <sup>2</sup>
	L	L	L	X	X	X	ILLEGAL

**FUNCTION TRUTH TABLE (Table 1) (2/2)**

Current State <sup>1</sup>	CS	RAS	CAS	WE	BA	ADDR	Action
Precharge	H	X	X	X	X	X	NOP --> Idle after t <sub>RP</sub>
	L	H	H	H	X	X	NOP --> Idle after t <sub>RP</sub>
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	X	BA	CA	ILLEGAL <sup>2</sup>
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A10	NOP <sup>4</sup>
	L	L	L	X	X	X	ILLEGAL
Write Recovery	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	X	BA	CA	ILLEGAL <sup>2</sup>
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A10	ILLEGAL <sup>2</sup>
	L	L	L	X	X	X	ILLEGAL
Row Active	H	X	X	X	X	X	NOP --> Row Active after t <sub>RCD</sub>
	L	H	H	H	X	X	NOP --> Row Active after t <sub>RCD</sub>
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	X	BA	CA	ILLEGAL <sup>2</sup>
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A10	ILLEGAL <sup>2</sup>
	L	L	L	X	X	X	ILLEGAL
Refresh	H	X	X	X	X	X	NOP --> Idle after t <sub>RC</sub>
	L	H	H	X	X	X	NOP --> Idle after t <sub>RC</sub>
	L	H	L	X	X	X	ILLEGAL
	L	L	H	X	X	X	ILLEGAL
	L	L	L	X	X	X	ILLEGAL
Mode Register Access	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	X	X	ILLEGAL
	L	H	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	ILLEGAL

**ABBREVIATIONS**

RA = Row Address

BA = Bank Address

NOP = No Operation command

CA = Column Address

AP = Auto Precharge

- Notes:
1. All inputs are enabled when CKE is set high for at least 1 cycle prior to the inputs.
  2. Illegal to bank in specified state, but may be legal in some cases depending on the state of bank selection.
  3. Satisfy the timing of I<sub>CCD</sub> and t<sub>WR</sub> to prevent bus contention.
  4. NOP to bank precharging or in idle state. Precharges activated bank by BA or A10.
  5. Illegal if any bank is not idle.

**FUNCTION TRUTH TABLE for CKE (Table 2)**

Current State (n)	CKEn-1	CKEn	CS	RAS	CAS	WE	ADDR	Action
Self Refresh	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self Refresh --> ABI
	L	H	L	H	H	H	X	Exit Self Refresh --> ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)
Power Down	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Power Down --> ABI
	L	H	L	H	H	H	X	Exit Power Down --> ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL <sup>6</sup>
	L	L	X	X	X	X	X	NOP (Continue power down mode)
All Banks Idle <sup>6</sup> (ABI)	H	H	X	X	X	X	X	Refer to Table 1
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	L	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self Refresh
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
Any State Other than Listed Above	H	H	X	X	X	X	X	Refer to Operations in Table 1
	H	L	X	X	X	X	X	Begin Clock Suspend Next Cycle
	L	H	X	X	X	X	X	Enable Clock of Next Cycle
	L	L	X	X	X	X	X	Continue Clock Suspension

Note: 6. Power-down and self refresh can be entered only when all the banks are in an idle state.