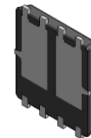
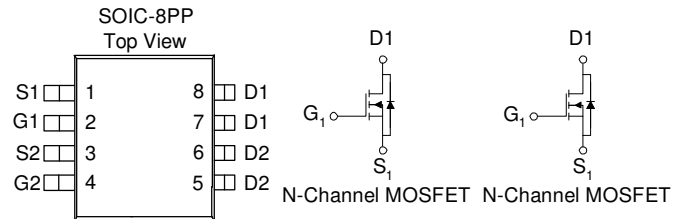


Dual N-Channel 40-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOIC-8PP saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
40	19 @ $V_{GS} = 10V$	24
	22 @ $V_{GS} = 4.5V$	22



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	20	
Continuous Drain Current ^a	$T_A=25^\circ C$	I_D	24	A
	$T_A=70^\circ C$		20	
Pulsed Drain Current ^b		I_{DM}	± 50	
Continuous Source Current (Diode Conduction) ^a		I_S	13	A
Power Dissipation ^a	$T_A=25^\circ C$	P_D	16	W
	$T_A=70^\circ C$		10	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	$R_{\theta JA}$	35	$^\circ C/W$
	Steady State	$R_{\theta JC}$	8	

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

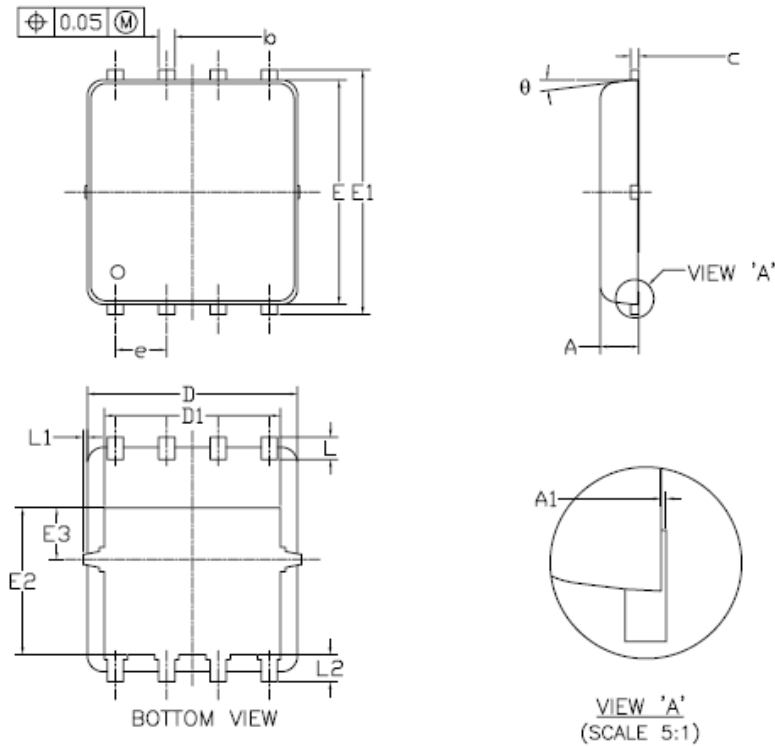
SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250 μA	1			V
Gate-Body Leakage	I _{GSS}	V _{GS} = 20 V, V _{DS} = 0 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V			1	μA
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	20			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 10 V, I _D = 1 A			19	mΩ
		V _{GS} = 4.5 V, I _D = 1 A			22	
Forward Transconductance ^A	g _{fs}	V _{DS} = 15 V, I _D = 1 A		40		S
Dynamic						
Total Gate Charge	Q _g	N-Channel V _{DS} =15V, V _{GS} =4.5V, I _D =1A		10		nC
Gate-Source Charge	Q _{gs}			2		
Gate-Drain Charge	Q _{gd}			2		
Input Capacitance	C _{iss}	N-Channel V _{DS} =15V, V _{GS} =0V, f=1MHz		600		pF
Output Capacitance	C _{oss}			100		
Reverse Transfer Capacitance	C _{rss}			50		
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} =15V, V _{GS} =10V, I _D =1A , R _{GEN} =25Ω		12		nS
Rise Time	t _r			14		
Turn-Off Delay Time	t _{d(off)}			20		
Fall-Time	t _f			10		

Notes

- Pulse test: PW ≤ 300μs duty cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.

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Package Information



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.95	1.00	0.033	0.037	0.039
A1	0.00	—	0.05	0.000	—	0.002
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.15	0.20	0.25	0.006	0.008	0.010
D	5.20 BSC			0.205 BSC		
D1	4.35 BSC			0.171 BSC		
E	5.55 BSC			0.219 BSC		
E1	6.05 BSC			0.238 BSC		
E2	3.625 BSC			0.143 BSC		
E3	1.275 BSC			0.050 BSC		
e	1.27 BSC			0.050 BSC		
L	0.45	0.55	0.65	0.018	0.022	0.026
L1	0	—	0.15	0	—	0.006
L2	0.68 REF			0.027 REF		
θ	0°	—	10°	0°	—	10°