13. ELECTRICAL SPECIFICATIONS

13.1 Absolute Maximum Ratings

Description	Absolute Maximum Rating[a]
Ambient temperature under bias	0°C to 70°C
Storage temperature	–65°C to 150°C
Voltage on any pin (with respect to ground)	–0.3 volts to 0.3 volts greater than voltage of the +5V pin, respective to ground
Operating power dissipation	500 mW
Power dissipation during Suspend mode	10 mW
Power supply voltage	7 volts
Injection current (latch up)	25 mA

[a] Stresses above those listed may cause permanent damage to system components. These are stress ratings only; functional operation at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect system reliability.

13.2 DC Specifications

Table 13–1. General DC Specifications

Symbol	Parameter	MIN	MAX	Unit	Conditions
C_{IN}	Input capacitance		10.0	pF	
C_{OUT}	Output capacitance		10.0	pF	
I_{IL}	Input leakage	–10.0	10.0	µA	$0 < V_{IN} <$ respective V_{CC} supply pin
I_{PU}	Internal pull-up current	–30	–400	µA	

Table 13–2. PCMCIA Bus Interface DC Specifications

Symbol	Parameter	MIN	MAX	Unit	Conditions
$SOCKET\_VCC_{5V}$	Power supply voltage	4.5	5.5	V	Normal operation
$SOCKET\_VCC_{3V}$		3.0	3.6	V	
V_{IH}	Input high voltage	2.0		V	V_{DD} core voltage = 3.0V, **Misc Control 2** register, bit 3 = '0'
		2.0		V	V_{DD} core voltage = 4.5V, **Misc Control 2** register, bit 3 = '1'
V_{IL}	Input low voltage		0.8	V	V_{DD} core voltage = 3.6V, **Misc Control 2** register, bit 3 = '0'
			0.8	V	V_{DD} core voltage = 5.5V, **Misc Control 2** register, bit 3 = '1'
V_{IHC}	Input high voltage CMOS	0.7 V_{DD}		V	V_{DD} core voltage = 4.5V, **Misc Control 2** register, bit 3 = '0'
V_{ILC}	Input low voltage CMOS		0.2 V_{DD}	V	V_{DD} core voltage = 5.5V, **Misc Control 2** register, bit 3 = '0'
V_{OH}	Output high voltage	2.4		V	At rated I_{OH}, respective SOCKET_VCC = 3.0V
V_{OHC}	Output high voltage CMOS	SOCKET_VCC – 0.5		V	At rated I_{OHC}, respective SOCKET_VCC = 3.0V
V_{OL}	Output low voltage		0.4	V	At rated I_{OL}
I_{OH}	Output high current	–2		mA	Respective SOCKET_VCC = 3.0V, V_{OH} = 2.4V
I_{OHC}	Output high current CMOS	–1		mA	Respective SOCKET_VCC = 3.0V, V_{OHC} = SOCKET_VCC – 0.5V
I_{OL}	Output low current	2		mA	Respective SOCKET_VCC = 3.0V, V_{OL} = 0.4V

Table 13–3. PCI Bus Interface DC Specifications

Symbol	Parameter	MIN	MAX	Unit	Conditions
PCI_VCC_{5V}	Power supply voltage	4.5	5.5	V	Normal operation
PCI_VCC_{3V}		3.0	3.6	V	
V_{IH}[a]	Input high voltage	2.0		V	V_{DD} core voltage = 3.0V
V_{IL}[a]	Input low voltage		0.8	V	V_{DD} core voltage = 3.6V
V_{IHC}[a]	Input high voltage CMOS	0.7 V_{DD}[b]		V	V_{DD} core voltage = 4.5V
V_{ILC}[a]	Input low voltage CMOS		0.2 V_{DD}[b]	V	V_{DD} core voltage = 5.5V
V_{OH}	Output high voltage	2.4		V	At rated I_{OH}, PCI_VCC = 3.0V
V_{OHC}	Output high voltage CMOS	PCI_VCC – 0.5		V	At rated I_{OHC}, PCI_VCC = 3.0V
V_{OL}	Output low voltage		0.5	V	At rated I_{OL}
I_{OH}	Output current high	–5		mA	PCI_VCC = 3.0V, V_{OH} = 2.4V
I_{OHC}	Output current high CMOS	–1		mA	PCI_VCC = 3.0V, V_{OHC} = PCI_VCC – 0.5V
I_{OL}	Output current low	16		mA	PCI_VCC = 3.0V, V_{OL} = 0.5V

[a] When CORE_VDD is 3.3V, input thresholds are TTL-compatible; when CORE_VDD is 5V, input thresholds are CMOS-compatible.

[b] The value of the input threshold level is dependent on the voltage applied to the CORE_VDD pin of the CL-PD6729.

Table 13–4. Power Control Interface (+5V Powered) DC Specifications

Symbol	Parameter	MIN	MAX	Unit	Conditions
+5V	+5V supply voltage	Highest V_{CC} – 0.3	5.5	V	
V_{IH}	Input high voltage	2.0		V	+5V pin voltage = 4.5V
V_{IL}	Input low voltage		0.8	V	+5V pin voltage = 5.5V
V_{OH}	Output high voltage	2.4		V	+5V pin voltage = 4.5V, I_{OH} = –5 mA
V_{OHC}	Output high voltage CMOS	+5V voltage – 0.5		V	+5V pin voltage = 4.5V, I_{OH} = –1 mA
V_{OL}	Output low voltage		0.4	V	
I_{OH}	Output current high	–5		mA	Respective +5V pin voltage = 4.5V, V_{OH} = 2.4V
I_{OHC}	Output current high CMOS	–1		mA	Respective +5V pin voltage = 4.5V, V_{OHC} = +5V pin voltage – 0.5V
I_{OL}	Output current low	16		mA	Respective +5V pin voltage = 4.5V, V_{OL} = 0.4V

Table 13–5. Operating Current Specifications (3.3V)

Symbol	Parameter	MIN	TYP	MAX	Unit	Conditions
$Icc_{tot(1)}$	Power supply current, operating	tbd	tbd	tbd	mA	CORE_VDD = 3.3V; +5V, SOCKET_VCC, and PCI_VCC = 5.0V; P_{DISS} = < 85 mW
$Icc_{tot(2)}$	Power supply current, Suspend mode (**Misc Control 2**, bit 2 = '1')		tbd		µA	CORE_VDD = 3.3V; +5V, SOCKET_VCC, and PCI_VCC = 5.0V; P_{DISS} = < 2 mW
$Icc_{tot(3)}$	Power supply current, RST# active, no clocks		tbd		µA	CORE_VDD = 3.3V; +5V, SOCKET_VCC, and PCI_VCC = 5.0V; P_{DISS} = < 1 mW

Table 13–6. Operating Current Specifications (5.0V)

Symbol	Parameter	MIN	TYP	MAX	Unit	Conditions
$Icc_{tot(1)}$	Power supply current, operating	tbd	tbd	tbd	mA	CORE_VDD, +5V, SOCKET_VCC, and PCI_VCC = 5.0V
$Icc_{tot(2)}$	Power supply current, Suspend mode (**Misc Control 2**, bit 2 = '1')		tbd		µA	CORE_VDD, +5V, SOCKET_VCC, and PCI_VCC = 5.0V
$Icc_{tot(3)}$	Power supply current, RST# active, no clocks		tbd		µA	CORE_VDD, +5V, SOCKET_VCC, and PCI_VCC = 5.0V

13.3 AC Timing Specifications

This section includes system timing requirements for the CL-PD6729. Unless otherwise specified, timings are provided in nanoseconds (ns), at TTL input levels, with the ambient temperature varying from 0°C to 70°C, and V_{CC} varying from 3.0V to 3.6V or 4.5V to 5.5V DC. The PCI bus speed is 33 MHz unless otherwise specified. Note the following conventions:

- A pound sign (#) at the end of a pin name indicates an active-low signal for the PCI bus.
- A dash (-) at the beginning of a pin name indicates an active-low signal for the PCMCIA bus.
- An asterisk (*) at the end of a pin name indicates an active-low signal that is a general-interface for the CL-PD6729.

Additionally, the following statements are true for all timing information:

- All timings assume a load of 50 pF.
- TTL signals are measured at TTL threshold; CMOS signals are measured at CMOS threshold.

Table 13–7. Index of AC Timing Specifications

13.3.1 PCI Bus Timing

Table 13–8. FRAME#, AD[31:0], C/BE[3:0]#, and DEVSEL#

Symbol	Parameter	PCI_VCC = 3.3 V		PCI_VCC = 5.0 V		Units
		MIN	MAX	MIN	MAX	
t_1	FRAME# setup to PCI_CLK	7	–	7	–	ns
t_2	AD[31:0] (address) setup to PCI_CLK	7	–	7	–	ns
t_3	AD[31:0] (address) hold from PCI_CLK	0	–	0	–	ns
t_4	AD[31:0] (data) setup to PCI_CLK	7	–	7	–	ns
t_5	AD[31:0] (data) active to HI-Z from PCI_CLK	0	28	0	28	ns
t_6	C/BE[3:0]# (bus command) setup to PCI_CLK	7	–	7	–	ns
t_7	C/BE[3:0]# (bus command) hold from PCI_CLK	0	–	0	–	ns
t_8	C/BE[3:0]# (byte enable) setup to PCI_CLK	7	–	7	–	ns
t_9	DEVSEL# delay from PCI_CLK	–	11	–	11	ns
t_{10}	DEVSEL# high before HI-Z	1	–	1	–	PCI_CLK

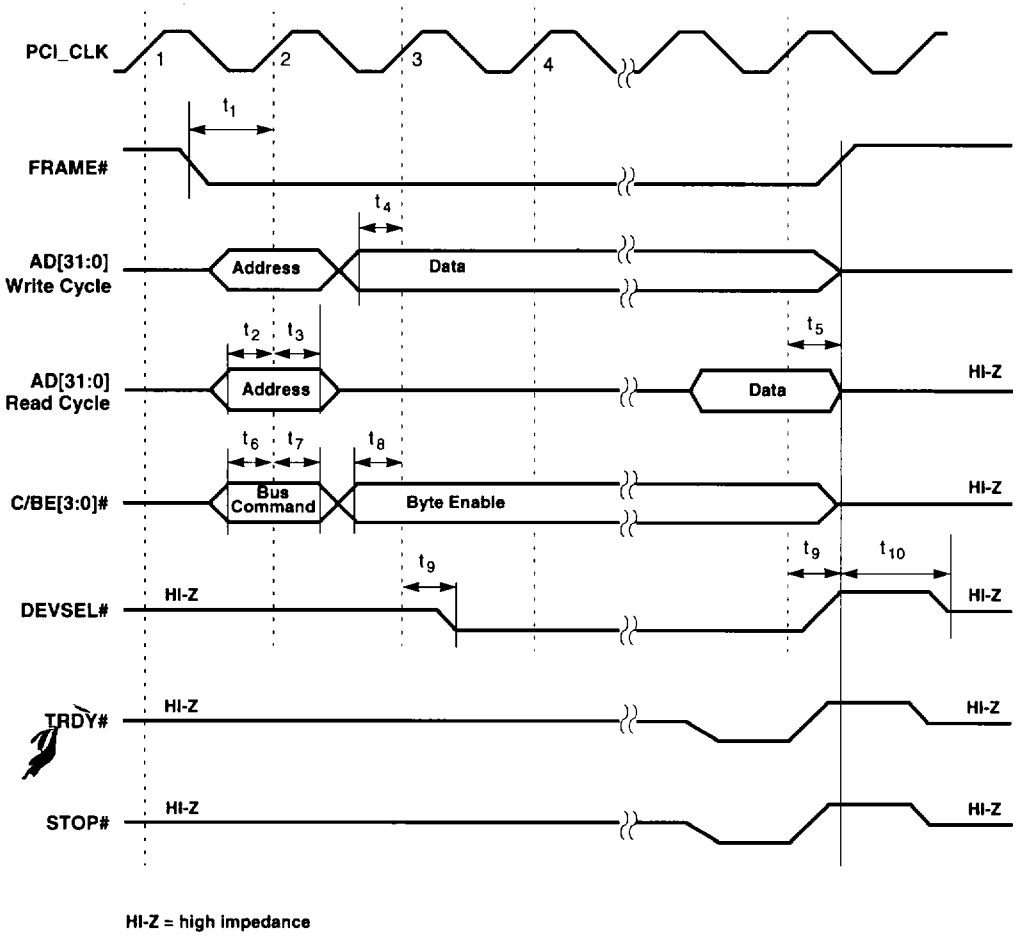


Figure 13–1. FRAME#, AD[31:0], C/BE[3:0]#, and DEVSEL# (PCI™ Bus)

Table 13–9. TRDY# and STOP# Delay

Symbol	Parameter	PCI_VCC = 3.3 V		PCI_VCC = 5.0 V		Units
		MIN	MAX	MIN	MAX	
t_1	TRDY# active delay from PCI_CLK	–	11	–	11	ns
t_2	TRDY# inactive delay from PCI_CLK	–	11	–	11	ns
t_3	TRDY# high before HI-Z	1	–	1	–	PCI_CLK
t_4	STOP# active delay from PCI_CLK	–	11	–	11	ns
t_5	STOP# inactive delay from PCI_CLK	–	11	–	11	ns
t_6	STOP# high before HI-Z	1	–	1	–	PCI_CLK

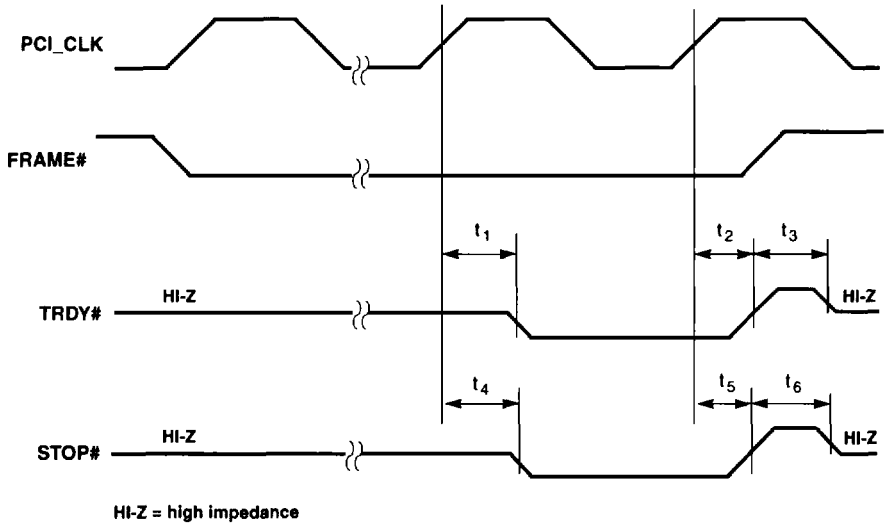


Figure 13–2. TRDY# and STOP# Delay (PCI™ Bus)

Table 13–10. IDSEL Timing in a Configuration Cycle

Symbol	Parameter	MIN	MAX	Units
t_1	IDSEL setup to PCI_CLK	7	–	ns
t_2	IDSEL hold from PCI_CLK	0	–	ns

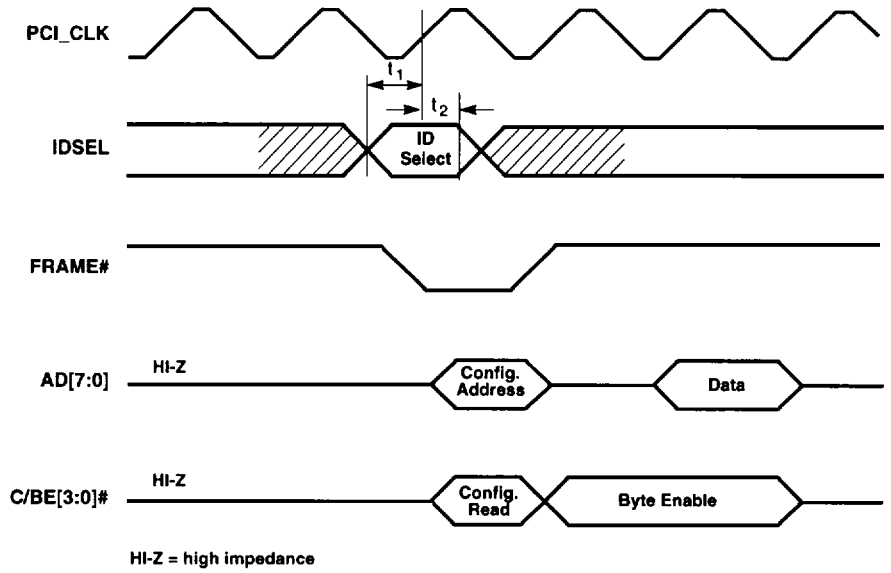
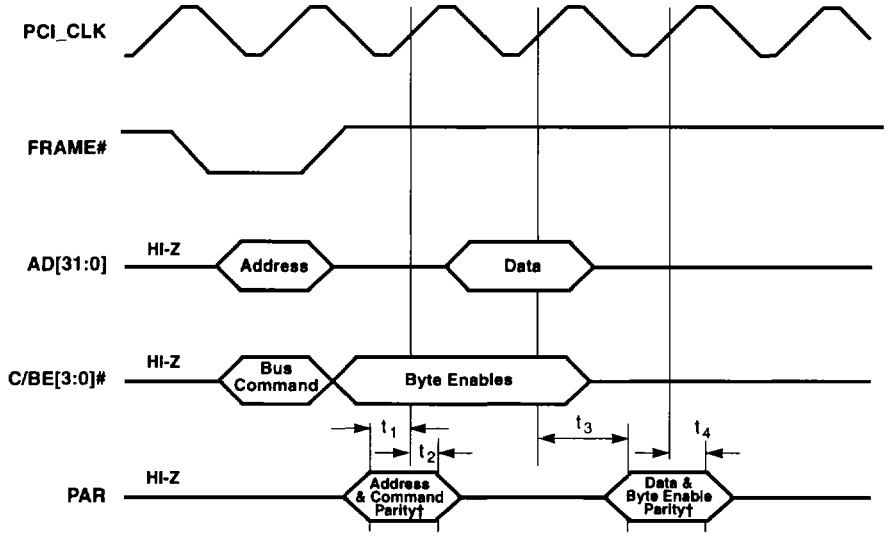


Figure 13–3. IDSEL Timing in a Configuration Cycle (PCI™ Bus)

Table 13–11. PAR Timing

Symbol	Parameter	MIN	MAX	Units
t_1	PAR setup to PCI_CLK (input to CL-PD6729)	7	–	ns
t_2	PAR hold from PCI_CLK (input to CL-PD6729)	0	–	ns
t_3	PAR valid delay from PCI_CLK (output from CL-PD6729)	–	11	ns
t_4	PAR hold from PCI_CLK (output from CL-PD6729)	0	–	ns



HI-Z = high impedance

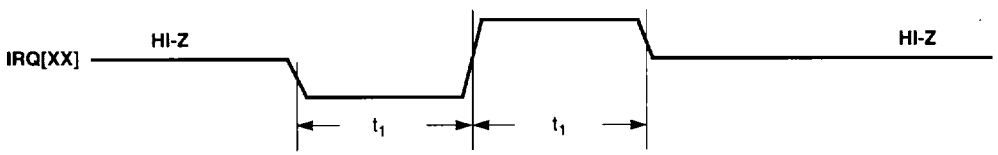
† PAR goes high or low depending on AD[31:0] and C/BE[3:0]# values.

Figure 13–4. PAR Timing (PCI™ Bus)

13.3.2 System Interrupt Timing

Table 13–12. Pulse Mode Interrupt Timing

Symbol	Parameter	MIN	MAX	Units
t_1	IRQ[XX] low or high	4	4	PCI_CLK



HI-Z = high impedance
NOTE: Each time indicated is 4 PCI clocks or 4 external clocks, independent of setting of the Timer Clock Divide bit.

Figure 13–5. Pulse Mode Interrupt Timing

13.3.3 PCMCIA Bus Timing Calculations

Calculations for minimum PCMCIA cycle Setup, Command, and Recovery timings are made by first calculating factors derived from the applicable timer set's timing registers and then by applying the factor to an equation relating it to the internal clock period.

The PCMCIA cycle timing factors, in terms of the number of internal clocks[1], are calculated as follows:

$$S = (N_{pres} \times N_{val}) + 1$$

$$C = (N_{pres} \times N_{val}) + 1$$

$$R = (N_{pres} \times N_{val}) + 1$$

N_{pres} and N_{val} are the specific selected prescalar and multiplier value from the timer set's Setup, Command, and Recovery Timing registers (see Chapter 11 for description of these registers).

From this, a PCMCIA cycle's Setup, Command, and Recovery time for the selected timer set are calculated as follows:

$$\text{Minimum Setup time} = (S \times Tcp) - 10 \text{ ns}$$

$$\text{Minimum Command time} = (C \times Tcp) - 10 \text{ ns}$$

$$\text{Minimum Recovery time} = (R \times Tcp) - 10 \text{ ns}$$

Tcp is the period of the internal clock.

If PCI_CLK is selected (**Misc Control 2** register bit 0 is a '0') and operates at 25 MHz, and the clock input is not being divided (**Misc Control 2** register bit 4 is a '0'), then:

$$Tcp = 40 \text{ ns}$$

The timing diagrams that follow were derived for a CL-PD6729 using the PCI clock at 25 MHz. The examples are for the default values of the Timing registers for Timer Set 0, as follows:

Timing Register Name (Timer Set 0)	Index	Value (Default)	Resultant N_{pres}	Resultant N_{val}
Setup Timing 0	3Ah	01h	1	1
Command Timing 0	3Bh	05h	1	8
Recovery Timing 0	3Ch	00h	1	0

Thus the minimum times for the default values are as follows:

$$\text{Minimum Setup time} = (S \times Tcp) - 10 \text{ ns} = \{[(1 \times 1) + 1] \times 40 \text{ ns}\} - 10 \text{ ns} = \mathbf{70\ ns}$$

$$\text{Minimum Command time} = (C \times Tcp) - 10 \text{ ns} = \{[(1 \times 5) + 1] \times 40 \text{ ns}\} - 10 \text{ ns} = \mathbf{230\ ns}$$

$$\text{Minimum Recovery time} = (R \times Tcp) - 10 \text{ ns} = \{[(1 \times 0) + 1] \times 40 \text{ ns}\} - 10 \text{ ns} = \mathbf{30\ ns}$$

[1] The internal clock period is the same as PCI_CLK or EXT_CLK period if **Misc Control 2** register bit 4 is a '0', and it is double the PCI_CLK or EXT_CLK period if **Misc Control 2** register bit 4 is a '1'.

13.3.4 PCMCIA Bus Timing

Table 13–13. Memory Read/Write Timing

Symbol	Parameter	MIN	MAX	Units
t_1	-REG, -CE[2:1], Address, and Write Data setup to Command active[1]	(S × Tcp) – 10		ns
t_2	Command pulse width[2]	(C × Tcp) – 10		ns
t_3	Address hold and Write Data valid from Command inactive[3]	(R × Tcp) – 10		ns
t_4	-WAIT active from Command active		(C – 2)Tcp – 10	ns
t_5	Command hold from -WAIT inactive	2 Tcp		ns
t_6	Data setup before -OE inactive	(2 Tcp) + 10		ns
t_7	Data hold after -OE inactive	0		ns
t_8	Data valid from -WAIT inactive	Tcp + 10		ns

[1] The Setup time is determined by the value programmed into the **Setup Timing** register, index 3Ah/3Dh. Using the Timer Set 0 default value of 01h, the setup time would be 70 ns. S = (N_{pres} × N_{val} + 1), see page 84.

[2] The Command time is determined by the value programmed into the **Command Timing** register, index 3Bh/3Eh. Using the Timer Set 0 default value of 05h, the Command time would be 230 ns. C = (N_{pres} × N_{val} + 1), see page 84.

[3] The Recovery time is determined by the value programmed into the **Recovery Timing** register, index 3Ch/3Fh. Using the Timer Set 0 default value of 00h, the hold (Recovery) time would be 30 ns. R = (N_{pres} × N_{val} + 1), see page 84.

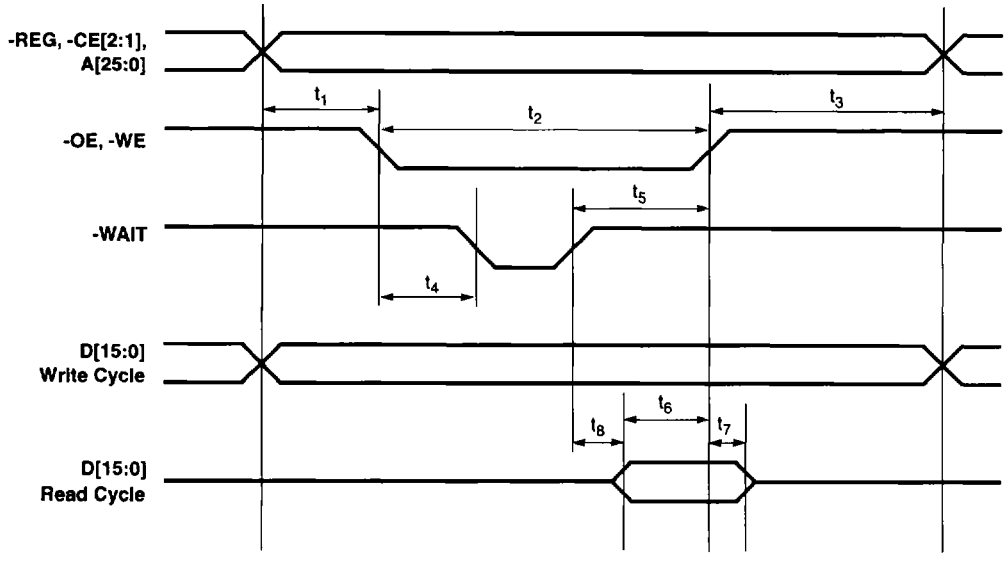


Figure 13–6. Memory Read/Write Timing

Table 13–14. Word I/O Read/Write Timing

Symbol	Parameter	MIN	MAX	Units
t_1	-REG or Address setup to Command active[1]	(S × Tcp) – 10		ns
t_2	Command pulse width[2]	(C × Tcp) – 10		ns
t_3	Address hold and Write Data valid from Command inactive[3]	(R × Tcp) – 10		ns
t_{ref}	Card -IOIS16 delay from valid Address (PCMCIA card specification)		35	ns
t_4	-IOIS16 setup time before Command end	(3 Tcp) + 10		ns
t_5	-CE2 delay from -IOIS16 active[4]	Tcp – 10		ns
t_6	Data setup before -IORD inactive	(2 Tcp) + 10		ns
t_7	Data hold after -IORD inactive	0		ns

[1] The Setup time is determined by the value programmed into the **Setup Timing** register, index 3Ah/3Dh. Using the Timer Set 0 default value of 01h, the setup time would be 70 ns. S = (N_{pres} × N_{val} + 1), see page 84.

[2] The Command time is determined by the value programmed into the **Command Timing** register, index 3Bh/3Eh. Using the Timer Set 0 default value of 05h, the Command time would be 230 ns. C = (N_{pres} × N_{val} + 1), see page 84.

[3] The Recovery time is determined by the value programmed into the **Recovery Timing** register, index 3Ch/3Fh. Using the Timer Set 0 default value of 00h, the hold (Recovery) time would be 30 ns. R = (N_{pres} × N_{val} + 1), see page 84.

[4] -IOIS16 must go low within 3Tcp + 10 ns of the cycle beginning or -IOIS16 will be ignored and -CE will not be activated.

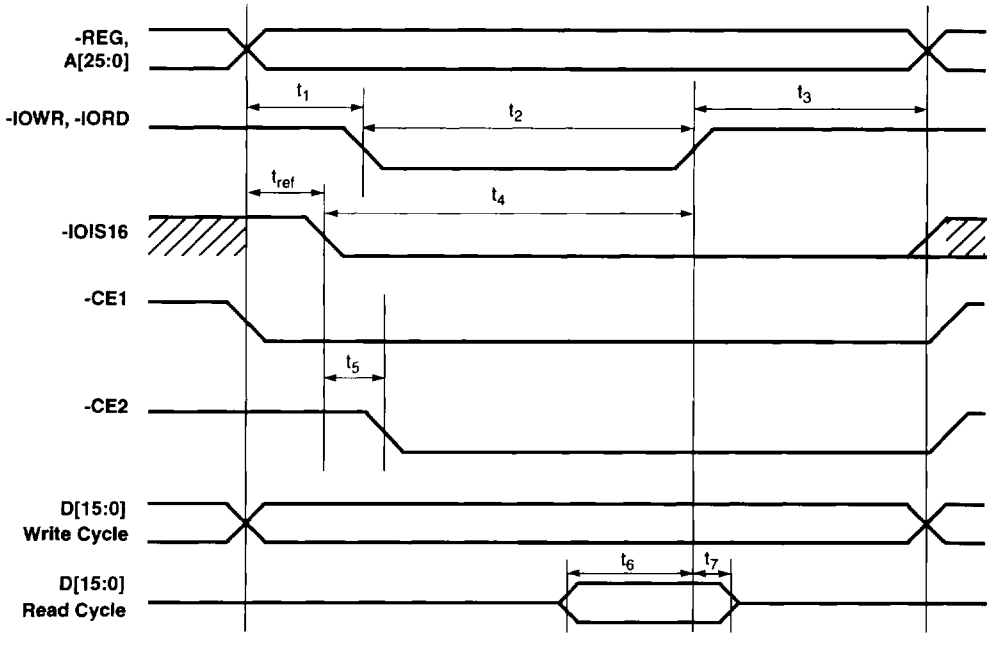


Figure 13–7. Word I/O Read/Write Timing

Table 13–15. PCMCIA Read/Write Timing when System is 8-Bit

Symbol	Parameter	MIN	MAX	Units
t_1	-REG or Address setup to Command active[1]	(S × Tcp) – 10		ns
t_2	Command pulse width[2]	(C × Tcp) – 10		ns
t_3	Address hold from Command inactive[3]	(R × Tcp) – 10		ns
t_4	Data setup before Command inactive	(2 Tcp) + 10		ns
t_5	Data hold after command inactive	0		ns

[1] The Setup time is determined by the value programmed into the **Setup Timing** register, index 3Ah/3Dh. Using the Timer Set 0 default value of 01h, the setup time would be 70 ns. S = (N_{pres} × N_{val} + 1), see page 84.

[2] The Command time is determined by the value programmed into the **Command Timing** register, index 3Bh/3Eh. Using the Timer Set 0 default value of 05h, the Command time would be 230 ns. C = (N_{pres} × N_{val} + 1), see page 84.

[3] The Recovery time is determined by the value programmed into the **Recovery Timing** register, index 3Ch/3Fh. Using the Timer Set 0 default value of 00h, the hold (Recovery) time would be 30 ns. R = (N_{pres} × N_{val} + 1), see page 84.

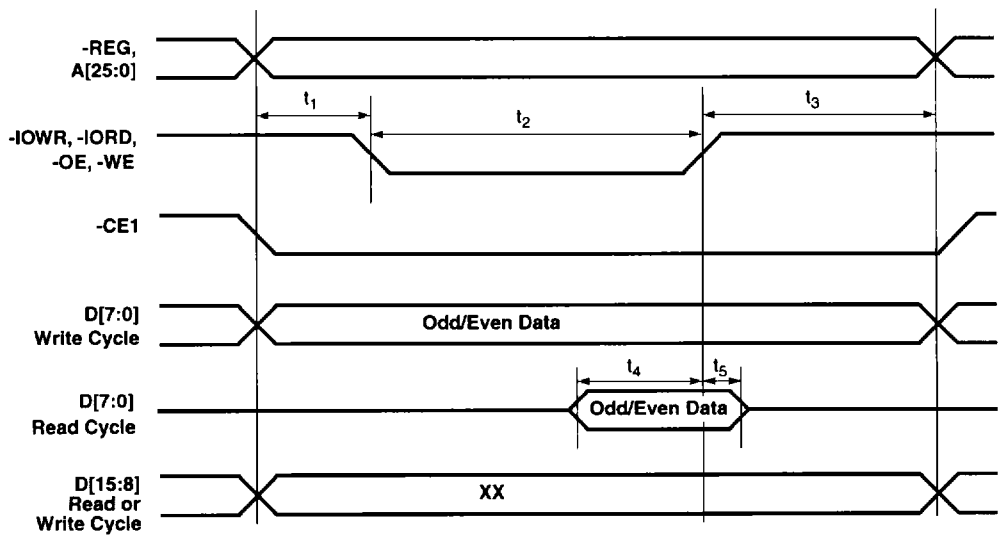


Figure 13–8. PCMCIA Read/Write Timing when System is 8 Bit ($\overline{SBHE}$ Tied High)

Table 13–16. Normal Byte Read/Write Timing

Symbol	Parameter	MIN	MAX	Units
t_1	Address setup to Command active[1]	(S × Tcp) – 10		ns
t_2	Command pulse width[2]	(C × Tcp) – 10		ns
t_3	Address hold from Command inactive[3]	(R × Tcp) – 10		ns

[1] The Setup time is determined by the value programmed into the **Setup Timing** register, index 3Ah/3Dh. Using the Timer Set 0 default value of 01h, the setup time would be 70 ns. S = (N_{pres} × N_{val} + 1), see page 84.

[2] The Command time is determined by the value programmed into the **Command Timing** register, index 3Bh/3Eh. Using the Timer Set 0 default value of 05h, the Command time would be 230 ns. C = (N_{pres} × N_{val} + 1), see page 84.

[3] The Recovery time is determined by the value programmed into the **Recovery Timing** register, index 3Ch/3Fh. Using the Timer Set 0 default value of 00h, the hold (Recovery) time would be 30 ns. R = (N_{pres} × N_{val} + 1), see page 84.

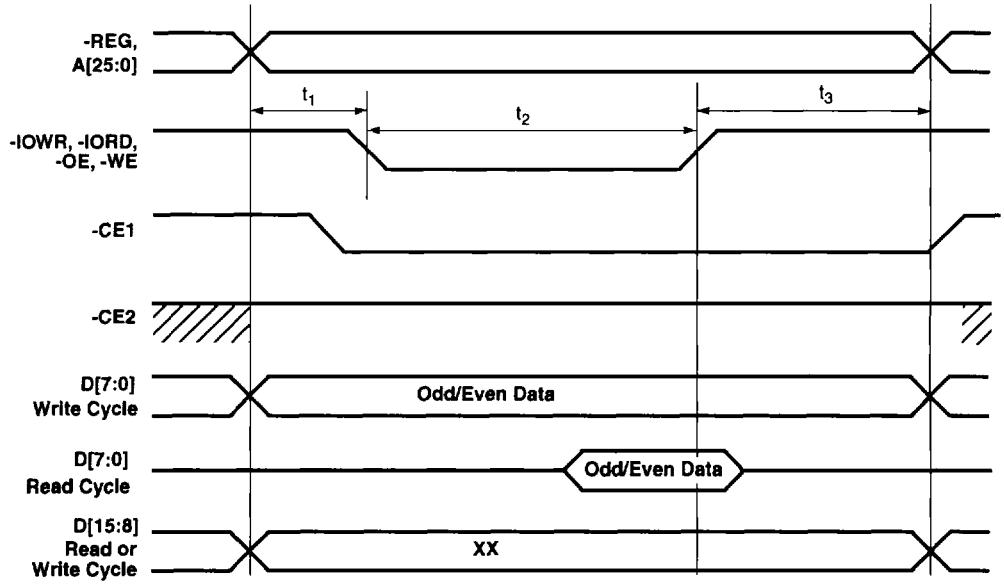


Figure 13–9. Normal Byte Read/Write Timing (that is, all other byte accesses, including odd I/O cycles where -IOIS16 is low)

Table 13–17. 16-Bit System to 8-Bit I/O Card: Odd Byte Timing

Symbol	Parameter	MIN	MAX	Units
t_1	Address change to -IOIS16 inactive[4]		(3Tcp) + 10	ns
t_2	-IOIS16 inactive to -CE2 inactive		20	ns
t_3	-IOIS16 inactive to -CE1 active		20	ns
t_4	Address setup to Command active[1]	(S × Tcp) – 10		ns
t_5	Command pulse width[2]	(C × Tcp) – 10		ns
t_6	Address hold from Command inactive[3]	(R × Tcp) – 10		ns

[1] The Setup time is determined by the value programmed into the **Setup Timing** register, index 3Ah/3Dh. Using the Timer Set 0 default value of 01h, the setup time would be 70 ns. S = (N_{pres} × N_{val} + 1), see page 84.

[2] The Command time is determined by the value programmed into the **Command Timing** register, index 3Bh/3Eh. Using the Timer Set 0 default value of 05h, the Command time would be 230 ns. C = (N_{pres} × N_{val} + 1), see page 84.

[3] The Recovery time is determined by the value programmed into the **Recovery Timing** register, index 3Ch/3Fh. Using the Timer Set 0 default value of 00h, the hold (Recovery) time would be 30 ns. R = (N_{pres} × N_{val} + 1), see page 84.

[4] -IOIS16 level from card must be valid within 3 clocks of an address change to the card.

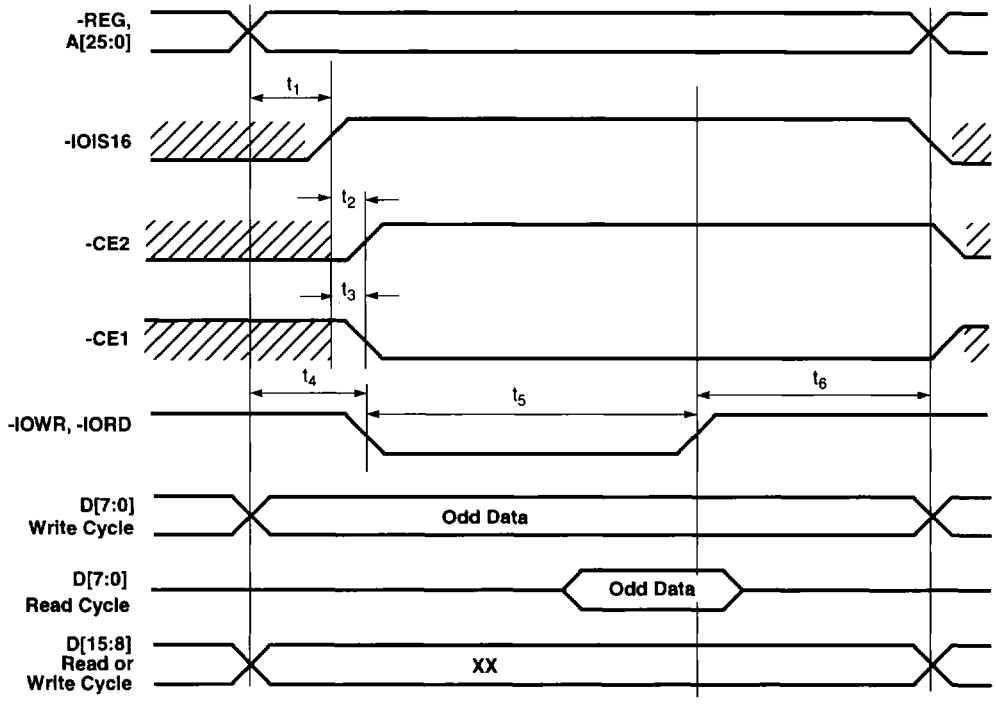


Figure 13–10. 16-Bit System to 8-Bit I/O Card: Odd Byte Timing