

# RJK0629JPE

60 V - 85 A - Silicon N Channel MOS FET  
High Speed Power Switching

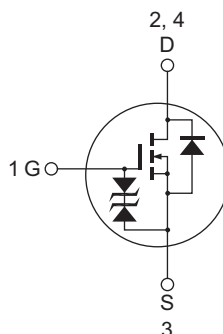
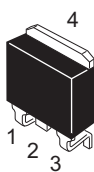
R07DS1075EJ0100  
Rev.1.00  
Jun 17, 2013

## Features

- For Automotive application
- AEC-Q101 compliant
- Low on-resistance :  $R_{DS(on)} = 3.75 \text{ m}\Omega$  typ.
- Capable of 4.5 V gate drive
- Low input capacitance :  $C_{iss} = 4100 \text{ pF}$  typ

## Outline

RENESAS Package code: PRSS0004AE-B  
(Package name: LDPAK(S)-(1) )



1. Gate
2. Drain
3. Source
4. Drain

## Absolute Maximum Ratings

( $T_a = 25^\circ\text{C}$ )

Item	Symbol	Value	Unit
Drain to source voltage	$V_{DSS}$	60	V
Gate to source voltage	$V_{GSS}$	$\pm 20$	V
Drain current	$I_D$	85	A
Drain peak current	$I_D$ (pulse) <sup>Note1</sup>	340	A
Body-drain diode reverse drain current	$I_{DR}$	85	A
Body-drain diode reverse drain peak current	$I_{DR}$ (pulse) <sup>Note1</sup>	340	A
Avalanche current	$I_{AP}$ <sup>Note2</sup>	55	A
Avalanche energy	$E_{AR}$ <sup>Note2</sup>	259	mJ
Channel dissipation	$P_{ch}$ <sup>Note3</sup>	120	W
Channel temperature	$T_{ch}$ <sup>Note4</sup>	175	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

Notes: 1.  $PW \leq 10 \mu\text{s}$ , duty cycle  $\leq 1\%$

2.  $T_{ch} = 25^\circ\text{C}$ ,  $R_g \geq 50 \Omega$

3.  $T_c = 25^\circ\text{C}$

4. AEC-Q101 compliant

## Thermal Impedance Characteristics

- Channel to case thermal impedance  $\theta_{ch-c}$ :  $1.25^\circ\text{C/W}$

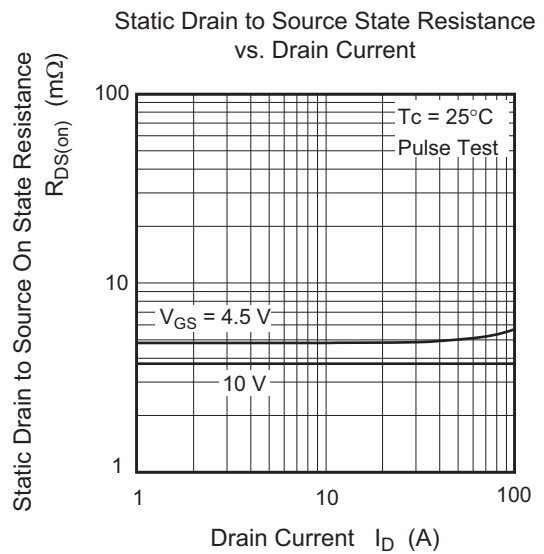
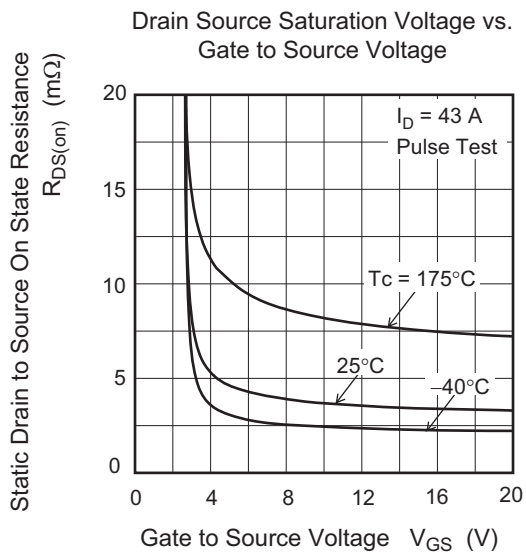
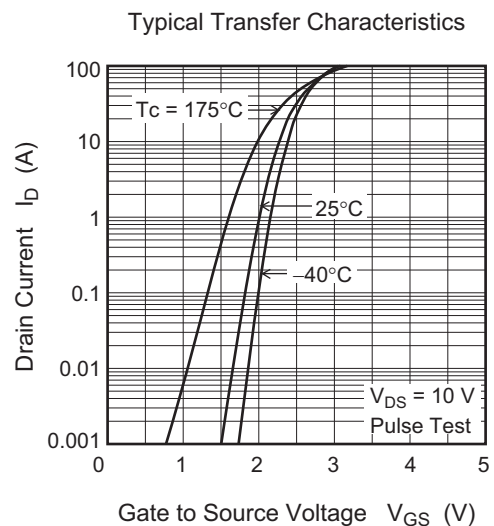
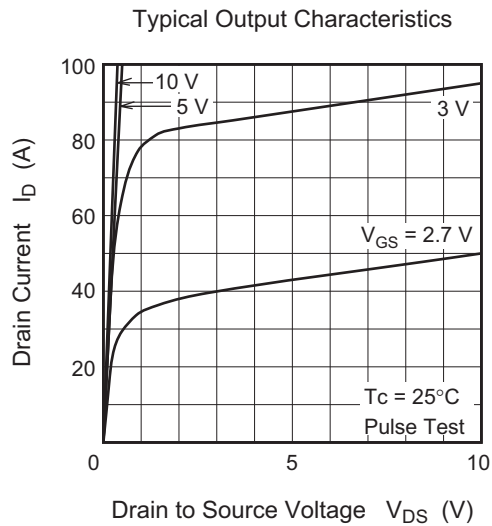
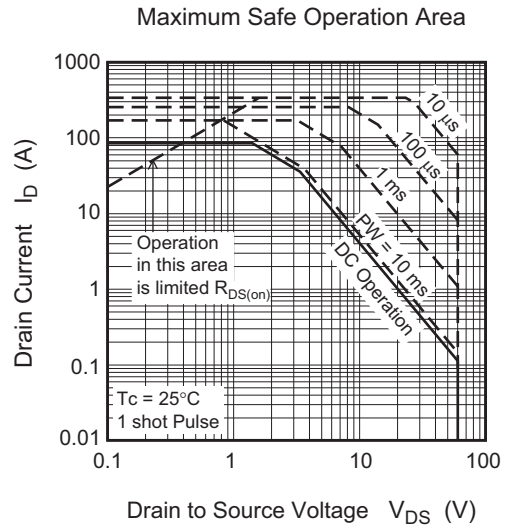
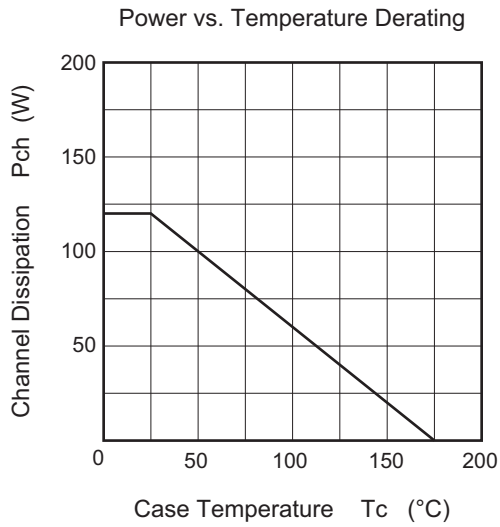
## Electrical Characteristics

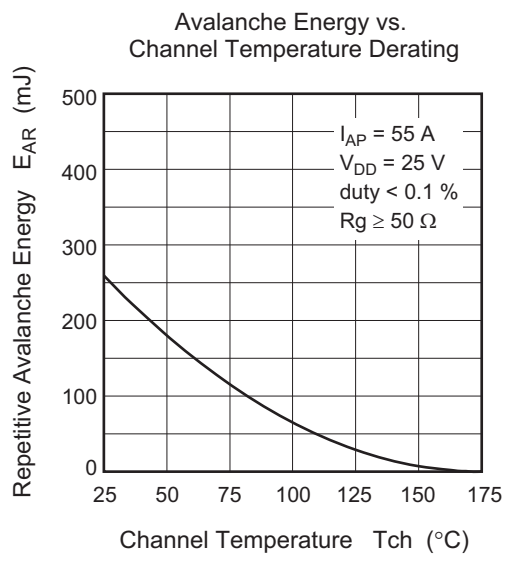
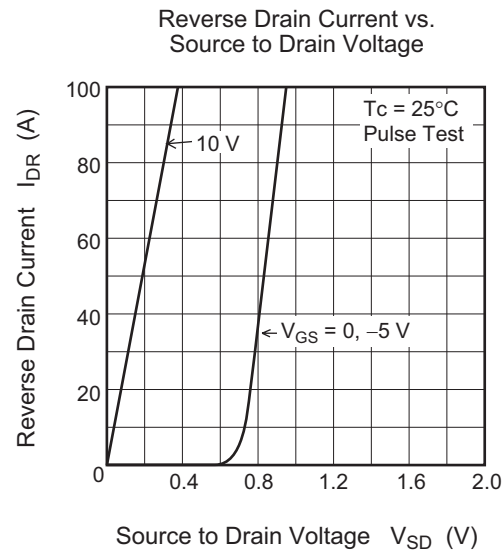
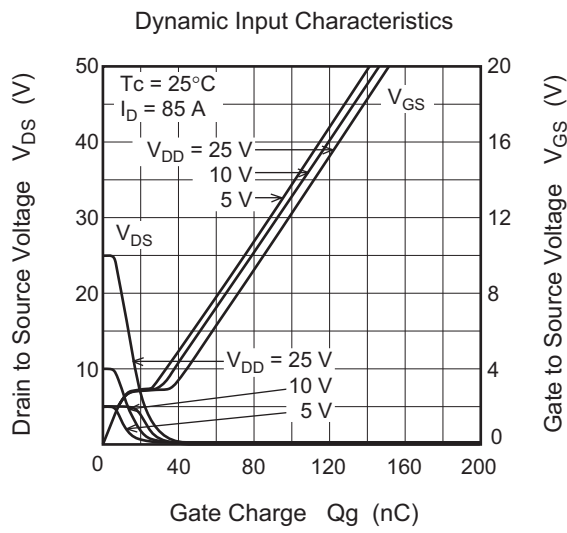
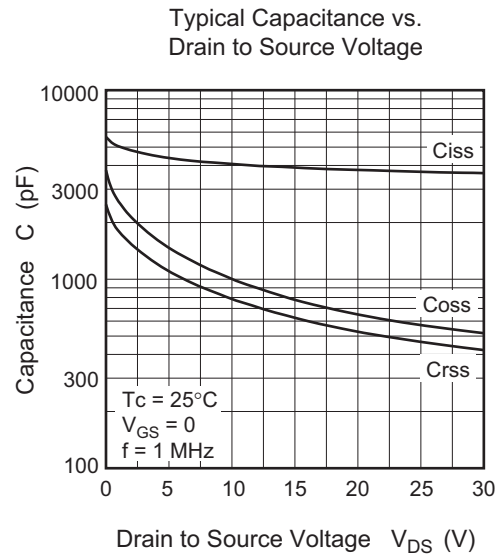
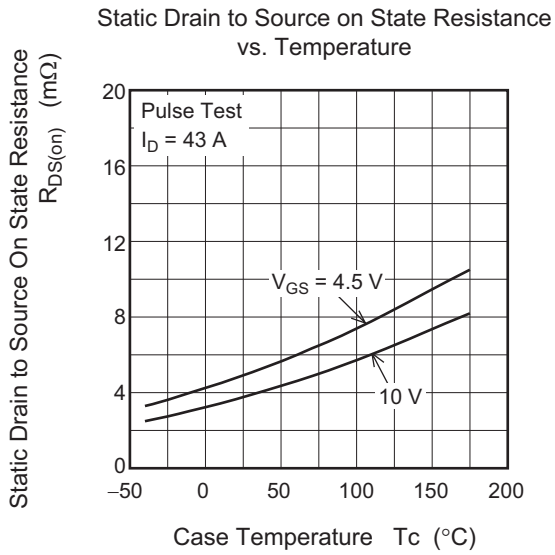
(Ta = 25°C)

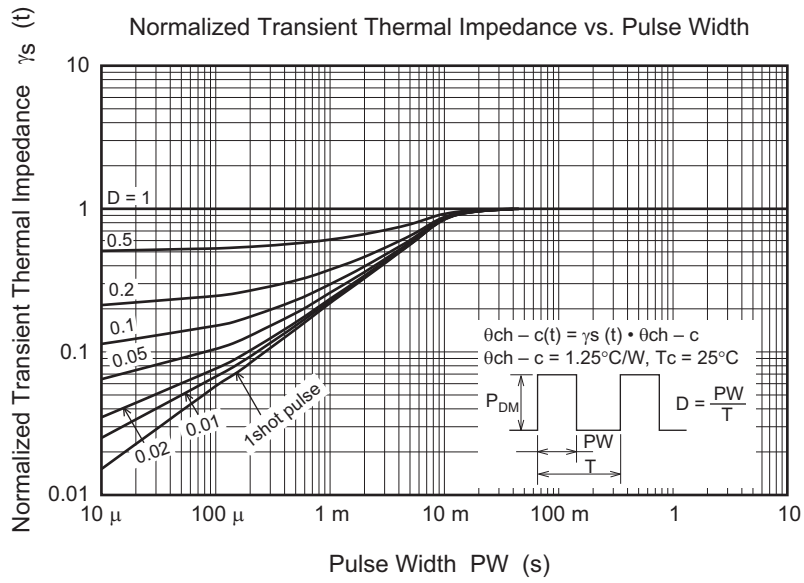
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Gate to source leak current	I <sub>GSS</sub>	—	—	±10	μA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0
Zero gate voltage drain current	I <sub>DSS</sub>	—	—	1	μA	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0
Gate to source cutoff voltage	V <sub>GS(off)</sub>	1.0	—	2.0	V	I <sub>D</sub> = 1 mA, V <sub>DS</sub> = 10 V
Static drain to source on state resistance	R <sub>DS(on)</sub>	—	3.75	4.5	mΩ	I <sub>D</sub> = 43 A, V <sub>GS</sub> = 10 V <sup>Note5</sup>
		—	4.9	6.6	mΩ	I <sub>D</sub> = 43 A, V <sub>GS</sub> = 4.5 V <sup>Note5</sup>
Input capacitance	C <sub>iss</sub>	—	4100	—	pF	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 f = 1 MHz
Output capacitance	C <sub>oss</sub>	—	1000	—	pF	
Reverse transfer capacitance	C <sub>rss</sub>	—	780	—	pF	
Total gate charge	Q <sub>g</sub>	—	85	—	nC	V <sub>DD</sub> = 25 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 85 A
Gate to source charge	Q <sub>gs</sub>	—	11	—	nC	
Gate to drain charge	Q <sub>gd</sub>	—	25	—	nC	
Turn-on delay time	t <sub>d(on)</sub>	—	20	—	ns	I <sub>D</sub> = 43A, R <sub>L</sub> = 0.698 Ω, V <sub>GS</sub> = 10 V, R <sub>G</sub> = 4.7 Ω
Rise time	t <sub>r</sub>	—	40	—	ns	
Turn-off delay time	t <sub>d(off)</sub>	—	100	—	ns	
Fall time	t <sub>f</sub>	—	40	—	ns	
Body-drain diode forward voltage	V <sub>DF</sub>	—	0.92	1.2	V	I <sub>F</sub> = 85 A, V <sub>GS</sub> = 0 <sup>Note5</sup>
Body-drain diode reverse recovery time	t <sub>rr</sub>	—	50	—	ns	I <sub>F</sub> = 85 A, V <sub>GS</sub> = 0, di <sub>F</sub> /dt = 100 A/μs

Note: 5. Pulse test

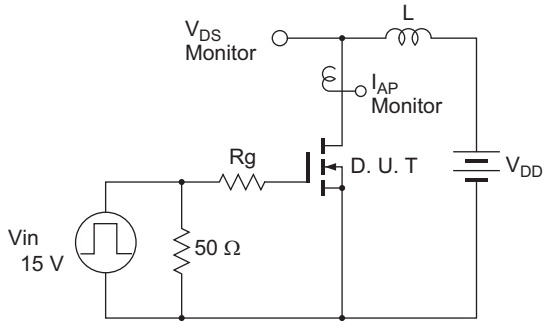
Main Characteristics





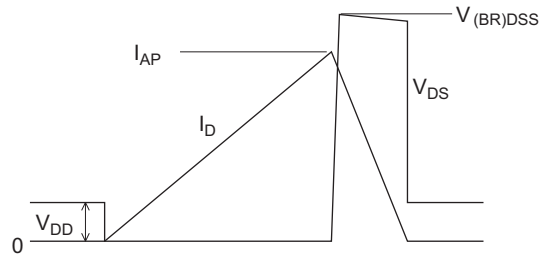


Avalanche Test Circuit

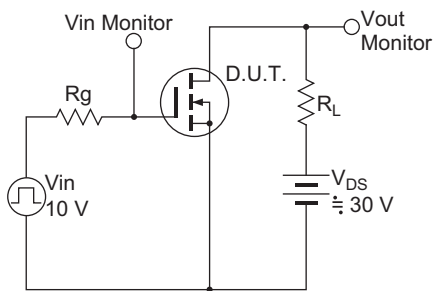


Avalanche Waveform

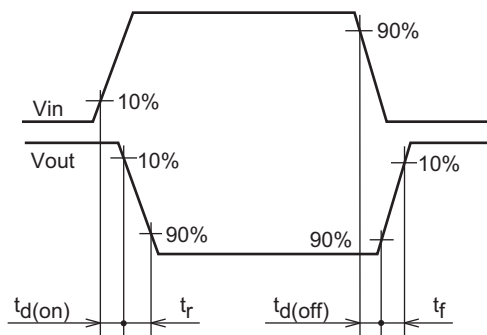
$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



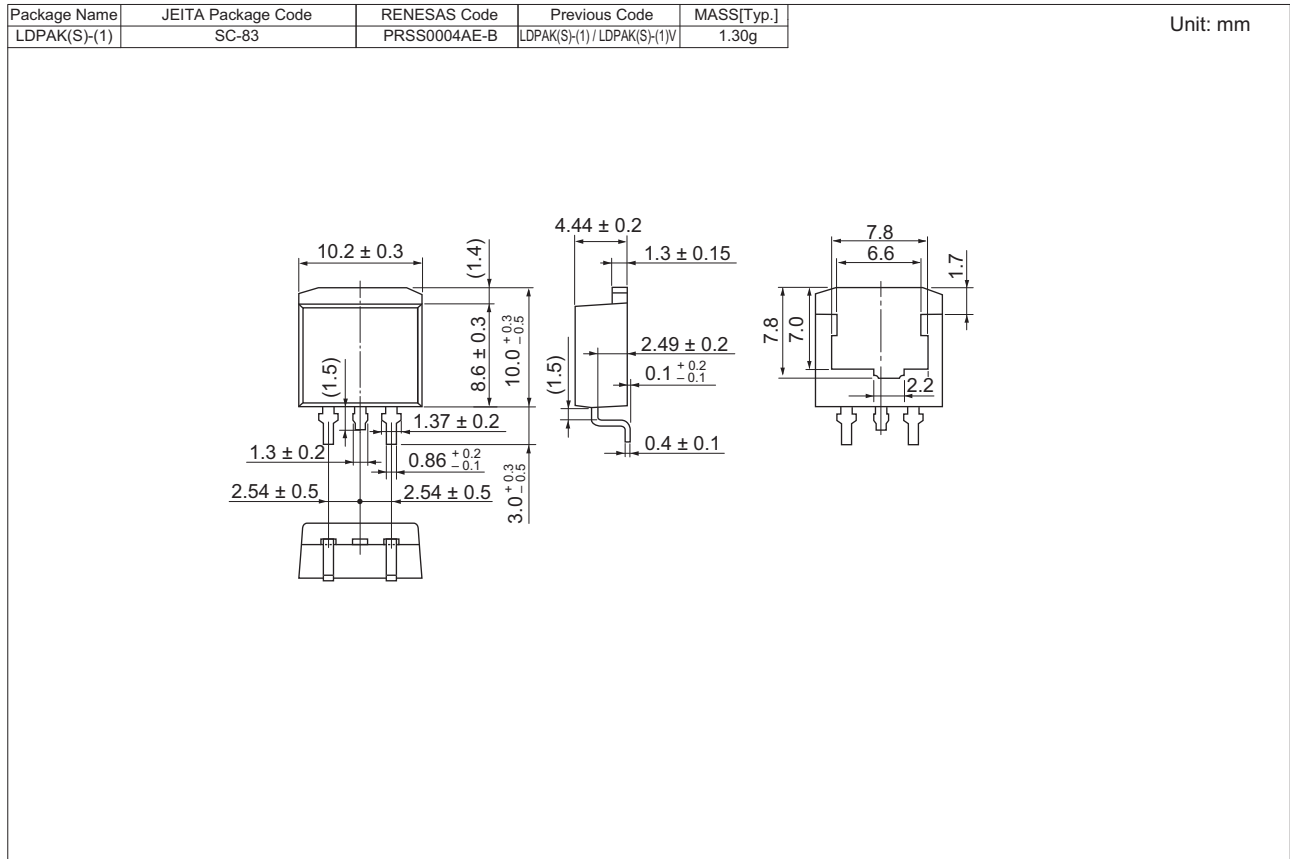
Switching Time Test Circuit



Switching Time Waveform



### Package Dimensions



### Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJK0629JPE-00-J3	1000 pcs	Taping (Sinistrorse)

Note: The symbol of 2nd "-" is occasionally presented as "#".

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