



GENERAL DESCRIPTION



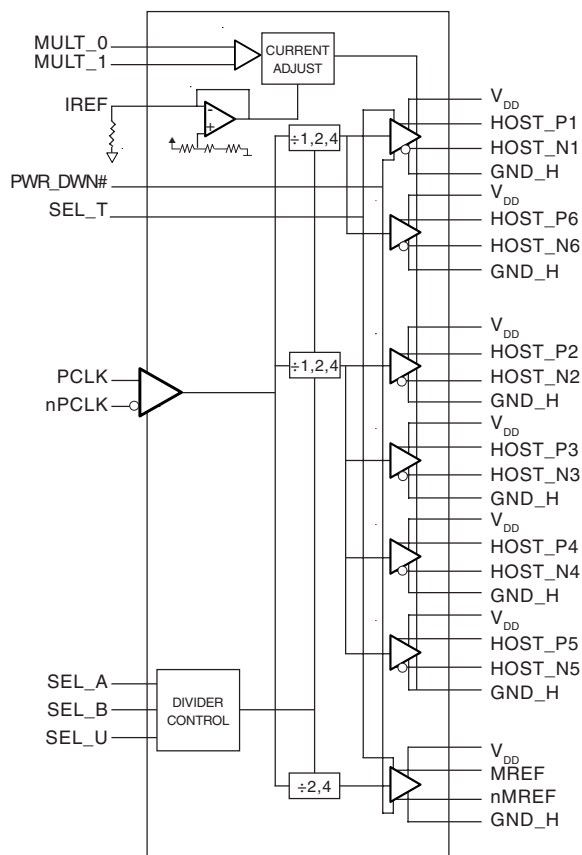
The ICS87158 is a high performance 1-to-6 LVPECL-to-HCSL/LVCMOS Clock Generator and is a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS87158 has one differential input (which can accept LVDS, LVPECL, LVHSTL, SSTL, HCSL), six differential HCSL output pairs and two complementary LVCMOS/LVTTL outputs. The six HCSL output pairs can be individually configured for divide-by-1, 2, and 4 or high impedance by use of select pins. The two complementary LVCMOS/LVTTL outputs can be configured for divide by 2, divide by 4, high impedance, or driven low for low power operation.

The primary use of the ICS87158 is in Intel® E8870 chipsets that use Intel® Pentium 4 processors. The ICS87158 converts the differential clock from the main system clock into HCSL clocks used by Intel® Pentium 4 processors. However, the ICS87158 is a highly flexible, general purpose device that operates up to 600MHz and can be used in any situation where Differential-to-HCSL translation is required.

FEATURES

- Six HCSL outputs
- Two LVCMOS/LVTTL outputs
- One Differential LVPECL clock input pair
- PCLK, nPCLK supports the following input types: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 600MHz (maximum)
- Output skew: 100ps (maximum)
- Propagation delay: 4ns (maximum)
- 3.3V operating supply
- 0°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS compliant packages
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT

GND	1	48	V _{DD}
V _{DD}	2	47	GND _H
V _{DD_R}	3	46	V _{DD_H}
PCLK	4	45	HOST_P1
nPCLK	5	44	HOST_N1
GND _R	6	43	GND _H
V _{DD_M}	7	42	HOST_P2
MREF	8	41	HOST_N2
nMREF	9	40	V _{DD_H}
GND _M	10	39	HOST_P3
V _{DD}	11	38	HOST_N3
GND	12	37	GND _H
V _{DD_L}	13	36	HOST_P4
V _{DD}	14	35	HOST_N4
GND _L	15	34	V _{DD_H}
SEL_T	16	33	HOST_P5
MULT_0	17	32	HOST_N5
MULT_1	18	31	GND _H
V _{DD_L}	19	30	HOST_P6
GND _L	20	29	HOST_N6
SEL_A	21	28	V _{DD_H}
SEL_B	22	27	IREF
SEL_U	23	26	GND _I
PWR_DWN#	24	25	V _{DD_I}

48-Lead TSSOP

6.1mm x 12.5mm x .92mm body package

G Package

Top View

48-Lead SSOP

7.5mm x 15.9mm x 2.3mm body package

F Package

Top View



TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 12	GND	Power		Power supply ground.
2, 11, 14, 48	V _{DD}	Power		Positive supply pins.
3	V _{DD-R}	Power		Power supply pin for differential reference clock inputs.
4	PCLK	Input		Non-inverting differential LVPECL clock input.
5	nPCLK	Input		Inverting differential LVPECL clock input.
6	GND_R	Power		Power supply ground for differential inputs.
7	V _{DD-M}	Power		Power supply pin for MREF clock outputs.
8, 9	MREF, nMREF	Output		Single ended clocks provided as a reference clock to a memory clock driver. LVCMOS / LVTTTL interface levels.
10	GND_M	Power		Power supply ground for MREF clock outputs.
13	V _{DD-L}	Power		Power supply pin for logic input pins.
15, 20	GND_L	Power		Power supply ground for logic input pins.
16	SEL_T	Input	Pulldown	Active high input tristates all outputs. LVCMOS / LVTTTL interface levels.
17	MULT_0	Input	Pulldown	The logic setting on these two pins selects the multiplying factor of the IREF reference current for the HOST pair outputs. LVCMOS / LVTTTL interface levels.
18	MULT_1	Input	Pullup	The logic setting on these two pins selects the multiplying factor of the IREF reference current for the HOST pair outputs. LVCMOS / LVTTTL interface levels.
19	V _{DD-L}	Power		Power supply pin for logic input pins.
21, 22, 23	SEL_A, SEL_B, SEL_U	Input	Pulldown	Selects desired output frequencies. LVCMOS / LVTTTL interface levels.
24	PWR_DWN#	Input	Pullup	Asynchronous active-low LVTTTL power-down signal forces MREF outputs low, tristates HOST_N outputs, and drives HOST_P output currents to 2xIREF. LVCMOS / LVTTTL interface levels.
25	V _{DD-I}	Power		Power supply pin for IREF current reference input.
26	GND_I	Power		Power supply ground for IREF current reference input.
27	IREF	Input		A fixed precision resistor from this pin to ground provides a reference current used for differential current-mode HOST clock outputs.
28, 34, 40, 46	V _{DD-H}	Power		Power supply pins for the differential HOST clock outputs.
29, 30	HOST_N6, HOST_P6	Output		Differential output pairs. HCSL interface levels.
31, 37, 43, 47	GND_H	Power		Power supply ground for the differential HOST clock outputs.
32, 33	HOST_N5, HOST_P5	Output		Differential output pairs. HCSL interface levels.
35, 36	HOST_N4, HOST_P4	Output		Differential output pairs. HCSL interface levels.
38, 39	HOST_N3, HOST_P3	Output		Differential output pairs. HCSL interface levels.
41, 42	HOST_N2, HOST_P2	Output		Differential output pairs. HCSL interface levels.
44, 45	HOST_N1, HOST_P1	Output		Differential output pairs. HCSL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.



TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		k Ω
$R_{PULLDOWN}$	Input Pulldown Resistor			51		k Ω

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs					Outputs						
PWR_DWN#	SEL_T	SEL_A	SEL_B	SEL_U	HST_P1 HST_N1	HST_P2 HST_N2	HST_P3 HST_N3	HST_P4 HST_N4	HST_P5 HST_N5	HST_P6 HST_N6	MREF_P MREF_N
1	0	0	0	0	÷ 2	÷ 2	÷ 2	÷ 2	÷ 2	÷ 2	÷ 4
1	0	0	0	1	Hi Z	÷ 2	÷ 2	÷ 2	÷ 2	Hi Z	÷ 4
1	0	0	1	0	÷ 4	÷ 2	÷ 2	÷ 2	÷ 2	÷ 4	÷ 4
1	0	0	1	1	÷ 4	÷ 4	÷ 4	÷ 4	÷ 4	÷ 4	÷ 4
1	0	1	0	0	÷ 1	÷ 1	÷ 1	÷ 1	÷ 1	÷ 1	÷ 4
1	0	1	0	1	Hi Z	÷ 1	÷ 1	÷ 1	÷ 1	Hi Z	÷ 4
1	0	1	1	0	÷ 2	÷ 1	÷ 1	÷ 1	÷ 1	÷ 2	÷ 4
1	0	1	1	1	÷ 2	÷ 2	÷ 2	÷ 2	÷ 2	÷ 2	÷ 2
1	1	X	X	X	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z
0	X	X	X	X	HST_P1 =2 x IREF	HST_P2 =2 x IREF	HST_P3 =2 x IREF	HST_P4 =2 x IREF	HST_P5 =2 x IREF	HST_P6 =2 x IREF	MREF_P = low
					HST_N1 = Hi Z	HST_N2 = Hi Z	HST_N3 = Hi Z	HST_N4 = Hi Z	HST_N5 = Hi Z	HST_N6 = Hi Z	MREF_N = low

TABLE 3B. FUNCTION TABLE

Inputs		Device Configurations			
MULT_0	MULT_1	Board Target Trace/Term Z	Reference R, $I_{REF} = V_{DD}/(3 \cdot R_r)$	Output Current	V_{OH} @ 50 Ω Environment
0	0	50 Ω	$R_r = 475 \text{ } \Omega$, $I_{REF} = 2.32 \text{ mA}$	$I_{OH} = 5 \cdot I_{REF}$	0.6V
0	1	50 Ω	$R_r = 475 \text{ } \Omega$, $I_{REF} = 2.32 \text{ mA}$	$I_{OH} = 6 \cdot I_{REF}$	0.7V
1	0	50 Ω	$R_r = 475 \text{ } \Omega$, $I_{REF} = 2.32 \text{ mA}$	$I_{OH} = 4 \cdot I_{REF}$	0.5V
1	1	50 Ω	$R_r = 475 \text{ } \Omega$, $I_{REF} = 2.32 \text{ mA}$	$I_{OH} = 7 \cdot I_{REF}$	0.8V



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, V_O	-0.5V to $V_{DD} + 0.5V$
Package Thermal Impedance, θ_{JA}	
48 Lead TSSOP	58.3°C/W (0 lfpm)
48 Lead SSOP	52.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				65	mA

TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{DD} + 0.3$	mV
V_{IL}	Input Low Voltage		-0.3		0.8	mV
I_{IH}	Input High Current	MULT_1, PWR_DWN# $V_{DD} = V_{IN} = 3.465V$			5	μA
		SEL_A, SEL_B, SEL_T, SEL_U, MULT_0 $V_{DD} = V_{IN} = 3.465V$			150	μA
I_{IL}	Input Low Current	MULT_1, PWR_DWN# $V_{DD} = 3.465V, V_{IN} = 0V$	-150			μA
		SEL_A, SEL_B, SEL_T, SEL_U, MULT_0 $V_{DD} = 3.465V, V_{IN} = 0V$	-5			μA
V_{OH}	Output High Voltage; NOTE 1		2.6			V
V_{OL}	Output Low Voltage; NOTE 1				0.5	V

All parameters measured at 200MHz in, 100MHz out on HOST_XX and 50MHz out on MREF.

Current adjust set for $V_{OH} = 0.7V$. Measurements refer to HOST_XX outputs only.

NOTE 1: Outputs terminated with 50Ω to $V_{DD}/2$. See Paramter Measurement Information Section, "3.3V Output Load Test Circuit".

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK, nPCLK $V_{DD} = V_{IN} = 3.465V$			5	μA
I_{IL}	Input Low Current	PCLK, nPCLK $V_{DD} = 3.465V, V_{IN} = 0V$	-5			μA
V_{PP}	Peak-to-Peak Input Voltage		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2		GND + 0.5		$V_{DD} - 0.85$	V

All parameters measured at 200MHz in, 100MHz out on HOST_XX and 50MHz out on MREF.

Current adjust set for $V_{OH} = 0.7V$. Measurements refer to HOST_XX outputs only.

NOTE 1: Common mode voltage is defined as V_{IH} .

NOTE 2: For single ended applications, the maximum input voltage for PCLK, nPCLK is $V_{DD} + 0.3V$.



TABLE 4D. HCSL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{OH}	Output Current		12.9		14.9	mA
V_{OH}	Output High Voltage	$R_{REF} = 475\Omega$, $R_{LOAD} = 50\Omega$ $I_{OH} = 6 \cdot I_{REF}$		0.7		V
V_{OL}	Output Low Voltage	$R_{REF} = 475\Omega$, $R_{LOAD} = 50\Omega$ $I_{OH} = 6 \cdot I_{REF}$		0.03		V
I_{OZ}	High Impedance Leakage Current		-10		10	μA
V_{OX}	Output Crossover Voltage		280		430	mV

All parameters measured at 200MHz in, 100MHz out on HOST_XX and 50MHz out on MREF.
Current adjust set for $V_{OH} = 0.7V$. Measurements refer to HOST_XX outputs only.

TABLE 5A. HCSL AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				600	MHz
t_{PD}	Propagation Delay; NOTE 1			3.7	4.0	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 4, 5			60	100	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 5				500	ps
$f_{jit(cc)}$	Cycle-to-Cycle Jitter				150	ps
t_R	Output Rise Time	20% to 80%	175		700	ps
t_F	Output Fall Time	20% to 80%	175		700	ps
odc	Output Duty Cycle		48		52	%

All parameters measured at 200MHz in, 100MHz out on HOST_XX and 50MHz out on MREF.
Current adjust set for $V_{OH} = 0.7V$. Measurements refer to HOST_XX outputs only.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: Maximum value calculated at $+3\sigma$ from typical.

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

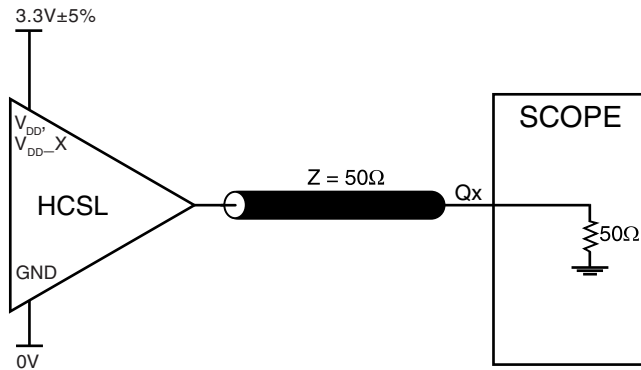
TABLE 5B. LVCMOS / LVTTTL AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				300	MHz
$f_{jit(cc)}$	Cycle-to-Cycle Jitter	$C_L = 10pF/30pF$			150	ps
t_R	Output Rise Time	0.4V to 2.4V, $C_L = 10pF$	0.4			ns
		0.4V to 2.4V, $C_L = 30pF$			1.8	ns
t_F	Output Fall Time	0.4V to 2.4V, $C_L = 10pF$	0.4			ns
		0.4V to 2.4V, $C_L = 30pF$			2	ns
odc	Output Duty Cycle	$C_L = 10pF/30pF$	48		52	%

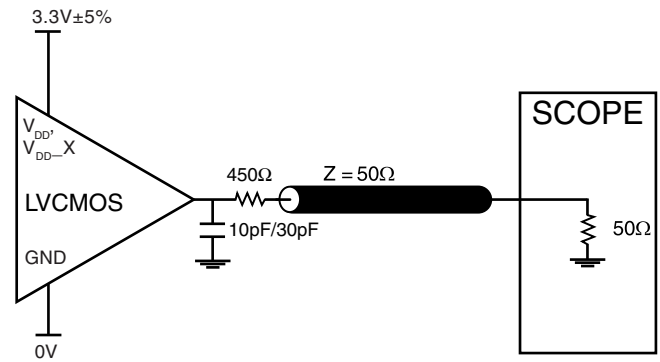
All parameters measured at 200MHz in, 100MHz out on HOST_XX and 50MHz out on MREF.
Current adjust set for $V_{OH} = 0.7V$. Measurements refer to MREF outputs only.



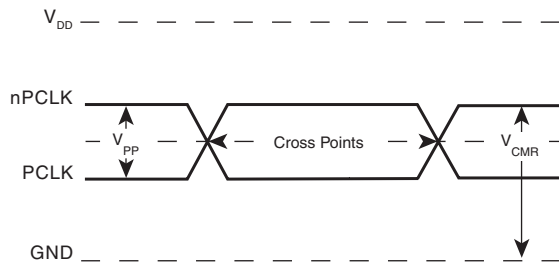
PARAMETER MEASUREMENT INFORMATION



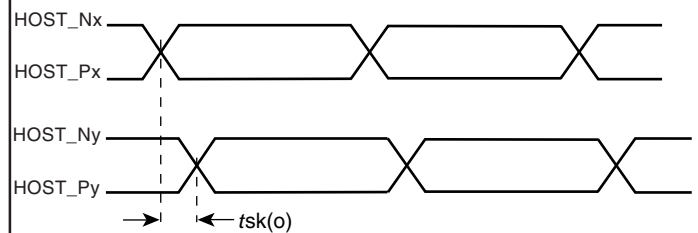
3.3V HCSL OUTPUT LOAD AC TEST CIRCUIT



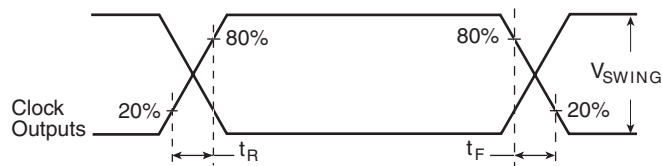
3.3V LVCMOS OUTPUT LOAD AC TEST CIRCUIT



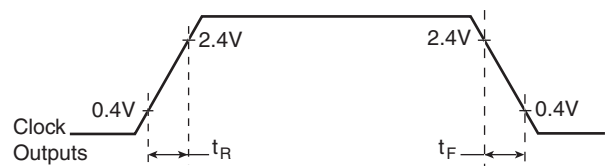
DIFFERENTIAL INPUT LEVEL



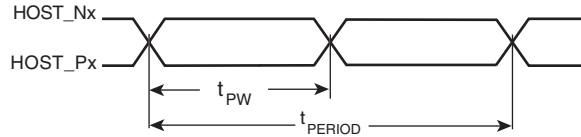
OUTPUT SKEW



HCSL OUTPUT RISE/FALL TIME

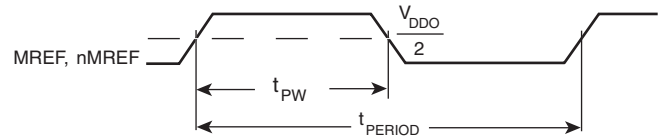


LVCMOS OUTPUT RISE/FALL TIME



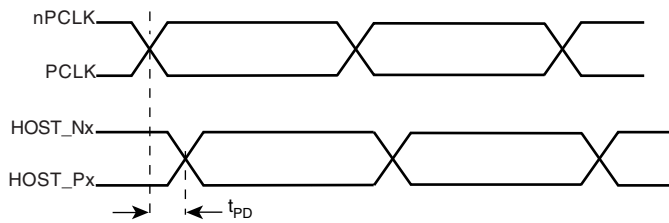
$$\text{odc} = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

HCSL OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



$$\text{odc} = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

LVCMOS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



PROPAGATION DELAY

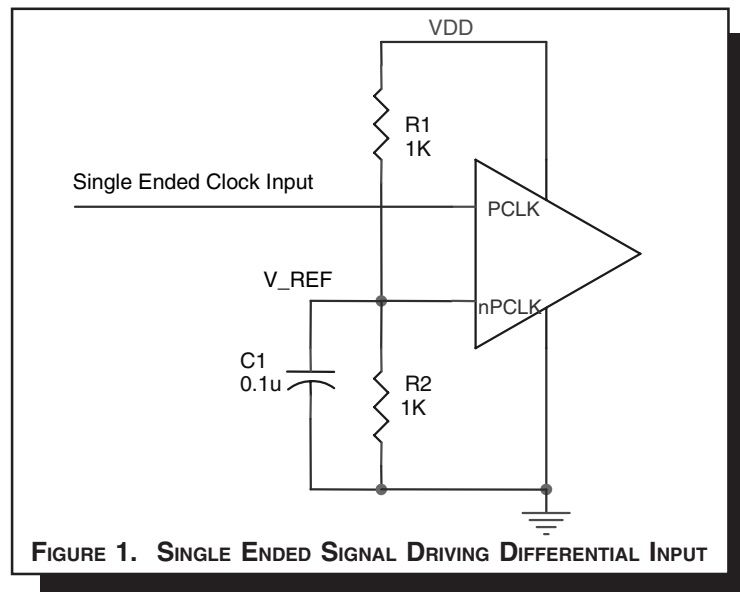


APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{DD} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.



RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

PCLK/nPCLK INPUT:

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

LVCMOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT:

All unused LVCMOS outputs can be left floating. There should be no trace attached.

HCSL OUTPUT

All unused HCSL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.



LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2F show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested

here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

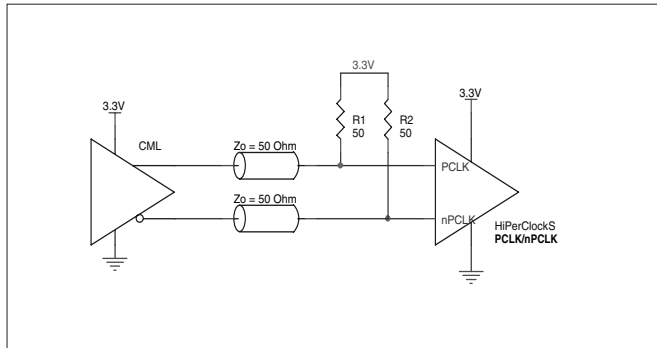


FIGURE 2A. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY AN OPEN COLLECTOR CML DRIVER

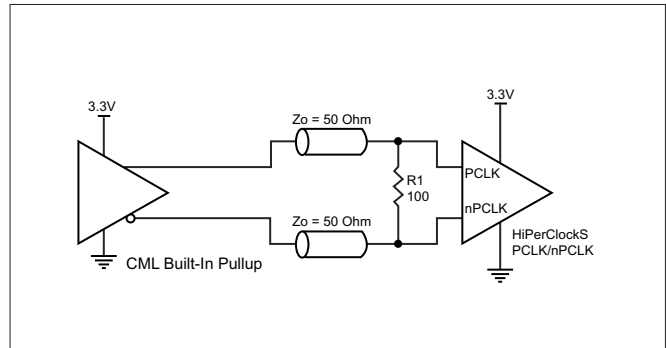


FIGURE 2B. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A BUILT-IN PULLUP CML DRIVER

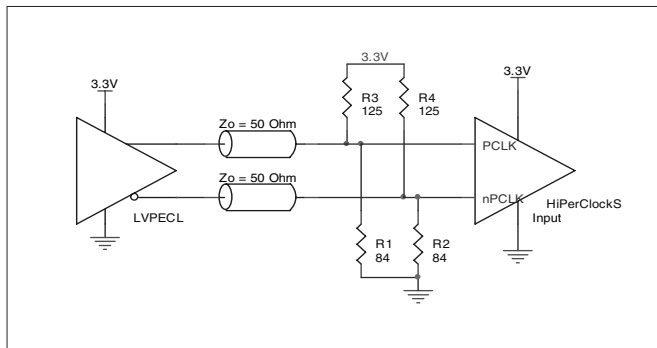


FIGURE 2C. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

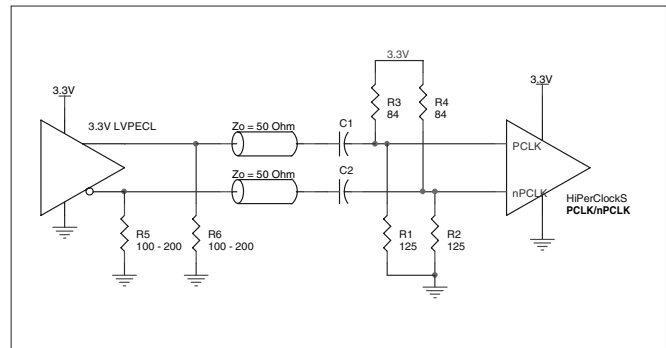


FIGURE 2D. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE

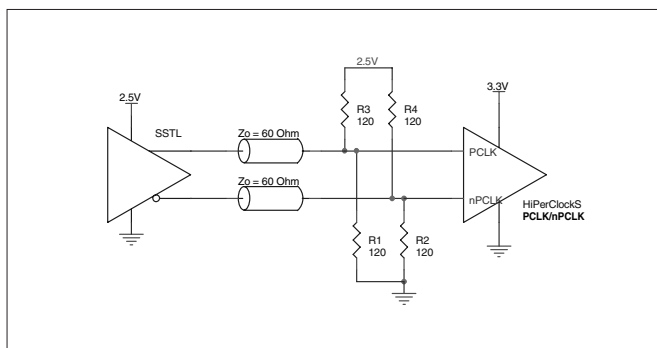


FIGURE 2E. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY AN SSTL DRIVER

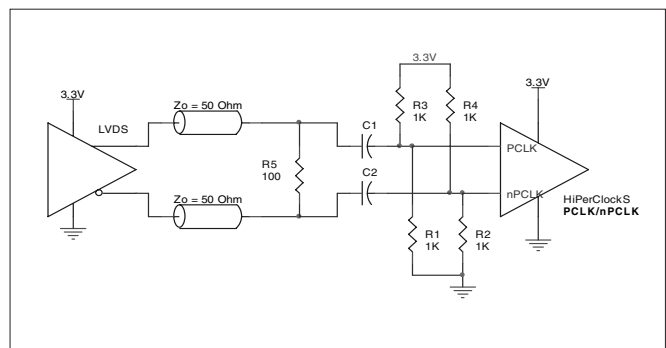


FIGURE 2F. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

SCHEMATIC EXAMPLE

Figure 3 shows an example of the ICS87158 LVPECL to HCSL Clock Generator schematic.

In this example, the ICS87158 is configured as follows:

PWR_DWN# = 1
 Mult_[1:0] = 10, Rref = 475Ω, IREF = 2.32mA, I_{OH} = 6*IREF
 SEL_[A,B,U] = 000, MREF = PECL ÷ 4, all HOST output = PECL ÷ 2
 SEL_T = 0, Output Enable

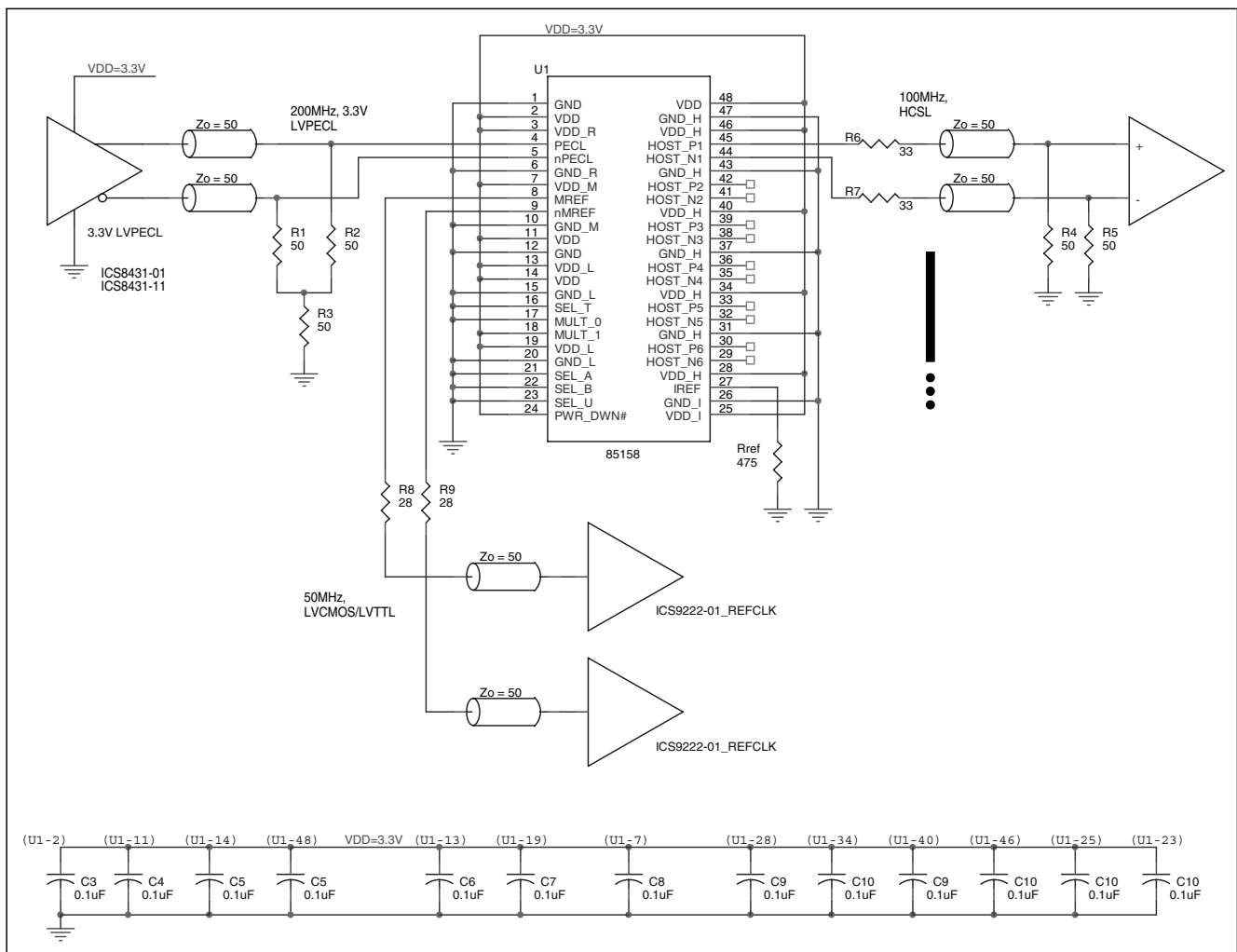


FIGURE 3. ICS87158 SCHEMATIC LAYOUT



Power and Ground

This section provides a layout guide related to power, ground and placement of bypass capacitors for a high-speed digital IC. This layout guide is a general recommendation. The actual board design will depend on the component types being used, the board density and cost constraints. The description assumes that the board has clean power and ground planes. The principle is to minimize the ESR between the clean power/ground plane and the IC power/ground pin.

A low ESR bypass capacitor should be used on each power pin. The value of bypass capacitors ranges from 0.01uF to 0.1uF. The bypass capacitors should be located as close

to the power pin as possible. It is preferable to locate the bypass capacitor on the same side as the IC. *Figure 4* shows suggested capacitor placement. Placing the bypass capacitor on the same side as IC allows the capacitor to have direct contact with the IC power pin. This can avoid any vias between the bypass capacitor and the IC power pins.

The vias should be placed at the Power/Ground pads. There should be minimum one via per pin. Increase the number of vias from the Power/Ground pads to Power/Ground planes can improve the conductivity.

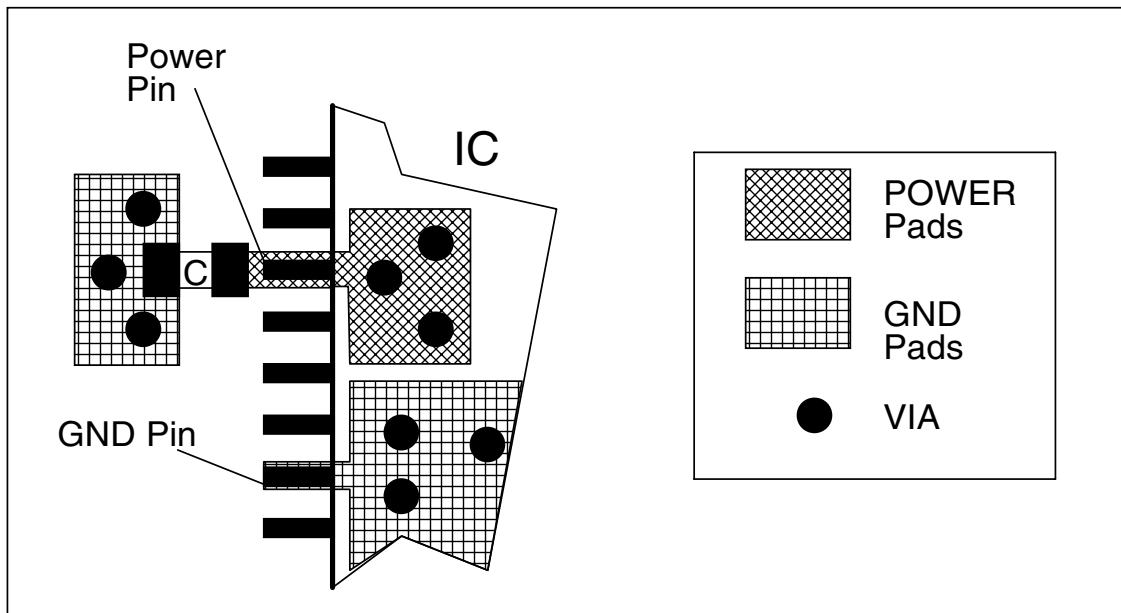


FIGURE 4. RECOMMENDED LAYOUT OF BYPASS CAPACITOR PLACEMENT



LOGIC CONTROL INPUT

The logic input control signals are 3.3V LVCMOS compatible. The logic control input contains ESD diodes and either pull-up or pull-down resistor as shown in *Figure 5*. The data sheet provides pull-up or pull-down information for each input pin. Leaving the input floating will set the control logic to default setting.

To set logic high, the input pin connected directly to V_{DD} . To set logic low, the control input connect directly to ground. For control signal source from the driver that has different power supply, a series current resistor of greater than 100 Ohm is required for random power on sequence.

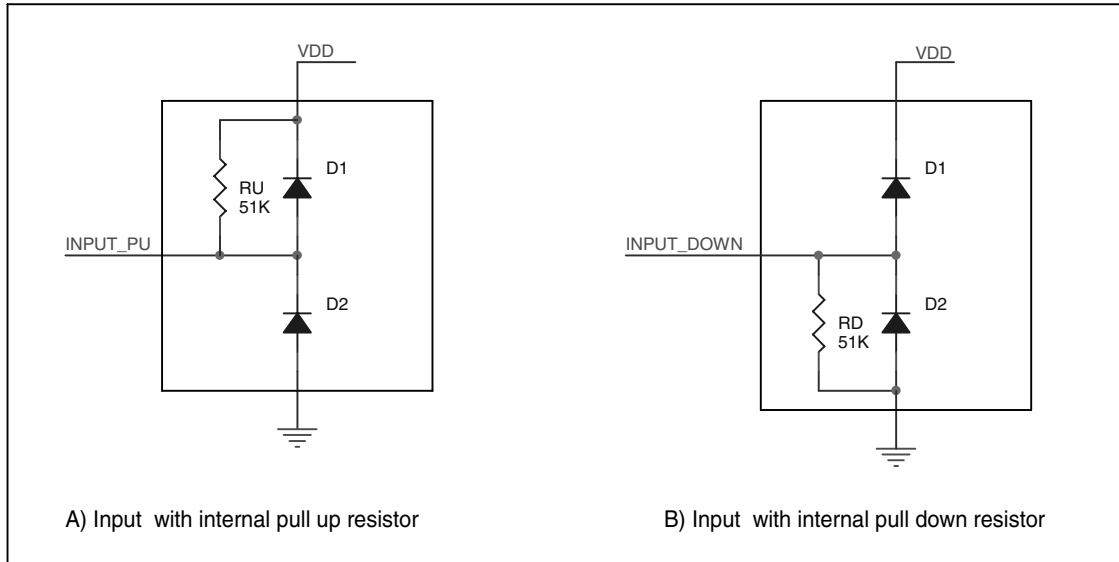


FIGURE 5. LOGIC INPUT CONTROLS

HCSL DRIVER TERMINATION

The HCSL is a differential constant current source driver. The output current is set by control pins $MULT_{[1:0]}$ and the value of resistor R_{ref} .

In the characteristic impedance of 50 Ohm environment, the match load 50 Ohm resistors R_4 and R_5 are terminated at the receiving end of the transmission line. The 33 Ohm series resistor R_6 and R_7 should be located as close to the driver pins as possible. For the clock traces that required very low skew should have equal length.

Other general rules of high-speed digital design also should be followed. Some check points are listed as follows:

- Avoid sharp angles on the clock trace. Sharp angle turn causes the characteristic impedance change on the transmission lines.
- Keep the clock trace on same layer. Whenever possible, avoid any vias on the middle clock traces. Any via on middle the trace can affect the trace characteristic impedance and hence degrade signal quality.
- There should be sufficient space between the clock traces that have different frequencies to avoid cross talk.
- No other signal trace is routed between the clock trace pair.
- Transmission line should not be routed across the split plane on the adjacent layer.



RELIABILITY INFORMATION

TABLE 6A. θ_{JA} vs. AIR FLOW TABLE FOR 48 LEAD TSSOP PACKAGE

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	82.6°C/W	70.3°C/W	63.7°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	58.3°C/W	52.3°C/W	49.9°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TABLE 6B. θ_{JA} vs. AIR FLOW TABLE FOR 48 LEAD SSOP PACKAGE

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Multi-Layer PCB, JEDEC Standard Test Boards	52.9°C/W	46.0°C/W	42.0°C/W

TRANSISTOR COUNT

The transistor count for ICS87158 is: 2631



PACKAGE OUTLINE - G SUFFIX FOR 48 LEAD TSSOP

PACKAGE OUTLINE - F SUFFIX FOR 48 LEAD SSOP

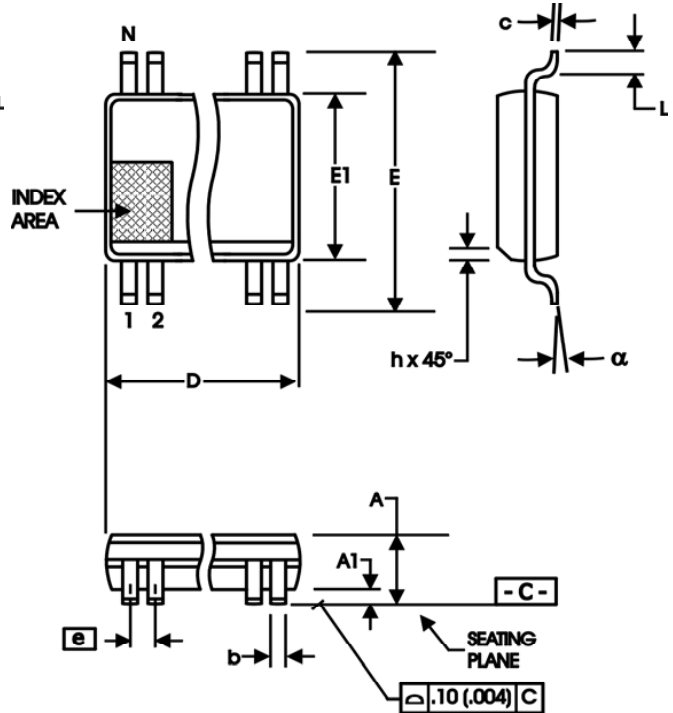
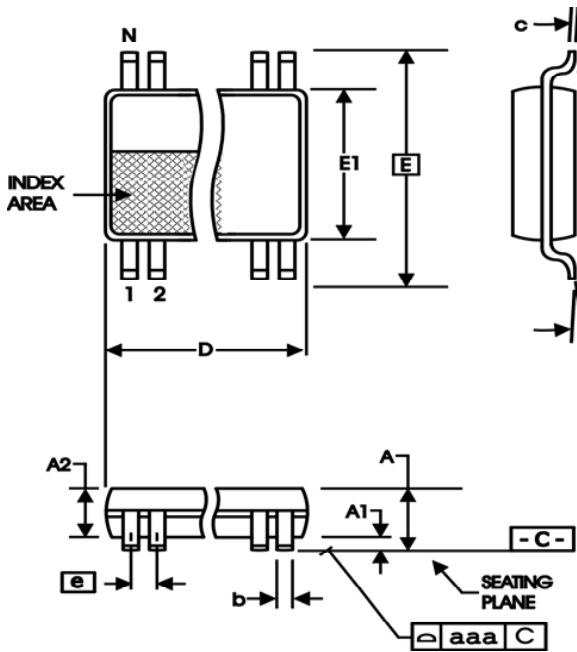


TABLE 6A. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	48	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.17	0.27
c	0.09	0.20
D	12.40	12.60
E	8.10 BASIC	
E1	6.00	6.20
e	0.50 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 6B. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	48	
A	2.41	2.80
A1	0.20	0.40
b	0.20	0.34
c	0.13	0.25
D	15.75	16.00
E	10.03	10.68
E1	7.40	7.60
e	0.635 BASIC	
h	0.38	0.64
L	0.50	1.02
α	0°	8°

Reference Document: JEDEC Publication 95, MO-118



Integrated
Circuit
Systems, Inc.

ICS87158

1-TO-6, LVPECL-TO-HCSL/LVCMOS

÷1, ÷2, ÷4 CLOCK GENERATOR

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS87158AG	ICS87158AG	48 Lead TSSOP	Tube	0°C to 85°C
ICS87158AGT	ICS87158AG	48 Lead TSSOP	1000 Tape & Reel	0°C to 85°C
ICS87158AGLF	ICS87158AGLF	48 Lead "Lead-Free" TSSOP	Tube	0°C to 85°C
ICS87158AGLFT	ICS87158AGLF	48 Lead "Lead-Free" TSSOP	1000 Tape & Reel	0°C to 85°C
ICS87158AF	ICS87158AF	48 Lead SSOP	Tube	0°C to 85°C
ICS87158AFT	ICS87158AF	48 Lead SSOP	1000 Tape & Reel	0°C to 85°C
ICS87158AFLF	ICS87158AFLF	48 Lead "Lead-Free" SSOP	Tube	0°C to 85°C
ICS87158AFLFT	ICS87158AFLF	48 Lead "Lead-Free" SSOP	1000 Tape & Reel	0°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
A		1	Pin Assignment - corrected typo error for Pin 4 and 5.	1/15/03
		6	Corrected 3.3V LVCMOS Output Load Test Circuit Diagram.	
		8	Updated Single Ended Signal Driving Differential Input Diagram. Updated format.	
B	T2 T4A	3	Pin Characteristics Table - changed C_{IN} 4pF max. to 4pF typical.	6/24/04
		4	Power Supply Table - changed I_{DD} 48mA typical to 65mA max.	
		9	Updated LVPECL Clock Input Interface section.	
B	T7	1	Added Lead-Free bullet to Features section.	7/8/04
		15	Added Lead-Free part number to Ordering Information table.	
B	T7	8	Added <i>Recommendations for Unused Input and Output Pins</i> .	1/17/06
		15	Ordering Information Table - added TSSOP Lead-Free part number and note.	
B	T7	15	Ordering Information Table - added TSSOP Lead-Free marking, and corrected TSSOP T&R count.	3/10/06