ICM7102B

LOW COST SINGLE CHIP TELEPHONE IC

FEATURES

- Includes dialer, speech, and ringer circuit replacing two or more ICs.
- Single board design meets multiple PTT requirements.
- Pause and mute functions.
- Adjustable flash duration.
- 32-digit last number redial.
- Selectable tone/pulse dialing.
- 13 to 70Hz ring frequency detection.
- Operating range from 15 to 100mA.
- Compatible with ICM7101D/ICM7102.

OVERVIEW

ICM7102B is a single chip telephone CMOS integrated circuits that meets multiple PTT requirements, allowing phone manufacturers to have single board design for various countries. This reduces inventory and simplify manufacturing processes.

ICM7102B integrates dialer, speech, and ringer circuits. The integration reduces component counts, hence increases product reliability.

TYPICAL APPLICATION CIRCUIT

Typical application circuit is as specified in Appendix A.

PACKAGE

28-Lead SOIC

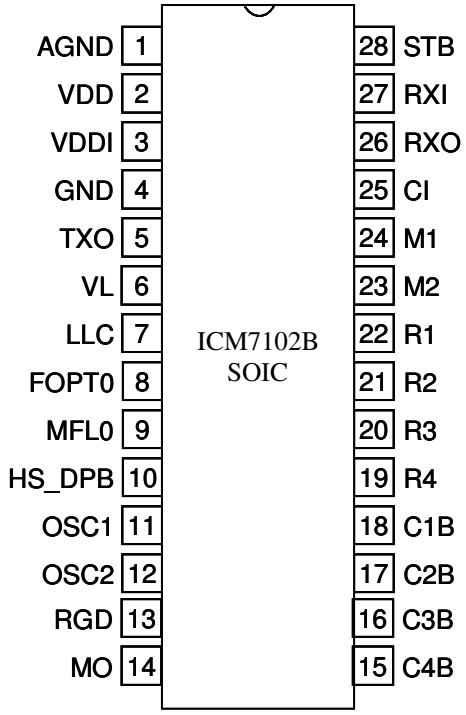


Figure 1: 28-lead SOIC Package

PIN DESCRIPTION

Pin No	Symbol	Description
1	AGND	**Analog Ground** 1.4V regulated voltage output. Used by internal amplifiers. External capacitor about 100uF should be connected to this pin.
2	VDD	**Regulated Supply Voltage** When HS_DPB pin is HIGH, the VDD pin is regulated to 3.1V, and the input power is extracted from VDDI pin. When HS_DPB is LOW, VDD should be externally powered and it must not fall below 1.0V to retain the redial memory. Most internal circuits are powered by VDD pin.
3	VDDI	**Supply Input Voltage** Power for the chip is extracted from this VDDI pin. See also VDD pin description. At steady state, VDDI is regulated to 3.5V by use of external PNP transistor whose base terminal is connected to the TXO pin. See typical application circuit. The external PNP transistor also functions to drain the excess line current.
4	GND	**Ground**
5	TXO	**Transmit Output** Transmit output is to be connected to external PNP transistor (typically medium power PNP) for the modulation of line voltage and for shorting the line during make period of pulse dialing. See the typical application circuit. The external PNP transistor also functions to drain the excess line current.
6	VL	**Line Voltage** If line-loss compensation (LLC) scheme is not used, then this pin can be shorted to GND. If LLC scheme is used, then this pin is used to sense the line current. The sense resistor (R11 in typical application circuit) must be 30 ohm for the LLC scheme to work properly. The receive and transmit gains are adjusted according to the sensed current and the chosen LLC scheme. See also description on "Line Loss Compensation" section. Since VL pin will typically experience high transient voltage, it is advisable to properly add external protection circuit to suppress the high transient voltage which can damage the pin.
7	LLC	**Line Loss Compensation** Line loss compensation scheme options: LLC=GND - No LLC scheme. LLC=AGND - "Low" LLC scheme. LLC=VDD - "High" LLC scheme. The receive and transmit gains are adjusted according to the sensed current and the chosen LLC scheme. See description on "Line Loss Compensation" section.
8	FOPT0	**Flash Option** Flash duration options: GND (logic 0) – 300ms flash duration. VDD (logic 1) – 600ms flash duration.
9	MFL0	**DTMF Option** Transmitted DTMF level options: GND (logic 0): typical -8/-10dB. VDD (logic 1): typical -6/-8dB.
10	HS_DPB	**Hook Switch Input and Dial Pulse Output** When off-hook, this pin needs to be pulled HIGH (by the hook switch) to activate the speech and dialer circuits. When on-hook this pin needs to be pulled LOW to activate ringer circuit and deactivate speech and dialer circuits. During pulse dialing (while off-hook, and pulse dialing mode is chosen), this pin is pulled LOW during line-break periods.

11	OSC1	**Oscillator Input** 3.58MHz ceramic resonator input.
12	OSC2	**Oscillator Output** 3.58MHz clock output. Can be used to drive other few high impedance inputs.
13	RGD	**Ring Detection Input** Input for ring frequency detection. Active when HS_DPB=LOW. When pulses with frequency between 13Hz and 70Hz are detected on this pin, ring melody is generated on the MO pin.
14	MO	**Melody Output** Open drain output. When ring signal is detected on the RGD pin, ring melody pulses are generated on this pin.
15 16 17 18	C4B C3B C2B C1B	**Keypad Columns** Keypad column inputs. When a column input pin is shorted to a row output pin, appropriate DTMF signal is generated. This DTMF signal complies with CCITT recommendation. For example, when R1 and C1B are shorted (when button #1 is pressed), DTMF signal of frequency 697Hz + 1209Hz is generated and transmitted thru TXO pin.
19 20 21 22	R4 R3 R2 R1	**Keypad Rows** Keypad rows. Logic pulses are generated on these pins to scan user input. See also Keypad Column pins. During power-on-reset, these pins are also used to determine various dialing modes. See description on Dialing Function section.
23 24	M1 M2	**Microphone Inputs** Input for electret microphone. M1 connects to inverting input of internal differential amplifier via a resistor. M2 connects to the non-inverting input via a resistor.
25	CI	**Complex Impedance and AC Impedance Input** Placing resistor between CI and AGND pins adjusts the AC impedance. If CI pin is left floating the typical AC impedance is 1000 ohm (when current sense resistor (R11) is 30 ohm).
26	RXO	**Received Audio Amplifier Output** Received audio amplifier output. RXO can drive a typical 120-ohm dynamic earpiece speaker.
27	RXI	**Received Audio Amplifier Input** Non-inverting input for internal received audio differential amplifier. RXI connects to the amplifier via an internal resistor. RXI also internally connects to the feedback path of the circuitry that determines the AC impedance.
28	STB	**Side Tone Balance Input** Inverting input for internal received audio differential amplifier. STB connects to the amplifier via an internal resistor.

FUNCTIONAL DESCRIPTION

SYSTEM STARTUP

ICM7102B generates internal power-on-reset when VDD reaches around 1.5V. Power-on-reset appropriately initiates the system to a known initial state. Note that the initial ramp up of VDD could come from external ringer interface circuit, or it could come from internal regulator when the system goes off-hook.

As long as HS_DPB pin stays LOW, ICM7102B operates in shutdown mode with only the ringer circuitry being activated to monitor the incoming ringing signal.

OSCILLATOR

All the timing of ICM7102B is based on a clock frequency of 3.58 MHz. A Crystal or ceramic resonator of this frequency should be connected to OSC1 and OSC2 pins. Care has to be taken in selecting this components since in practise minor deviations from the nominal frequency may occur due to the characteristics of the oscillator.

It is recommended to connect a small value capacitors (≤ 47pF) in parallel with the oscillator to ensure proper start-up and operation at the nominal frequency.

TONE RINGER

The tone ringer of ICM7102B consists of ring detection circuit and melody generator circuit. These circuits are active when the system is in on-hook state (HS_DPB pin is LOW).

Ring Detection Circuit

Ring detection circuit will assures the signal present on RGD pin input is valid. The signal is considered valid if it has frequencies between 13Hz and 70Hz. This signal is monitored continuously and the ring melody is turned on/off accordingly.

Melody Generator

Once the valid ring signal is detected on the schmitt-triggered ring detection pin (RGD) and the signal is present for about 75 ms continously, the melody generator will be enabled, generating ring tones of 1250Hz and 1600Hz on the MO pin. Note that MO is an open-drain pin.

SPEECH NETWORK

The speech network of ICM7102B consists of a transmitter and a receiver path, side tone cancellation and line loss compensation.

The speech network is activated as soon as the phone goes off-hook (i.e. when HS_DPB pin goes HIGH). At the same time the ringer circuitry is deactivated.

Transmit

The typical total transmit gain from microphone input (M1/M2 pins) to the VDDI pin is 35dB when the AC impedance is 600Ω.

Receive

The typical total receive gain from the line voltage to RXO pin is 5dB when the AC impedance is 600Ω.

Side Tone Cancellation

As shown in the typical application circuit in Appendix A, side tone cancellation can be achieved best by balancing the Whitestone bridge comprised of R11, R12, R13+R14//C6, and the line impedance.

Line Loss Compensation

LLC pin input level is scanned as the phone goes off-hook (i.e. as HS_DPB pin goes HIGH). At the same time, the loop current level is sensed and determined. If LLC=0, no compensation scheme is in effect.

If LLC=AGND, "low" compensation scheme is in effect. Transmit and receive gains are reduced by as much as 6dB when the loop current exceeds 50mA.

If LLC=VDD, "high" compensation scheme is in effect. Transmit and receive gains are reduced by as much as 6dB when the loop current exceeds 75mA.

AC Impedance (Z_{AC})

Placing a resistor, R_{ZAC} between CI and AGND pins adjusts the AC impedance. If R_{ZAC} is not

present, the typical AC impedance is 1000Ω. Refer to Figure 2 for the equivalent test circuit. R_{ZAC}=82KΩ typically sets the AC impedance to 600Ω, while R_{ZAC}=47KΩ typically sets the AC impedance to 470Ω. Please note that the overall system AC impedance also depends on the whole system circuit.

DTMF Signal Level

DTMF signal level can be selected by setting MFL0 pin as follow:

MFL0	Typical DTMF level (R_{ZAC}=47KΩ; Z_{AC} = 470Ω)
0	Low, typical -8/-10dB
1	High, typical -6/-8dB

DIALING FUNCTIONS

Keypad arrangement is as shown in the typical application circuit in Appendix A. Dialing modes are selectable using the pull-up/pull-down resistors connected to the row inputs.

As soon as the phone goes off-hook (i.e when HS_DPB pin goes HIGH), voltage levels on keypad row inputs (R1 thru R4) are first scanned to determine the operating mode as follow:

Pin	Function	Level – Mode
R1	Dialing Mode	0 – MF mode 1 – Pulse mode
R2	Pulse Period	0 – 10 PPS 1 – 20 PPS
R3	Make/Break Ratio	0 – 40/60 1 – 33/67
R4	DTMF option	0 – 82ms/82ms 1 – 82ms/160ms

Valid Keys

ICM7102B has a total of 16 valid keys. It scans the keys by asserting known state on pins R1, R2, R3, and R4 in sequence, and check which column (pins C1B, C2B, C3B, C4B) is shorted to which row. The following specify the combinations:

	C1B	*C2B*	*C3B*	*C4B*
R1	**1**	**2**	**3**	**Pause**
R2	**4**	**5**	**6**	**Mute**
R3	**7**	**8**	**9**	**Flash**
R4	*	**0**	#	**LNR**

DTMF Tones

The DTMF tone generator creates 12 tones in compliance with CCITT Recommendation. There are two group of frequencies of DTMF tones. The low group depends on the key's row, while the high group depends on the key's column as illustrated in the following table:

	C1B	*C2B*	*C3B*	*Low Freq*
R1	**1**	**2**	**3**	697 Hz
R2	**4**	**5**	**6**	770 Hz
R3	**7**	**8**	**9**	852 Hz
R4	*	**0**	#	941 Hz
High Freq	1209 Hz	1336 Hz	1477 Hz	

Last Number Redial (LNR)

The last Number Redial (LNR) is a facility of ICM7102B to allow resignalling of the last manually dialled number without keying in all digits again. The LNR is repeatable after each off-hook.

A manually entered number is stored in internal 32-digit RAM. VDD shall not fall below 1.0V during on-hook state to properly retain the data in the memory.

Flash

ICM7102B asserts line break (pulls down HS_DPB pin) when Flash key is depressed. The flash duration depends on the input levels of FOPT0 pin as follow:

FOPT0	Flash Duration
0	300 ms
1	600 ms

Mute

ICM7102B inhibits mic (M1/M2) input when Mute key is depressed. Depressing the key again toggles the mute function.

Pause

ICM7102B pauses (no dialing and microphone is muted) for 2.2 seconds when Pause key is depressed.

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
VDDI	Supply Line Voltage	-0.3 to 7.0	V
V_{IN}	Digital Input Voltage	-0.3 to 7.0	V
T_{STG}	Storage Temperature	-55 to +150	°C
T_{SOL}	Soldering Temperature	300	°C

Note 1: Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature
Commercial	-25 °C to 70 °C

DC CHARACTERISTICS

(I_{LINE} = 15mA unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VDDI	Regulated Line Voltage	I_{LINE}: 13mA to 100mA	3.2	3.5	3.8	V
VDD	Regulated Supply			3.1		V
AGND	Regulated Reference		1.3	1.4	1.5	V
I_{DD}	Operating Current	Speech mode		2.5	5.5	mA
		Dialing mode		4.0	5.5	mA
		Ring mode		0.3		mA
I_{OL}	Output Current Sink	HS_DPB, MO; V_{OL} = 0.4V		1.5		mA
VIL	Input Voltage Low	HS_DPB, RGD; T_A=25°C	0.0		1.5	V
VIH	Input Voltage High	HS_DPB, RGD; T_A=25°C	2.2		6.0	V

AC CHARACTERISTICS

(I_{LINE} = 15mA, Frequency = 800Hz, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Transmit (TX)						
G_{TX}	Transmit Gain	LLC=GND, Z_{AC}=600Ω	31.5	33	32.5	dB
THD	Distortion	V_L < 0.5 V_{RMS}			2	%
$Z_{IN\ M1,M2}$	Input Impedance			20		KΩ
G_{MUTE}	Mute Attenuation	Mute activated	80			dB
$V_{IN\ M1,M2}$	Input Voltage Range			± 2.8		V_{PEAK}
Receive (RX)						
G_{RX}	Receive Gain	LLC=GND, Z_{AC}=600Ω, Volume=Reset	4.0	5.0	6.0	dB
THD	Distortion	V_{RXI} < 0.5 V_{RMS}			2	%
$Z_{IN\ RXI}$	Input Impedance			8		KΩ
$V_{IN\ RXI}$	Input Voltage Range			± 2.8		V_{PEAK}

Side Tone (ST)						
G_{ST}	Side Tone Cancellation	LLC=GND, Z_{AC}=600Ω	23			dB
$Z_{IN\ STB}$	Input Impedance			80		KΩ
$V_{IN\ STB}$	Input Voltage Range			± 2.8		V_{PEAK}
Output Driver (BJT)						
$V_{IN\ PNP}$	Input Voltage Range			± 2.8		V_{PEAK}
V_{TXPNP}	Dynamic Range			± 2.8		V_{PEAK}
Return Loss						
RL	Return Loss	Z_{LINE}=600Ω, Z_{AC}=600Ω	18			dB
Keyboard						
t_D	Key debounce time			64		ms
HS/DPB INPUT						
t_{HS-L}	Low to High Debounce	Going off-hook		15		ms
t_{HS-H}	High to Low Debounce	Going on-hook		240		ms
Tone Ringer						
V_{MO}	Melody Output			PDM		
t_{MD}	Melody Delay				10	ms
F1	Frequency 1			1250		Hz
F2	Frequency 2			1600		Hz
t_{DT}	Detection Time	Ring Freq = 20Hz	50		80	ms
f_{MIN}	Min. Detection Freq.		13			Hz
f_{MAX}	Max. Detection Freq.				70	Hz
DTMF						
F	Frequency Deviation	note 2	-0.31		+0.75	%
t_{TD}	Tone Duration	note 1	80	82	84	ms
t_{ITP}	Inter Tone Pause	note 1	80	82	84	ms

Note 1: The values are valid during automatic dialing and are minimum values during manual dialing, i.e. the tones will continue as long as the key is depressed.
Note 2: This does not include the frequency deviation of the ceramic resonator.

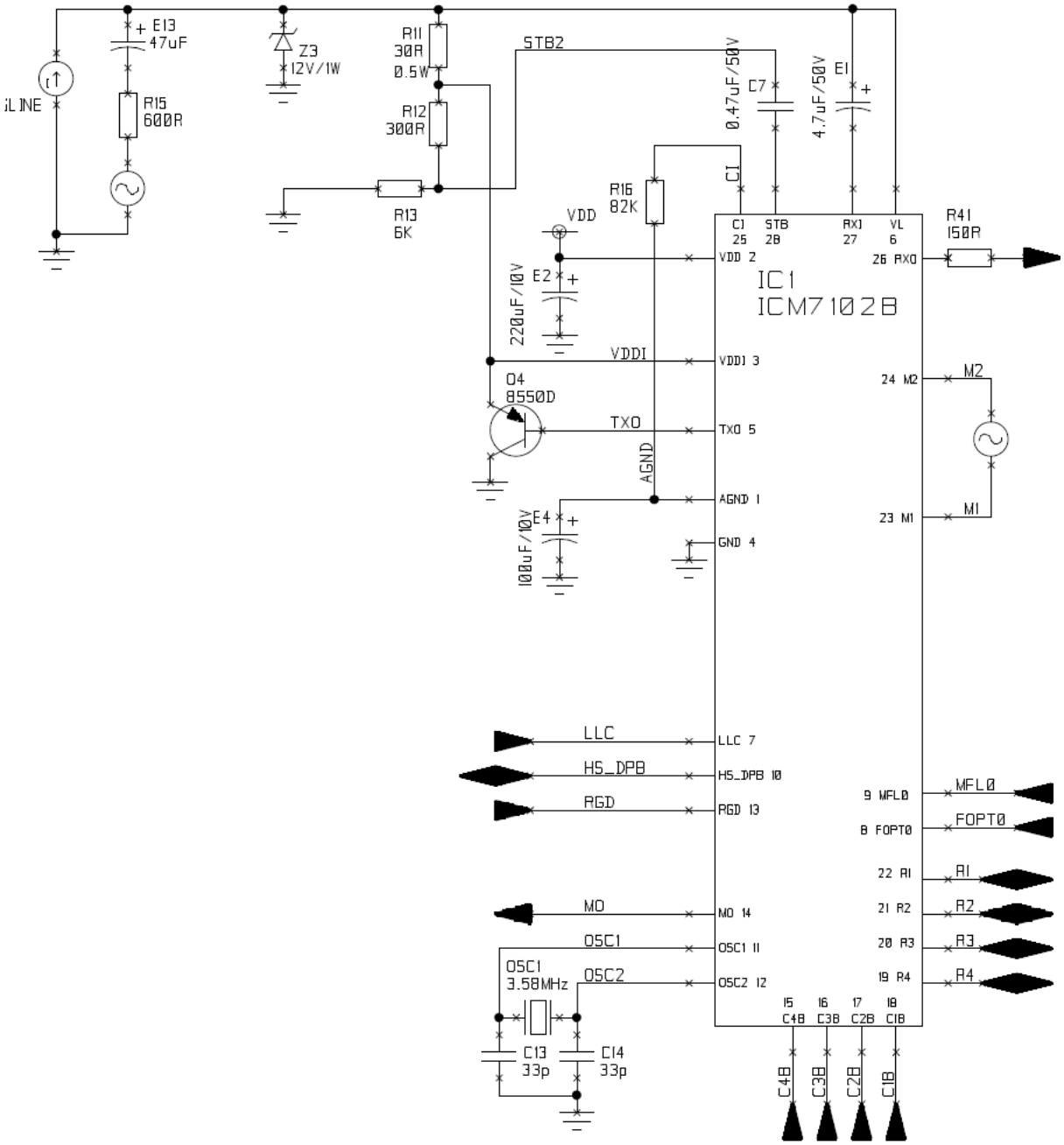
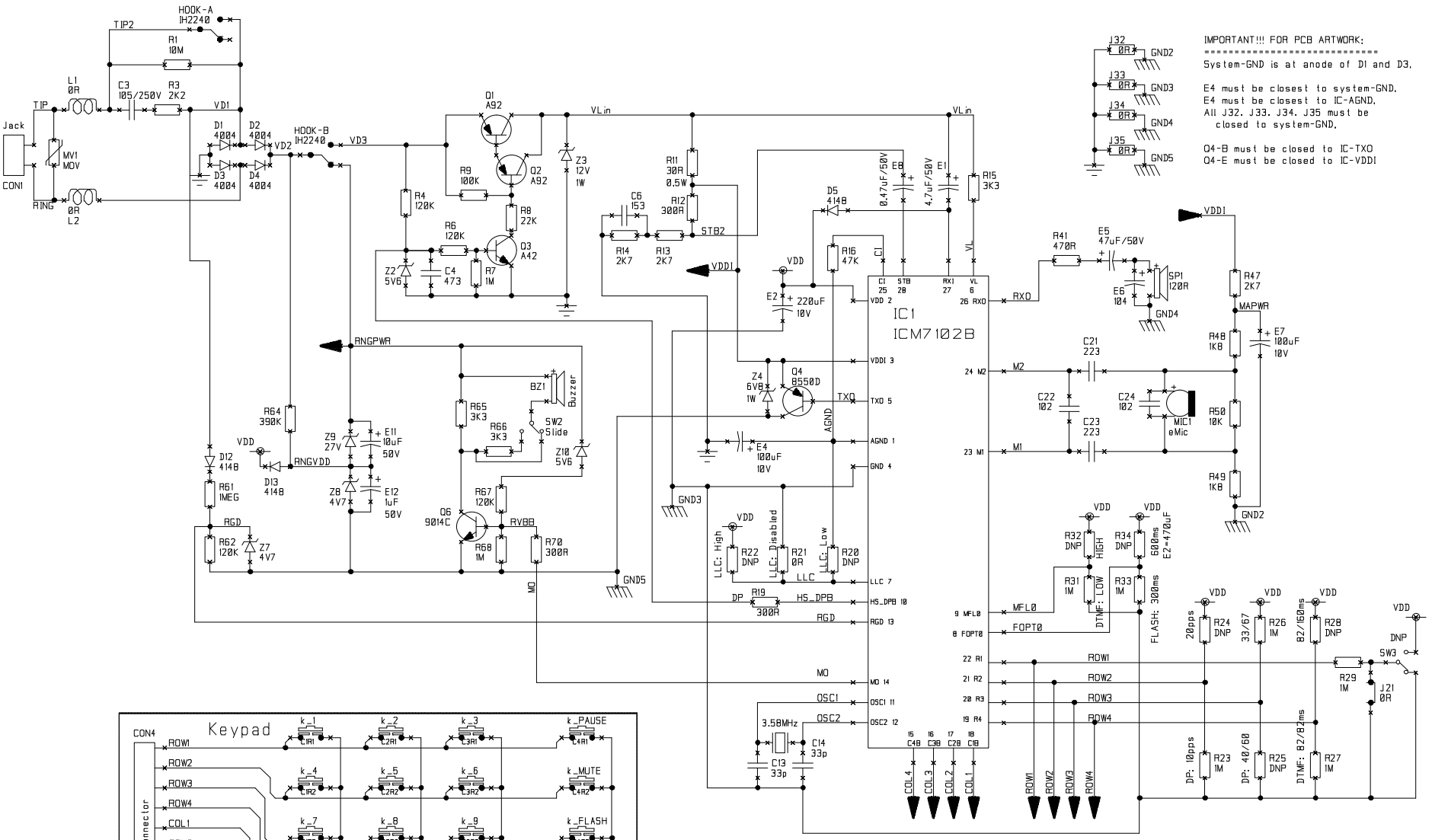
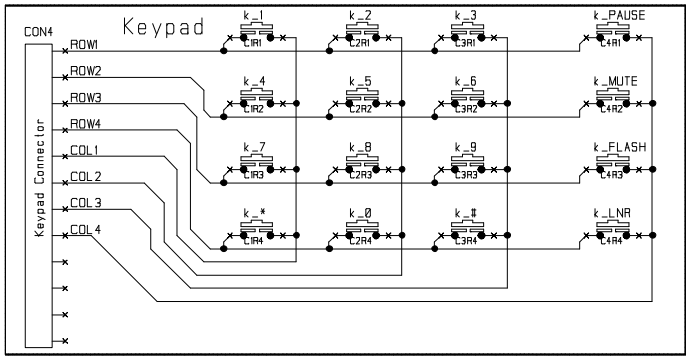


Figure 2: Equivalent Test Circuit

APPENDIX A: TYPICAL APPLICATION CIRCUIT





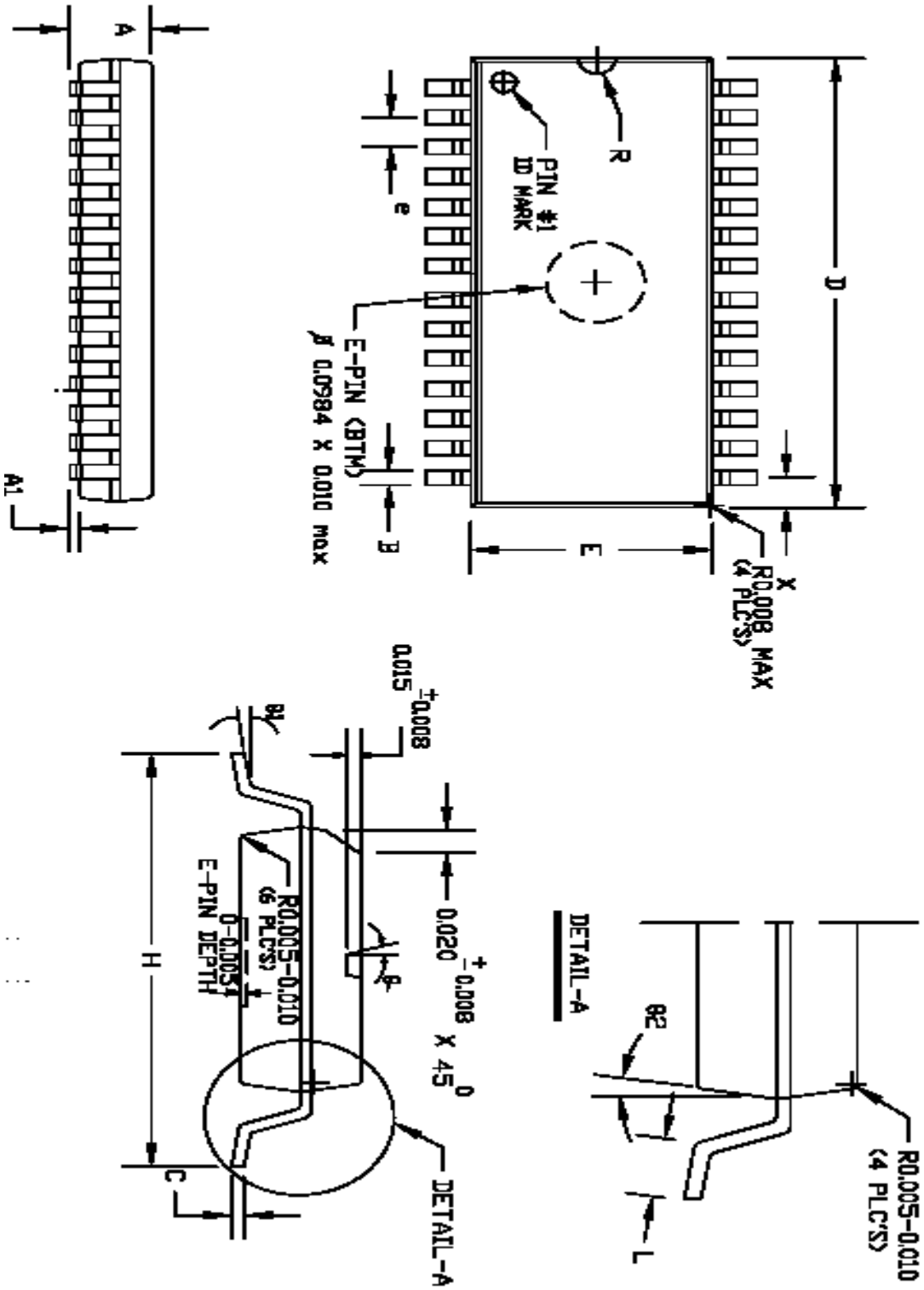
LEGEND:
* DNP - Do Not Populate

ICmic reserves the right to change the specifications without prior notice.

CONTRACT NO.		COMPANY NAME	IC Microsystems Sdn Bhd
APPROVALS	DATE	DWG	7102HA03
DRAWN	3-DEC-10	SIZE: B	FSCM NO. / DWG NO. / REV.: 4.1
CHECKED	3-DEC-10		
ISSUED	3-DEC-10	SCALE	SHEET 1 of 1

APPENDIX B: PACKAGE INFORMATION

28-Lead SOP (Unit: Inches)



SYMBOL	28 SOIC	
	MIN	MAX
A	0.096	0.104
A1	0.004	0.012
B	0.014	0.020
D	0.698	0.706
E	0.291	0.299
H	0.398	0.414
e	0.050 BSC	
C	0.009	0.011
L	0.020	0.040
X	0.026 REF	
R	0.025	0.035
α	7° BSC	
θ1	0°	8°
θ2	7° BSC	

NOTE:
1) LEAD COPLANARITY SHOULD BE 0 TO 0.10MM (0.004") MAX.
2) PACKAGE SURFACE FINISHING:
   (2.1) TOP: MATTE (CHARMILLES # 24-27)
   (2.2) ALL SIDE: MATTE (CHARMILLES # 24-27)
   (2.3) BOTTOM: MATTE (CHARMILLES # 24-27)
3) ALL DIMENSIONS EXCLUDING MOLD FLASHES.
4) MAX DEVIATION OF CENTER OF PACKAGE AND CENTER OF LEADFRAME TO BE 0.10MM (0.004").
5) MAX MISALIGNMENT BETWEEN TOP AND BTM CENTER OF PACKAGE TO BE 0.10MM (0.004").

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