

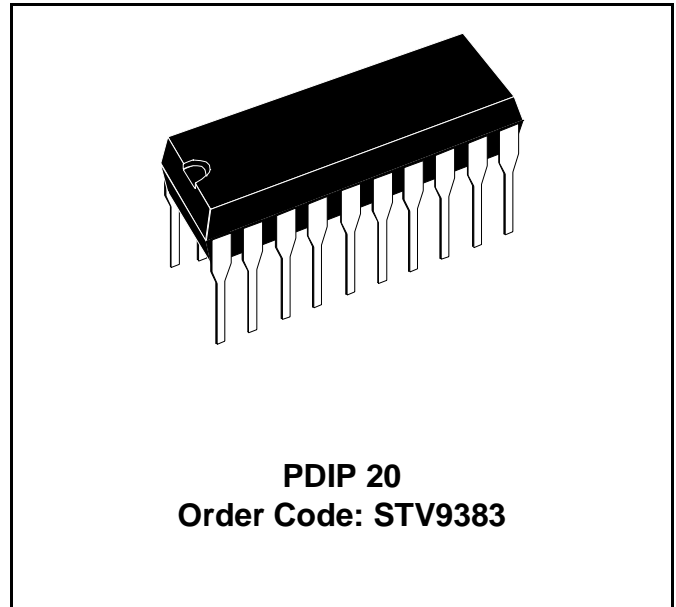


# STV9383

## Class-D Vertical Deflection Amplifier for 2.0 Amp TV and Monitor Applications

### Main Features

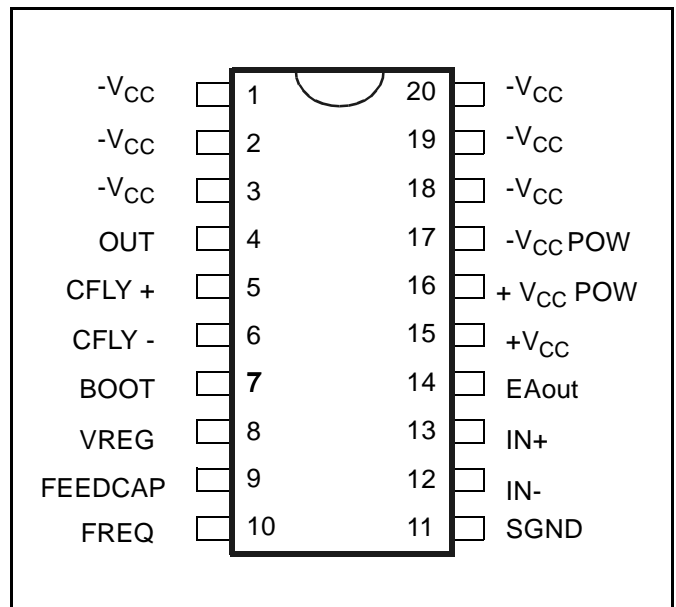
- High-Efficiency Power Amplifier
- No Heatsink
- Split Supply
- Internal Flyback Generator
- Output Current up to 2.0 A<sub>PP</sub>
- Suitable for DC Coupling Applications
- Few External Components
- Protection against Low V<sub>CC</sub>



### Description

Designed for TV and monitor applications, the STV9383 is a Class-D vertical deflection booster assembled in a 20-pin plastic DIP package.

It operates with supplies up to  $\pm 18$  V and provides an output current up to 2.0 A<sub>PP</sub> to drive the yoke. The internal flyback generator avoids the need for an extra power supply.



# 1 Pin Functions

Table 1: STV9383 Pin Descriptions

| Pin | Name             | Function                        | Pin | Name                 | Function                            |
|-----|------------------|---------------------------------|-----|----------------------|-------------------------------------|
| 1   | -V <sub>CC</sub> | Negative Supply                 | 11  | SGND                 | Signal Ground                       |
| 2   | -V <sub>CC</sub> | Negative Supply                 | 12  | IN-                  | Error Amplifier Inverting Input     |
| 3   | -V <sub>CC</sub> | Negative Supply                 | 13  | IN+                  | Error Amplifier Non-inverting Input |
| 4   | OUT              | PWM Output                      | 14  | EA out               | Error Amplifier Output              |
| 5   | CFLY+            | Flyback Capacitor               | 15  | +V <sub>CC</sub>     | Positive Supply                     |
| 6   | CFLY-            | Flyback Capacitor               | 16  | +V <sub>CC</sub> POW | Positive Power Supply               |
| 7   | BOOT             | Bootstrap Capacitor             | 17  | -V <sub>CC</sub> POW | Negative Power Supply               |
| 8   | VREG             | Internal Voltage Regulator      | 18  | -V <sub>CC</sub>     | Negative Supply                     |
| 9   | FEEDCAP          | Feed-back Integrating Capacitor | 19  | -V <sub>CC</sub>     | Negative Supply                     |
| 10  | FREQ             | Frequency Setting Resistor      | 20  | -V <sub>CC</sub>     | Negative Supply                     |

Note 1. The voltage reference, accessible on pin 8, is for internal use only. No additional components should be connected to this pin except the decoupling capacitor.

## 2 Functional Description

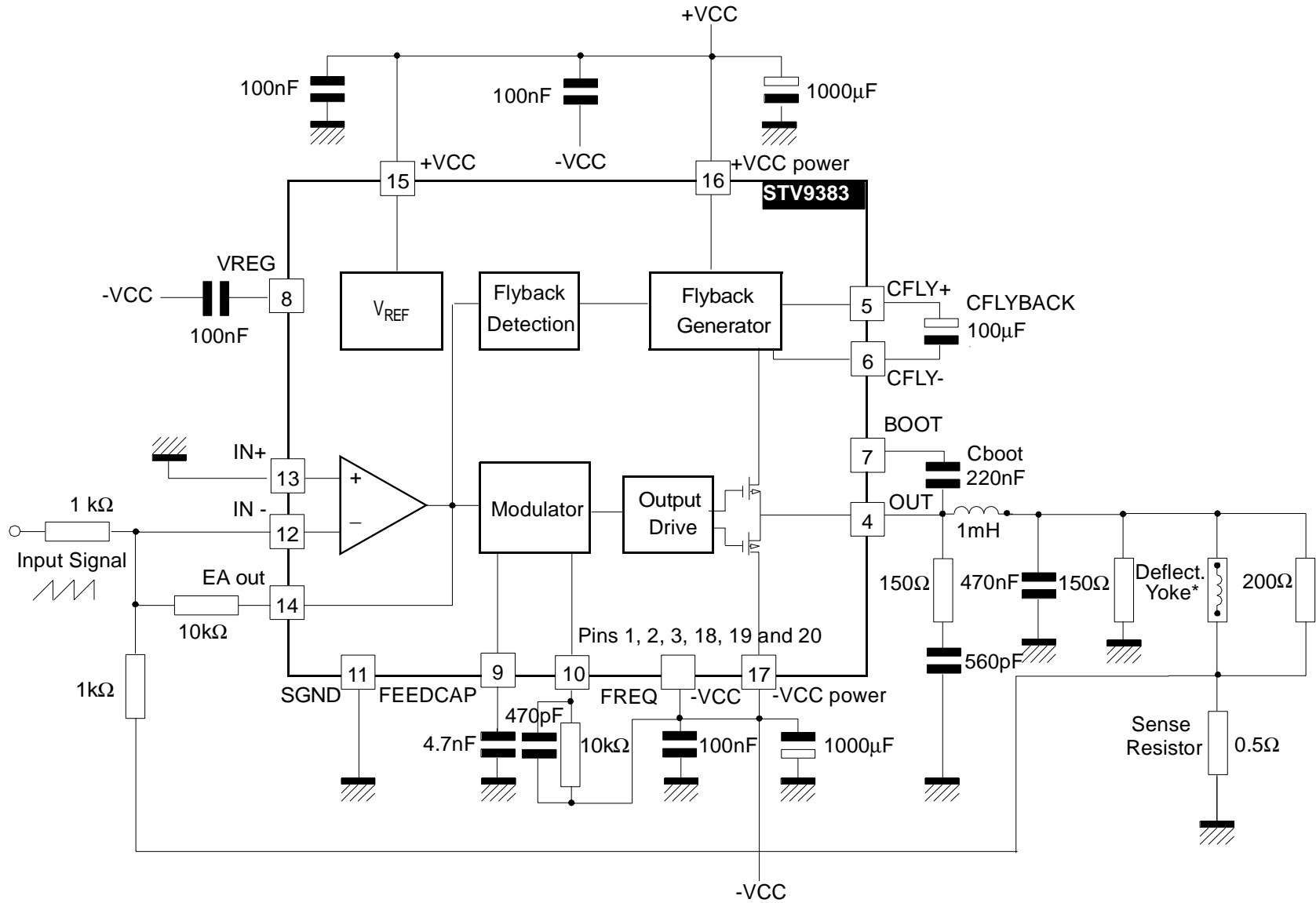
The STV9383 is a vertical deflection circuit operating in Class D. Class D is a modulation method where the output transistors work in switching mode at high frequency. The output signal is restored by filtering the output square wave with an external LC filter. The major interest of this IC is the comparatively low power dissipation in regards to traditional amplifiers operating in class AB, eliminating the need of an heatsink.

Except for the output stage which uses Class D modulation, the circuit operation is similar to the one of a traditional linear vertical amplifier.

A (sawtooth) reference signal has to be applied to the circuit which can accept a differential or single ended signal. This sawtooth is amplified and applied as a current to the deflection yoke. This current is measured by means of a low value resistor. The resulting voltage is used as a feedback signal to guarantee the conformity of the yoke current with the reference input signal.

The overvoltage necessary for a fast retrace is obtained with a chemical capacitor charged at the power supply voltage of the circuit. At the flyback moment, this capacitor is connected in series with the output stage power supply. This method, used for several years with the linear vertical boosters and called "internal flyback" or "flyback generator", avoids the need of an additional power supply, while reducing the flyback duration.

The circuit uses a BCD process that combines Bipolar, CMOS and DMOS devices. The output stage is composed of low-R<sub>ON</sub> N-channel DMOS transistors.

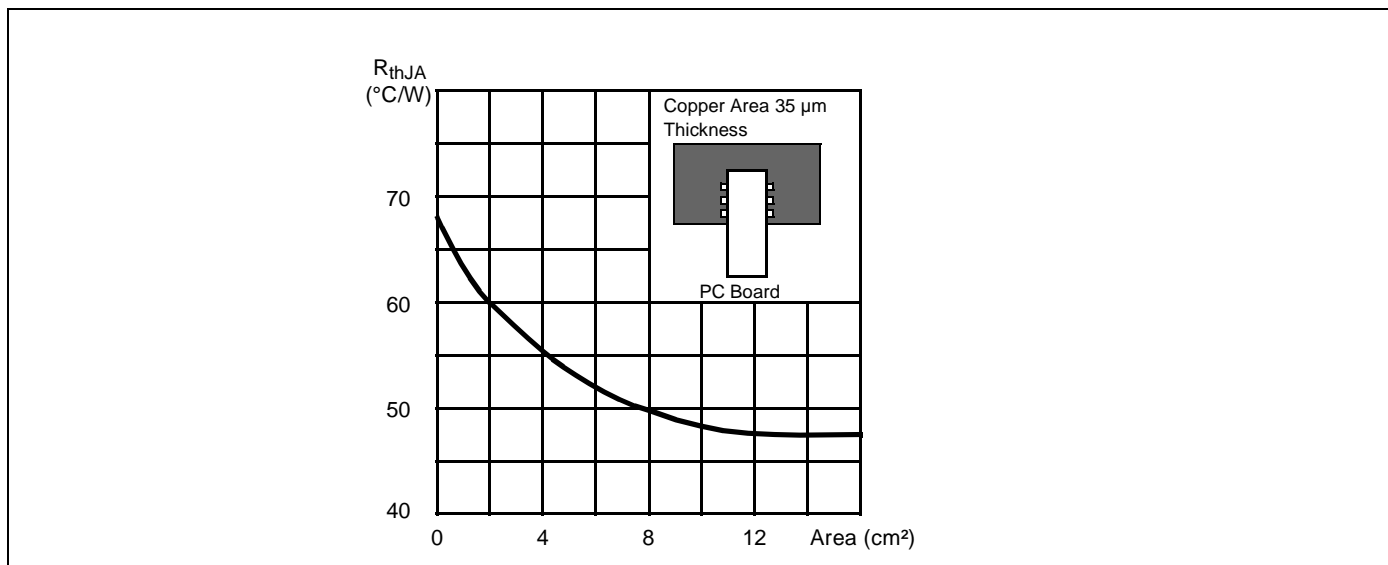


\* Deflection yoke characteristics:  $R = 5.5\Omega$ ,  $L = 7\text{mH}$

$f_{\text{VERT}} = 50\text{ Hz}$

Figure 1: Test and Application Circuit Diagram

Figure 2: Thermal Resistance with “On-board” Square Heatsink vs. Copper Area



### 3 Absolute Maximum Ratings

| Symbol                            | Parameter   | Value       | Unit |
|-----------------------------------|---|-------------|------|
| V <sub>CC</sub>                   | DC Supply Voltage   | ±20         | V    |
| T <sub>STG</sub> , T <sub>J</sub> | Storage and Junction Temperature  | -40 to +150 | °C   |
| T <sub>OP</sub>                   | Operating Temperature Range   | -20 to +70  | °C   |
| V <sub>ESD</sub>                  | ESD Susceptibility - Human Body Model (100 pF discharge through 1.5 kΩ)   | ±2          | kV   |
| I <sub>OUT</sub>                  | Output current  | ±1.3        | A    |
| V <sub>OUT</sub>                  | Maximum output voltage (pin 4) with respect to -V <sub>CC</sub> (pins 1, 2, 3, 18, 19 and 20) and during flyback (see Note 1) | 80          | V    |

Note 1. During the flyback with V<sub>CC</sub> = ±18 V, the maximum output voltage (pin 4) is close to 72 V, with respect to -V<sub>CC</sub> (pins 1, 2, 3, 18, 19 and 20).

### 4 Thermal Data

| Symbol            | Parameter                              | Value | Unit |
|-------------------|--|-------|------|
| R <sub>thJA</sub> | Junction-to-Ambient Thermal Resistance | 70    | °C/W |

Pins 1, 2, 3, 18, 19 and 20 are internally connected together and participate in heat evacuation.

## 5 Electrical Characteristics

$T_{AMB} = 25^{\circ} C$ ,  $V_{CC} = \pm 12 V$  and  $f_{VERT} = 50 Hz$  unless otherwise specified (refer to Figure 1)

| Symbol                            | Parameter   | Test Conditions                   | Min. | Typ.      | Max.    | Units      |
|-----------------------------------|---|-----------------------------------|------|-----------|---------|------------|
| +V <sub>CC</sub>                  | Positive Supply Range   |                                   | +10  |           | +18     | V          |
| -V <sub>CC</sub>                  | Negative Supply Range   |                                   | -18  |           | -10     | V          |
| $\Delta V_{CC}$                   | Maximum recommended difference between +V <sub>CC</sub> and  -V <sub>CC</sub> |                                   |      |           | $\pm 4$ | V          |
| V <sub>CCSTART</sub>              | Low V <sub>CC</sub> Detection   |                                   |      | $\pm 6.5$ |         | V          |
| I <sub>Q</sub>                    | Quiescent Supply Current  | Input Voltage = 0                 |      | 14        |         | mA         |
| I <sub>Y</sub>                    | Maximum Vertical Yoke Current   |                                   |      |           | $\pm 1$ | A          |
| I <sub>13</sub> , I <sub>12</sub> | Amplifier Input Bias Current  |                                   |      | -0.1      |         | $\mu A$    |
| V <sub>OS</sub>                   | Output Offset Voltage   | Note 1                            | -50  |           | +50     | mV         |
| SVR                               | Supply Voltage Rejection  | Note 2                            |      | 82        |         | dB         |
| Fly <sub>THR</sub>                | Flyback Detection Threshold (Positive Slope)                                  | V(14)                             |      | 1.5       |         | V          |
| Fly <sub>THF</sub>                | Flyback Detection Threshold (Negative Slope)                                  | V(14)                             |      | 0.5       |         | V          |
| P <sub>D</sub>                    | Integrated Circuit Dissipated Power   | Note 3                            |      | 0.85      |         | W          |
| f <sub>SW</sub>                   | Switching Frequency   | R <sub>FREQ</sub> = 10 k $\Omega$ | 120  | 140       | 160     | kHz        |
| f <sub>SW-OP</sub>                | Switching Frequency Operative Range   |                                   | 100  |           | 200     | kHz        |
| R <sub>FREQ</sub>                 | Frequency Controller Resistor Range   | Pin 10                            | 7    | 10        | 14      | k $\Omega$ |

Note 1. Input voltage = 0, measured after the filter (e.g. across the 470 nF filter capacitor)

- Supply rejection of the positive or negative power supply. V<sub>CC</sub> ripple = 1 V<sub>PP</sub>, f = 100 Hz, measured on the sense resistor.
- Power dissipated in the circuit in the case of the application from Figure 1 and the current in the deflection yoke adjusted to 2 A<sub>PP</sub>. The corresponding power dissipated in the vertical deflection yoke is 1.8 W.

## 6 I/O Waveforms

The following waveforms are obtained with the schematic diagram given in Figure 1: Test and Application Circuit Diagram.

Figure 3: Current in the Deflection Yoke (Calibration: 0.5 A/div.)

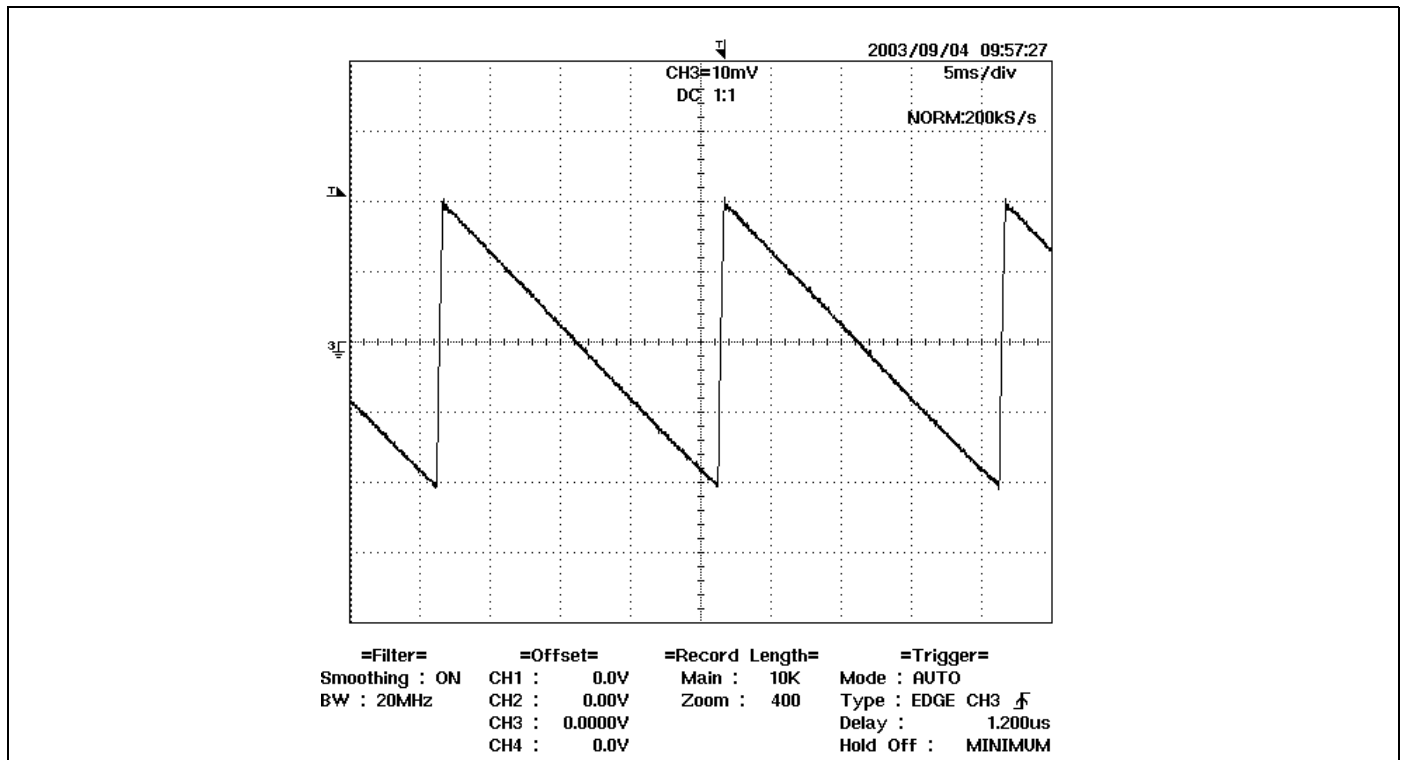


Figure 4: Current and Voltage in the Deflection Yoke during Flyback (Calibration: 0.5A/div, 10 V/div)

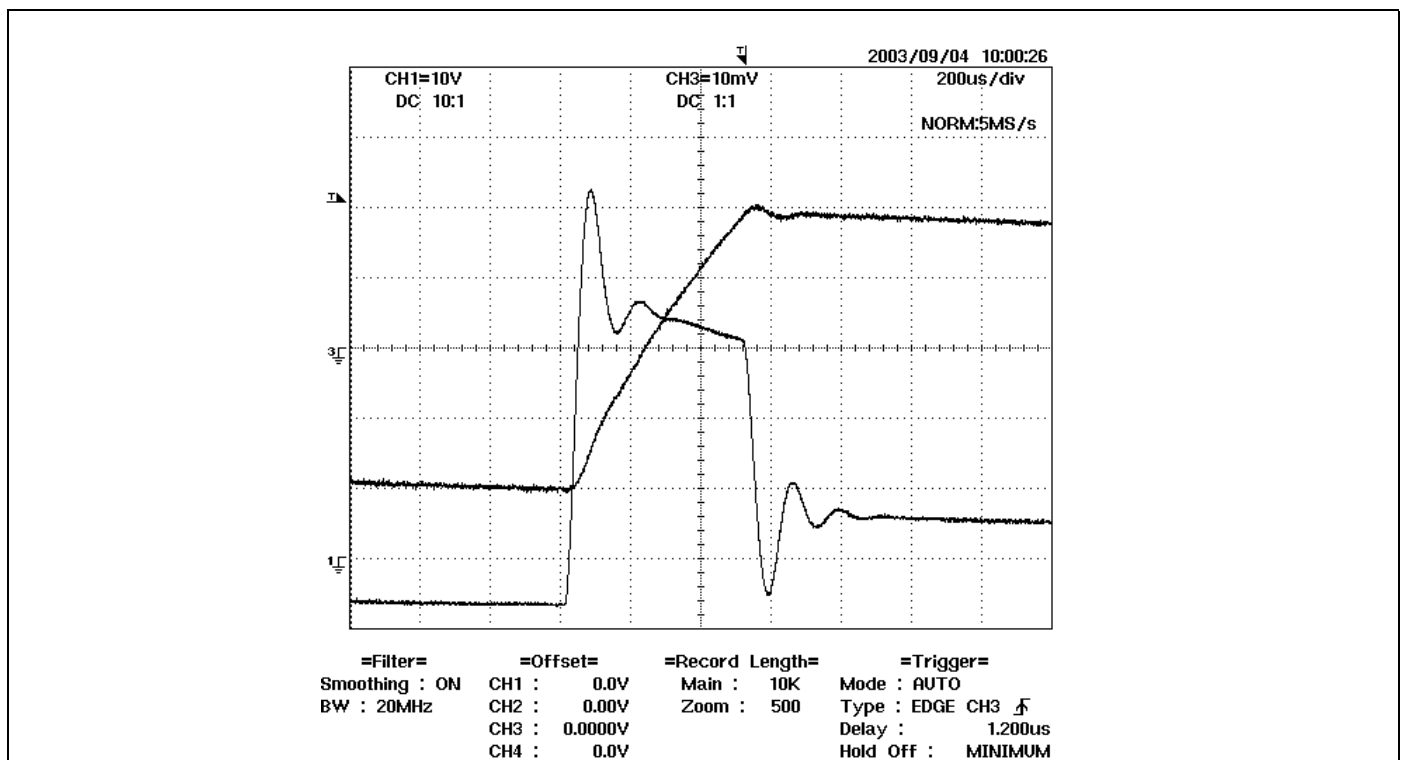


Figure 5: Current in the Deflection Yoke and Voltage at the Error Amplifier Output (pin 14 - STV9383) during Flyback (Calibration: 0.5 A/div, 1 V/div)

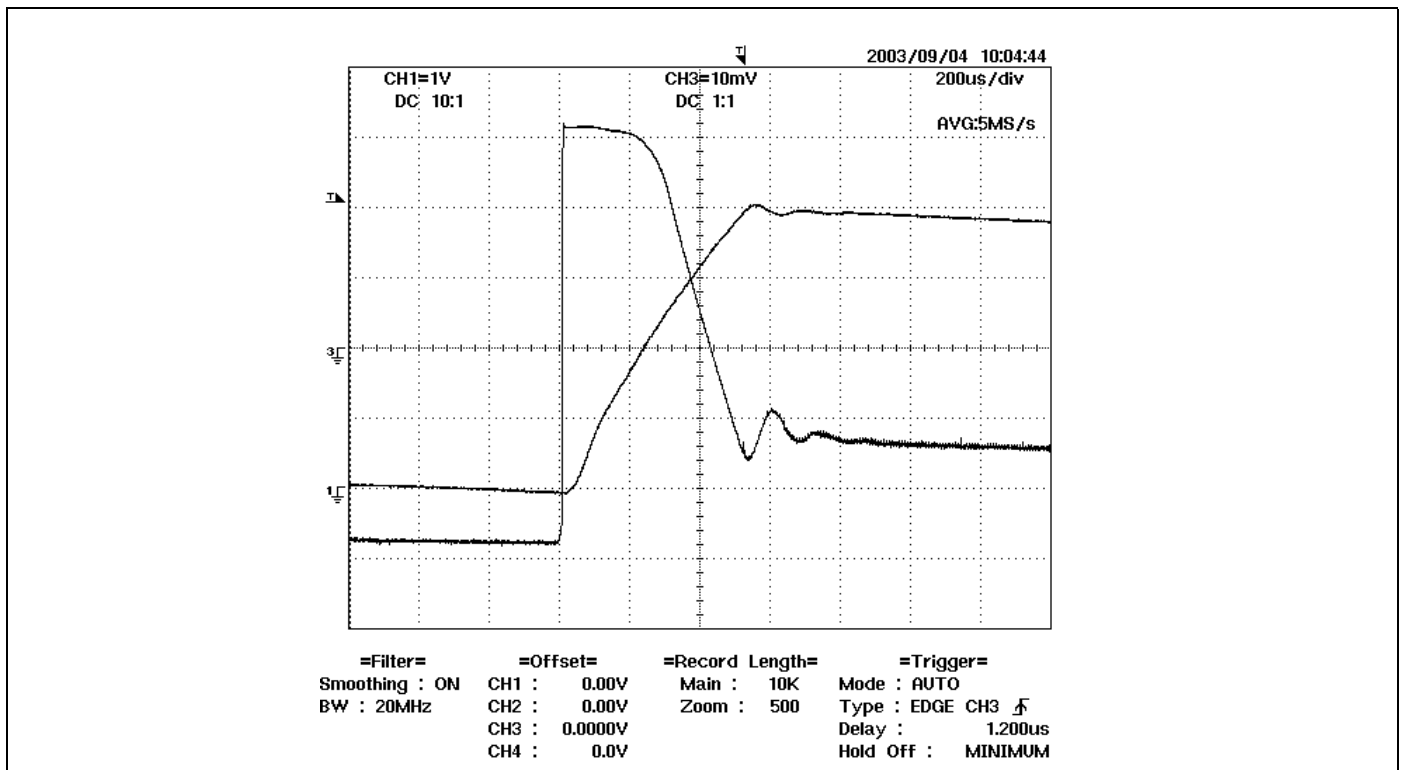
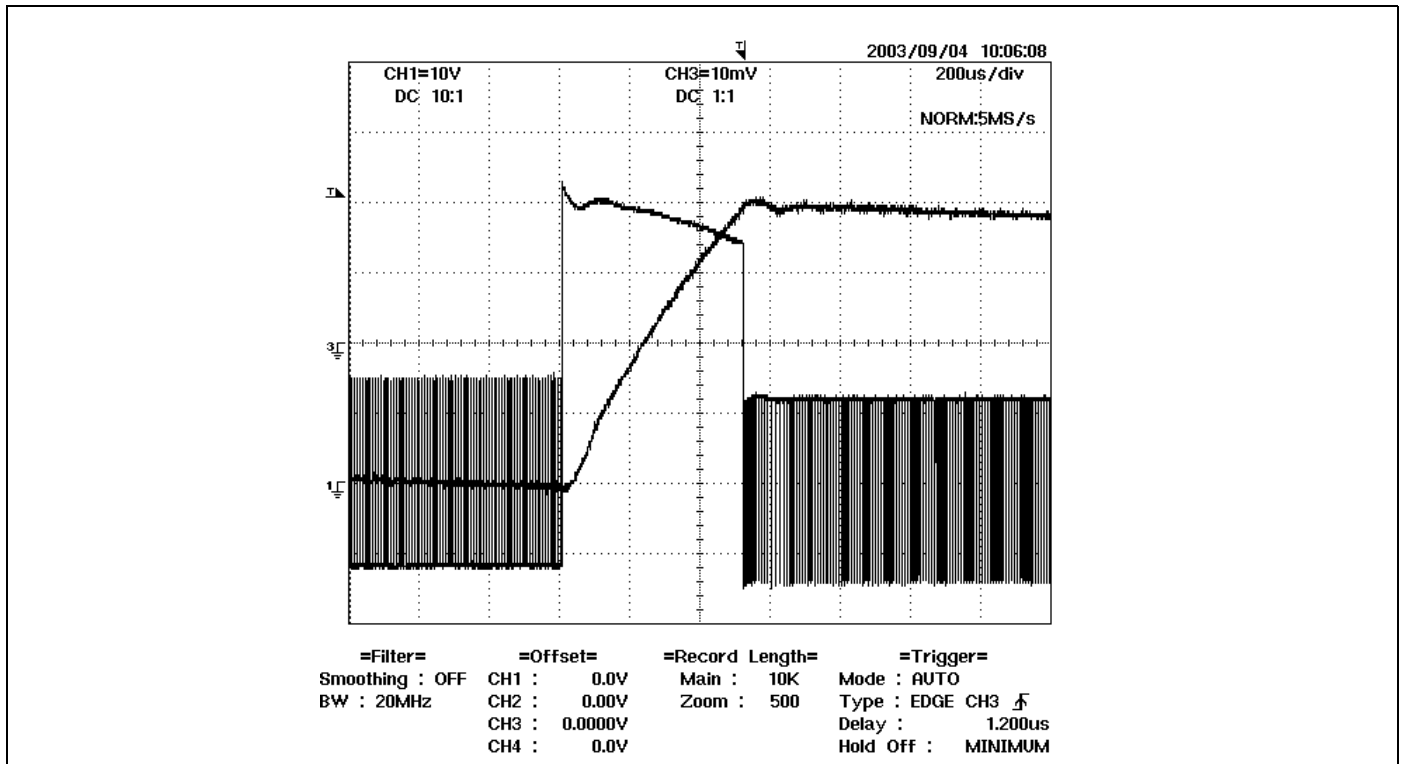


Figure 6: Current in the Deflection Yoke and Voltage at the Output of the STV9383 (pin 4), during the Flyback (Calibration: 0.5 A/div, 10 V/div)



# 7 Package Mechanical Data

Figure 7: 20-Pin Plastic Dual In-Line Package, 300-mil Width

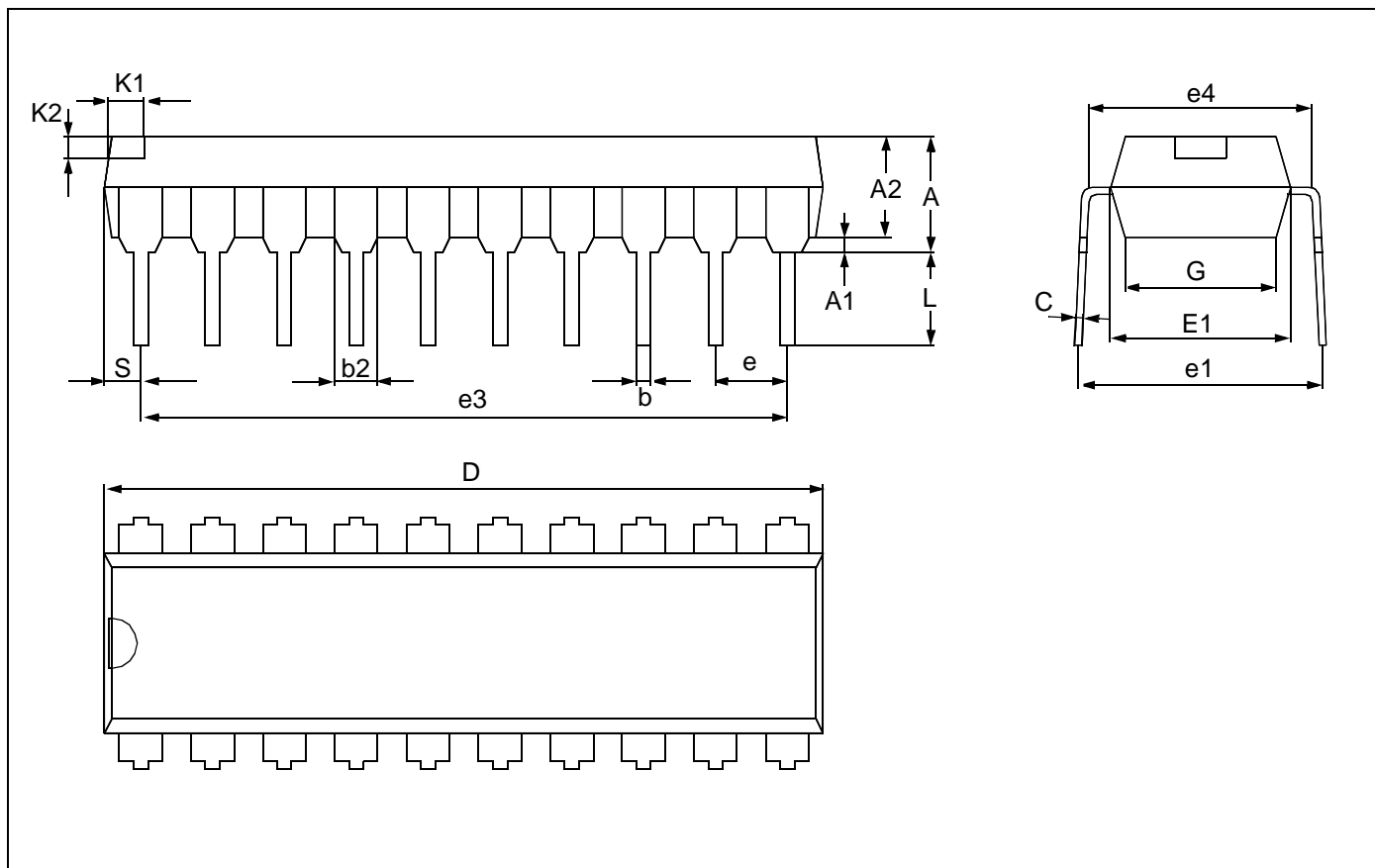
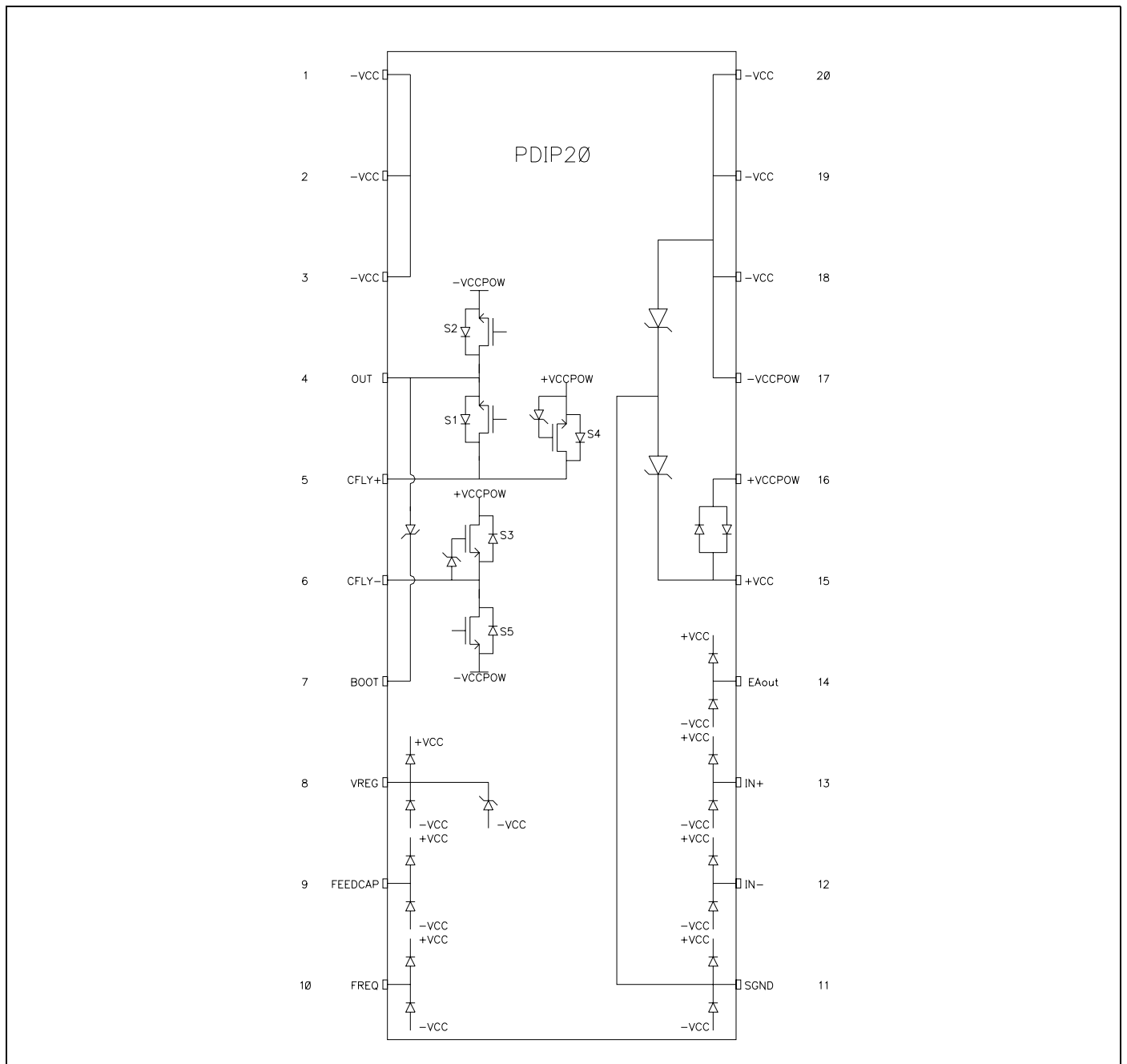


Table 2: DIP20 Package

| Dim. | mm             |      |       | inches |       |       |
|------|----------------|------|-------|--------|-------|-------|
|      | Min.           | Typ. | Max.  | Min.   | Typ.  | Max.  |
| A    |                |      | 5.33  |        |       | 0.210 |
| A1   | 0.38           |      |       | 0.015  |       |       |
| A2   | 2.92           | 3.30 | 4.95  | 0.115  | 0.130 | 0.195 |
| b    | 0.36           | 0.46 | 0.56  | 0.014  | 0.018 | 0.022 |
| b2   | 1.14           | 1.52 | 1.78  | 0.045  | 0.060 | 0.070 |
| c    | 0.20           | 0.25 | 0.36  | 0.008  | 0.010 | 0.014 |
| D    | 24.89          |      | 26.92 | 0.980  |       | 1.060 |
| e    |                | 2.54 |       |        | 0.100 |       |
| E1   | 6.10           | 6.35 | 7.11  | 0.240  | 0.250 | 0.280 |
| L    | 2.92           | 3.30 | 3.81  | 0.115  | 0.130 | 0.150 |
|      | Number of Pins |      |       |        |       |       |
| N    | 20             |      |       |        |       |       |



Figure 8: ESD Protection Structure



## 8 Revision History

Table 3: Summary of Modifications

| Version | Date           | Description |
|---------|----------------|-------------|
| 0.1     | September 2003 | First Draft |

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