Temic
S

TFDU6100E
TFDS6500E
TFDT6500E

2.7–5.5V Fast Infrared Transceiver Module Family (FIR, 4 Mbit/s)

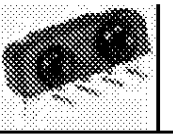
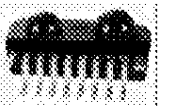
General Description

The TFDU6100E, TFDS6500E and TFDT6500E are a family of low power infrared transceiver modules compliant to the IrDA 1.1 standard for fast infrared (FIR) data communication and supports all IrDA speeds up to 4.0 Mbit/s, HP-SIR, Sharp ASK and carrier based remote control modes up to 2 MHz. Integrated within the transceiver modules are a photo PIN diode, infrared emitter (IRED) and a low power CMOS control IC to provide a total front-end solution in a single package. TEMIC's FIR transceivers are available in three package options including our BabyFace package (TFDU6100E), the smallest FIR transceiver available on the market. This wide selection provides flexibility for a variety of applications and space constraints.

The transceivers are capable to directly interface to a wide variety of I/O chips which perform the pulse width modulation/demodulation function such as the National Semiconductor's PC87338, PC87108 and PC87109, SMSC's FDC37C669, FDC37N769 and CAM35C44, and Hitachi's SH3. At a minimum, a current limiting resistor in series with the infrared emitter and a Vcc bypass capacitor are the only external components required to implement a complete solution.

Features

- Compliant to IrDA 1.1 (up to 4 Mbit/s), HP–SIR, Sharp ASK and TV Remote
- Wide Operating Voltage Range (2.7 to 5.5 V)
- Low Power Consumption (3 mA supply current)
- Power Shutdown Mode (1 µA shutdown current)
- Long Range (up to 2.0 m at 4 Mbit/s in nominal design)
- High Efficiency Emitter (120 mW/sr min ± 15°)
- Three Surface Mount Package Options
  - Universal (9.7 x 4.7 x 4.0 mm)
  - Side View (13.0 x 5.95 x 5.3 mm)
  - Top View (13.0 x 7.6 x 5.95 mm)
- BabyFace (Universal) Package Capable of Surface Mount Solderability to Side and Top View Orientation
- Directly Interfaces with Various Super I/O and controller devices.
- Built-in EMI Protection – no external shielding necessary

Package Options	Part Number	Package
	**TFDU6100E**	**BabyFace (Universal)**
	**TFDS6500E**	**Side View**
	**TFDT6500E**	**Top View**

- Few External Components Required
- Backward Compatible to all TEMIC SIR and FIR Infrared Transceivers

Applications

- Notebook Computers, Desktop PCs, Palmtop Computers (Win CE), PDAs
- Digital Still and Video Cameras
- Printers, Fax Machines, Photocopiers, Screen Projectors
- Telecommunication Products (Cellular Phones, Pagers)
- Internet TV Boxes, Video conferencing systems
- External Infrared Adapters (Dongles)
- Medical and Industrial Data Collection Devices

Functional Block Diagram

PRELIMINARY SPECIFICATION

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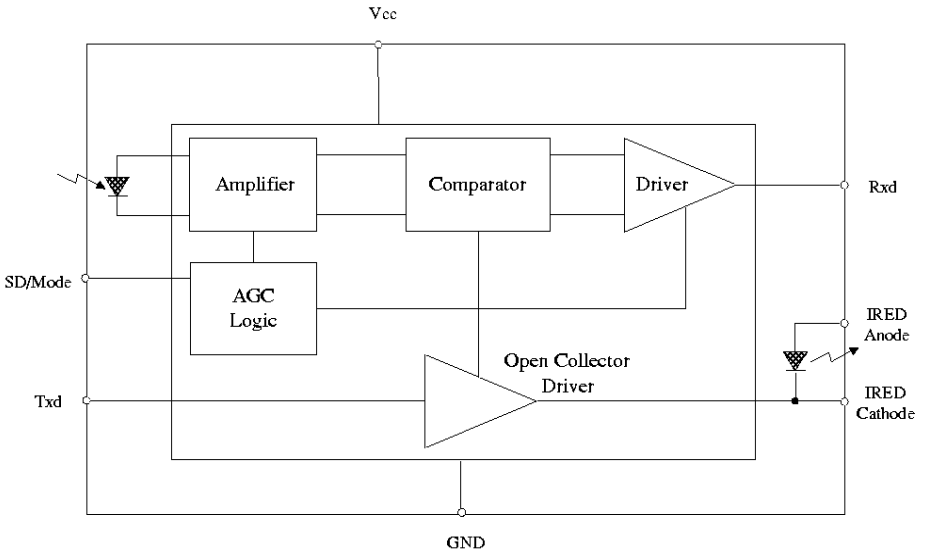
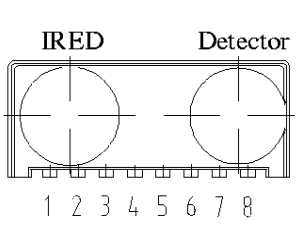
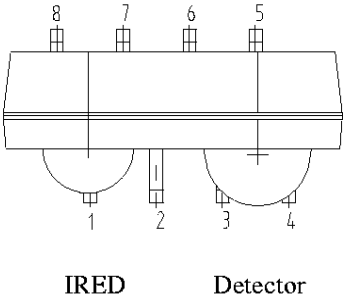


Pin Assignment and Description

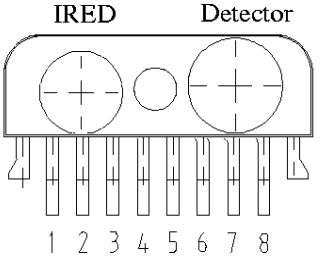
Pin Number		Function	Description	I/O	Active
" U ", " T " Option	" S " Option				
1	8	IRED Anode	IRED anode, should be externally connected to VCC through a current control resistor		
2	1	IRED Cathode	IRED cathode, internally connected to driver transistor		
3	7	Txd	Transmit Data Input	I	HIGH
4	2	Rxd	Received Data Output, push-pull CMOS driver output capable of driving a standard CMOS or TTL load. No external pull-up or pull-down resistor is required.	O	LOW
5	6	SD/Mode	Shut Down/Mode	I	HIGH
6	3	Vcc	Supply Voltage		
7	5	NC	Do not connect		
8	4	GND	Ground		



BabyFace (Universal)



Side View



Top View

Ordering Information

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Part number	Qty/ Reel	Description
TFDU6100E–TR3	1000 pcs	Oriented in carrier tape for side view surface mounting
TFDU6100E–TT3	1000 pcs	Oriented in carrier tape for top view surface mounting
TFDS6500E–TR3	750 pcs	
TFDT6500E–TR3	750 pcs	

Absolute Maximum Ratings

Parameter	Symbol	Test Conditions[a]	Min[b]	Typ[c]	Max[b]	Unit
Supply Voltage Range	V_{cc}		–0.5		6	V
Input Currents[d]					10	mA
Output Sinking Current					25	mA
Power Dissipation[e]	P_D				450	mW
Junction Temperature	T_J				125	°C
Ambient Temperature Range (Operating)	T_{amb}		–25		85	°C
Storage Temperature Range	T_{stg}		–25		85	°C
Soldering Temperature		t = 20 s @215°C		215	240	°C
Average Output Current	I_{IRED} (DC)				130	mA
Repetitive Pulsed Output Current	I_{IRED} (RP)	<90µs, t_{on}<20%			600	mA
IRED Anode Voltage at Current Output	V_{IREDA}		–0.5		6	V
Transmitter Data Input Voltage	V_{Txd}		–0.5		V_{cc} + 0.5	V
Receiver Data Output Voltage	V_{Rxd}		–0.5		V_{cc} + 0.5	V
Virtual Source Size[f]	d		2.5	2.8		mm
Maximum Intensity for Class 1 Operation of IEC 825 or EN60825[g]		EN60825, 1997			320	mW/sr

[a] Reference point ground unless otherwise noted
[b] The algebraic convention whereby the most negative value is a minimum and the most positive a maximum
[c] Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
[d] Maximum input current for all pins
[e] See Derating Curve
[f] Method: (1–1/e) encircled energy
[g] Worst case IrDA SIR pulse pattern, 115.2 kbit/s

Electrical characteristics

Parameter	Symbol	Test Conditions[a]	Min[b]	Typ[c]	Max[b]	Unit
Transceiver						
Supply Voltage	V_{CC}		2.7		5.5	V
Dynamic Supply Current	I_{CC}	SD = Low, E_e = 0 mW/m^2		3	4	mA
Dynamic Supply Current	I_{CC}	SD = Low, E_e = 1 klx[d]		3	4	mA
Standby Supply Current[e]	I_{SD}	SD = High, Mode = floating, 25°C, E_e = 0 klx			1	µA
Standby Supply Current	I_{SD}	SD = High, Mode = floating, T =25°C, E_e = 1 klx[d]			1.5	µA
Standby Supply Current[e]	I_{SD}	SD = High, Mode = floating, T = 85°C			5	µA
Operating Temperature Range	T_A		-25		85	°C
Output Voltage Low	V_{OL}	I_{OL} = 4 mA		0.5	0.8	V
Output Voltage High	V_{OH}	I_{OH} = -4 mA	V_{cc}-0.5			
Input Voltage Low	V_{IL}		0		0.8	V
Input Voltage High[f]	V_{IH}	V_{cc}<4.5V	V_{cc}/2+0.5			V
Input Voltage High[g]	V_{IH}	V_{cc}≥4.5V	V_{cc}/2+0.25			V
Input Leakage Current	I_L		-10		+10	µA
Input Capacitance	C_I				5	pF

[a] T_{amb} = -25 to 85°C, V_{CC} = 2.7 -5.5 V unless otherwise noted.

[b] The algebraic convention whereby the most negative value is a minimum and the most positive a maximum

[c] Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing

[d] Standard illuminant A

[e] Not ambient light sensitive

[f] CMOS levels

[g] TTL levels

Optoelectronic Characteristics

Parameter	Symbol	Test Conditions[a]	Min[b]	Typ[c]	Max[b]	Unit
Receiver						
Minimum Detection Threshold Irradiance	E_e	9.6 kbit/s to 115.2 kbit/s		20	35	mW/m^2
Minimum Detection Threshold Irradiance	E_e	1.152 Mbit/s to 4 Mbit/s		50	80	mW/m^2
Maximum Detection Threshold Irradiance	E_e		5	10		kW/m^2
Logic LOW Receiver Input Irradiance	E_e		4			mW/m^2
Rise Time of Output Signal	t_{RR}	10% to 90%, @2.2 kΩ, 15pF	10		35	ns
Fall Time of Output Signal	t_{FR}	90% to 10%, @2.2 kΩ, 15pF	10		35	ns
Rx Pulse Width of Output Signal, 50%	P_w	Input pulse length 20 µs, 9.6 kbit/s	1.2	10	20	µs
Rx Pulse Width of Output Signal, 50%	P_w	Input pulse length 1.41µs, 115.2 kbit/s mode	1.2		2.2	µs
Rx Pulse Width of Output Signal, 50%	P_w	Input pulse length 217 ns, 115.2 kbit/s mode	190		260	ns
Rx Pulse Width of Output Signal, 50%	P_w	Input pulse length 125 ns, 4.0 Mbit/s	90		160	ns
Rx Pulse Width of Output Signal, 50%	P_w	Input pulse length 250 ns, 4.0 Mbit/s	210		290	ns
Jitter, Leading Edge		Input Irradiance = 90 mW/m^2, 4.0 Mbit/s mode			10	ns
Latency	t_L				120	µs
Transmitter						
Output Radiant Intensity [d]	I_e	Txd = High, SD = Low, R_L= 5.6 Ω	120	140	280	mW/sr
Output Radiant Intensity Half Angle	α			±24		°
Output Radiant Intensity[d]	I_e	Txd = Low or SD = High[e], R_L=5.6 Ω			.04	mW/sr
Peak Wavelength	λ_P		880		900	nm
Voltage drop at output driver		I_F = 600 mA, pulse length 2 µs, duty cycle 25%		400	800	mV
Rise Time, Fall Time	t_R, t_F		10		40	ns
Optical Overshoot					25	%

[a] Tamb = –25 to 85°C, V_{CC} = 2.7 –5.5 V unless otherwise noted.

[b] The algebraic convention whereby the most negative value is a minimum and the most positive a maximum

[c] Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing

[d] V_{cc} = 5V, α = 0°, 15°

[e] Receiver is inactive as long as SD = High

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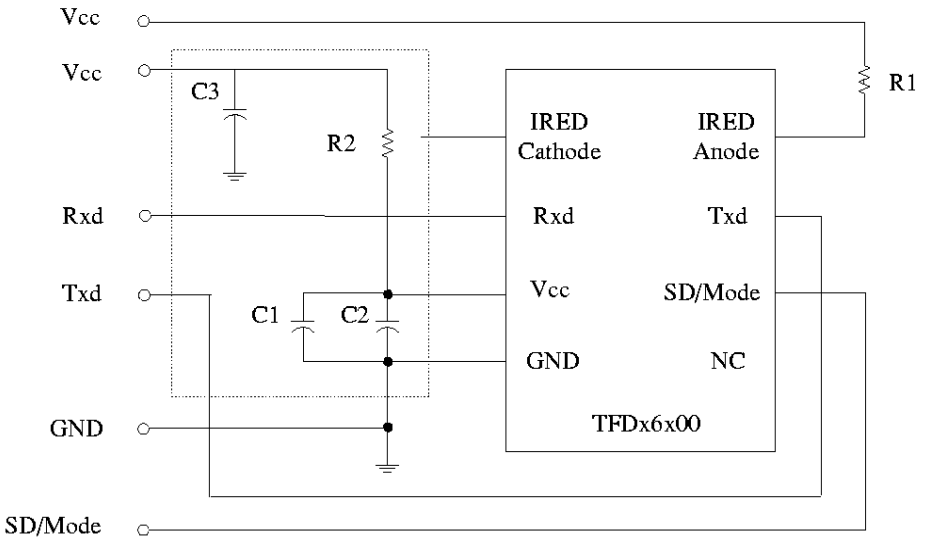
Recommended Circuit Diagram

The only required components for designing an IrDA 1.1 compatible design using TEMIC FIR transceivers are a current limiting resistor, R_1, to the IRED. However, depending on the entire system design and board layout, additional components may be required (see Figure 1).

TEMIC FIR transceivers integrate a sensitive receiver and a built-in power driver. The combination of both needs a careful circuit board layout. The use of thin, long resistive and inductive wiring should be avoided. A board layout identical or similar to the circuit in Fig 1 below is recommended. The inputs (Txd, SD/Mode) and the output Rxd should be directly (DC) coupled to the I/O circuit. Capacitive coupling is not necessary and should be avoided. TEMIC FIR transceivers will automatically switch off the output if input is kept active longer than approximately 60 µs. Also, care should be taken to avoid exceeding specified voltage ratings at the Txd and SD/Mode pins.



note: outlined components are optional depending on quality of power supply

Figure 1

R1 is used for controlling the current through the IR emitter. For increasing the output power of the IRED, the value of the resistor should be reduced. Similarly, to reduce the output power of the IRED, the value of the transceiver should be increased. For typical values of R1 see Figure 2 . For IrDA compliant operation, a current control resistor of 4.7 – 5.2 Ω is recommended. The upper drive current limitation is dependent on the duty cycle and is given by the absolute maximum ratings on the data sheet.

R2, C1, C2 and C3 are optional and dependent on the quality of the supply voltage V_{cc} and injected noise. An unstable power supply with dropping voltage during transmission may reduce sensitivity (and transmission range) of the transceiver.

Recommended Circuit Diagram (continued)

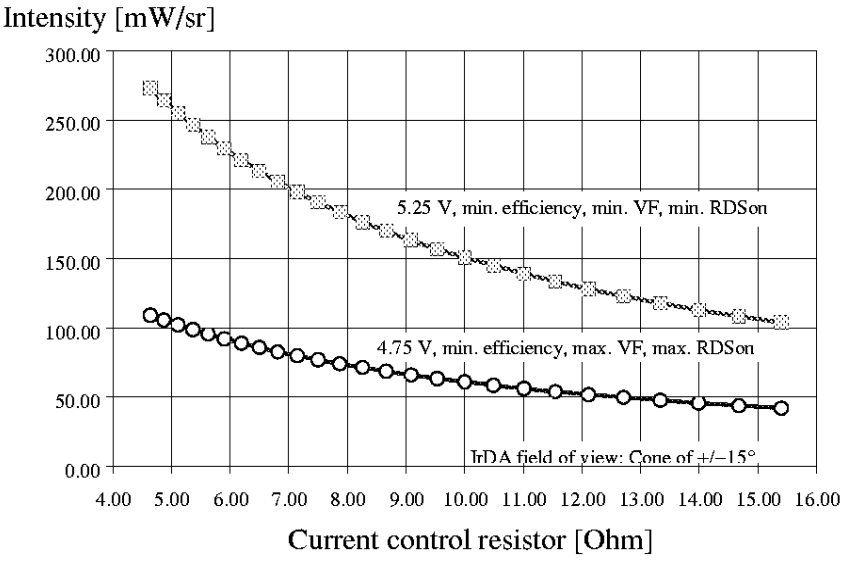


Figure 2

The placement of these parts is critical. It is strongly recommended to position the ceramic capacitor C2 and C3 as near as possible to the transceiver power supply pins as in the proposed layout in Figure 1. A tantalum capacitor should be used for C1 while less expensive ceramic capacitors for C2 and C3. Also, when connecting the described circuit to the power supply, low impedance wiring should be used.

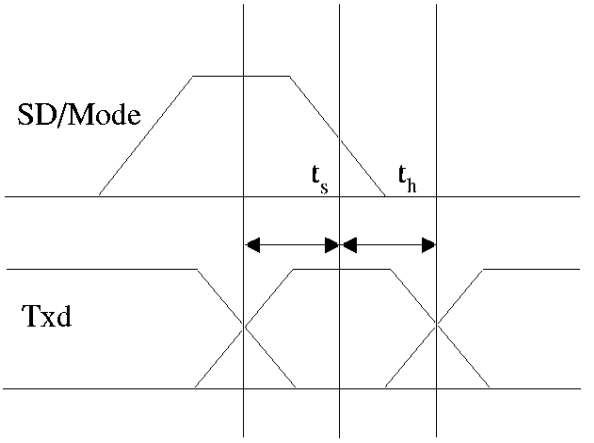
Recommended Application Circuit Components

Component	Recommended Value
C1	0.47 µf, Ceramic
C2	0.1 µf, Ceramic
C3	6.8 –10 µF, Tantalum
R1	4.7 –5.6 Ω, 0.25 W (recommend using two 0.125 W resistors in parallel)
R2	22 –47 Ω, 0.125 W

Mode Switching

The TFDU6100E, TFDS6500E and TFDT6500E powers on in a no default mode, therefore the data transfer rate has to be set by a programming sequence as described below or selected by setting the mode pin. When using the Mode pin, the standby current might be increased to about 50 to 60 µA. In standby mode, the mode input should float to minimize standby current.

The low frequency mode covers speeds up to 115.2 kbit/s. Signals with higher data rates should be detected in the high frequency mode. Lower data frequency data can also received in high frequency mode with reduced sensitivity. To switch the transceivers from low frequency mode to the 4.0 Mbit/s mode and vice versa, the programming sequences described below are required.



Timing Diagram

Setting to the High Bandwidth Mode (0.576 to 4.0 Mbit/s)

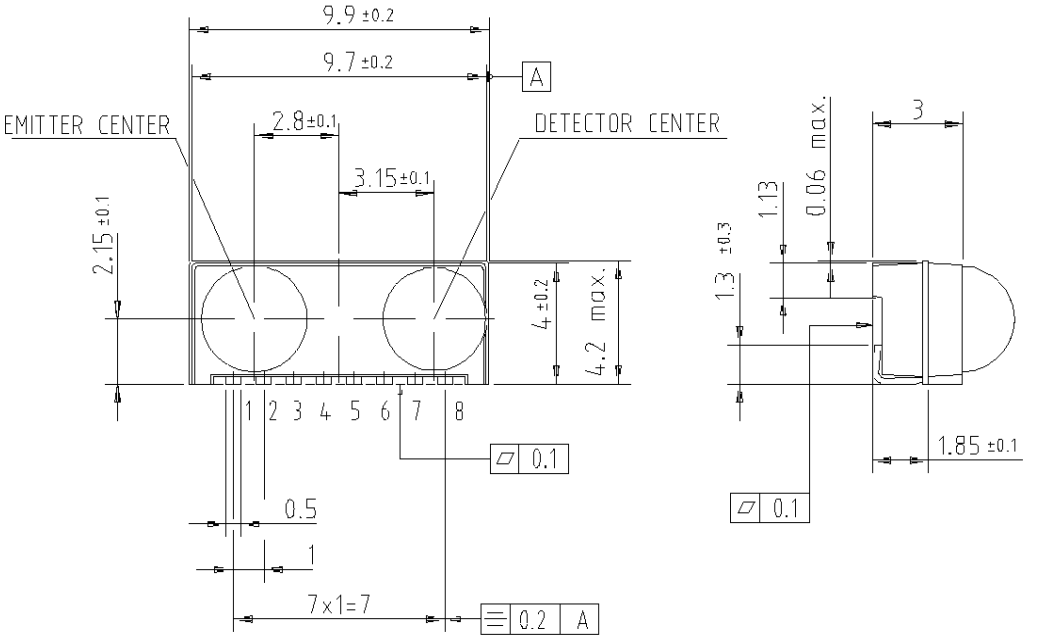
1. Set SD/MODE input to logic "HIGH".
2. Set Txd input to logic "HIGH". Wait $t_s \geq 200$ ns
3. Set SD/MODE to logic "LOW" (This negative edge latches state of Txd, which determines speed setting).
4. After waiting $t_h \geq 200$ ns Txd is to set to logic "LOW". The hold time of Txd is limited by the maximum allowed pulse length.
   Txd is now enabled as normal Txd input for the high bandwidth mode.

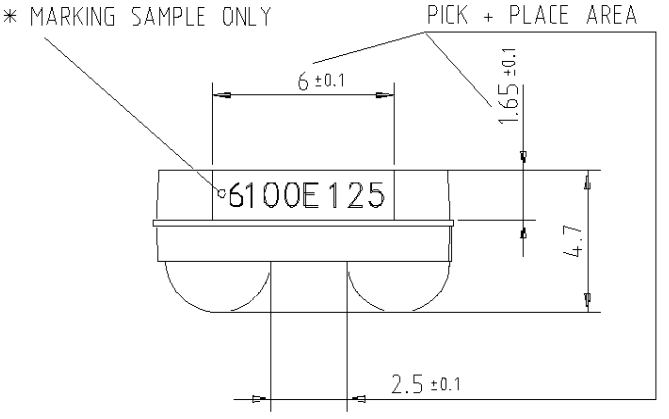
Setting to the Lower Bandwidth Mode (2.4 to 115.2 kbit/s)

1. Set SD/MODE input to logic "HIGH".
2. Set Txd input to logic "LOW". Wait $t_s \geq 200$ ns
3. Set SD/MODE to logic "LOW" (This negative edge latches state of Txd, which determines speed setting).
4. Txd must be held for $t_h \geq 200$ ns.
   Txd is now enabled as normal Txd input for the lower bandwidth mode.

Mechanical Dimensions

TFDU6100E – BabyFace (Universal) Package





* MARKING ORIENTATION
180 DEGREES ALLOWED

technical drawings
according to DIN
specifications

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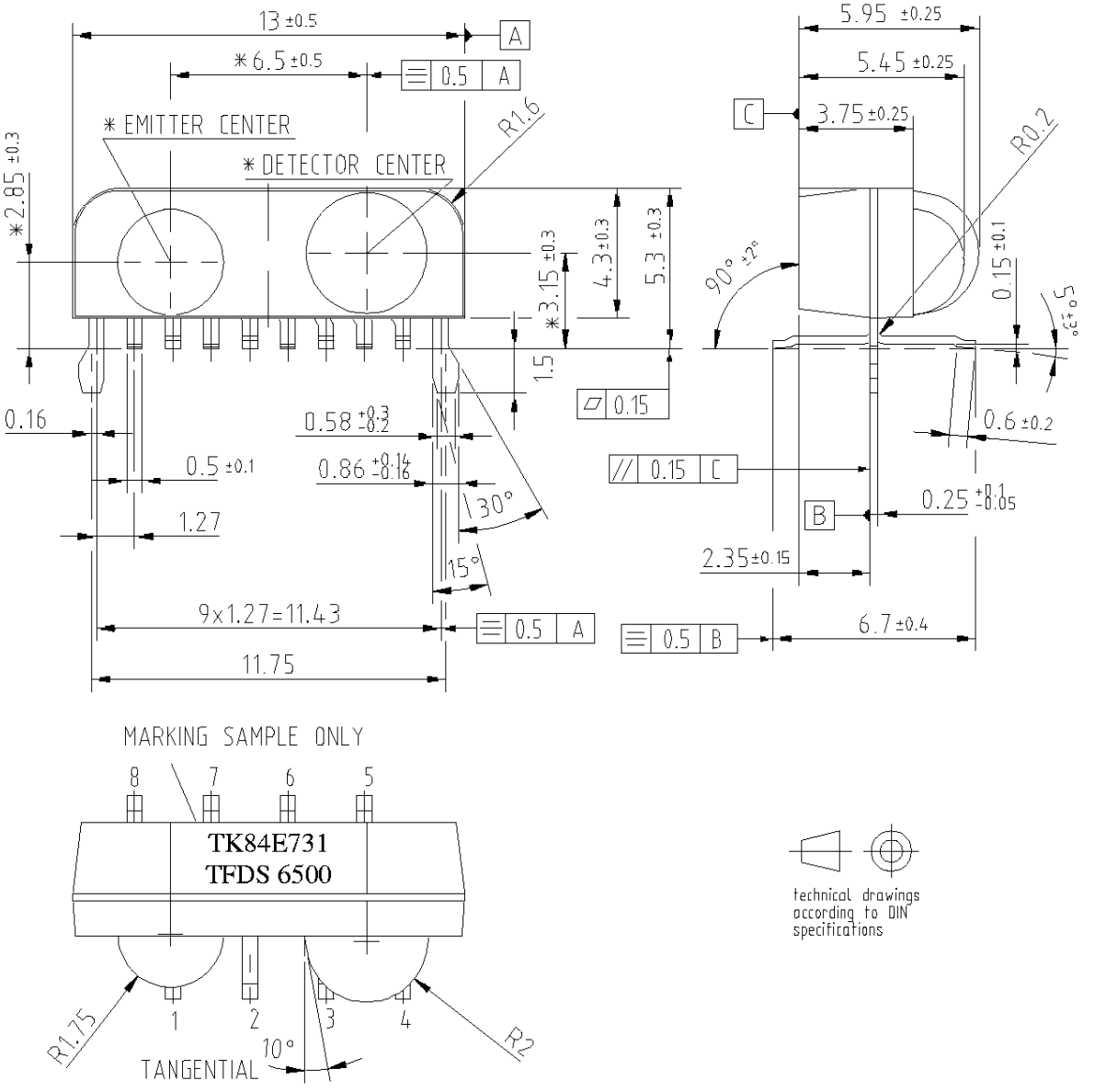
Mechanical Dimensions

TFDS6500E –Side View Package



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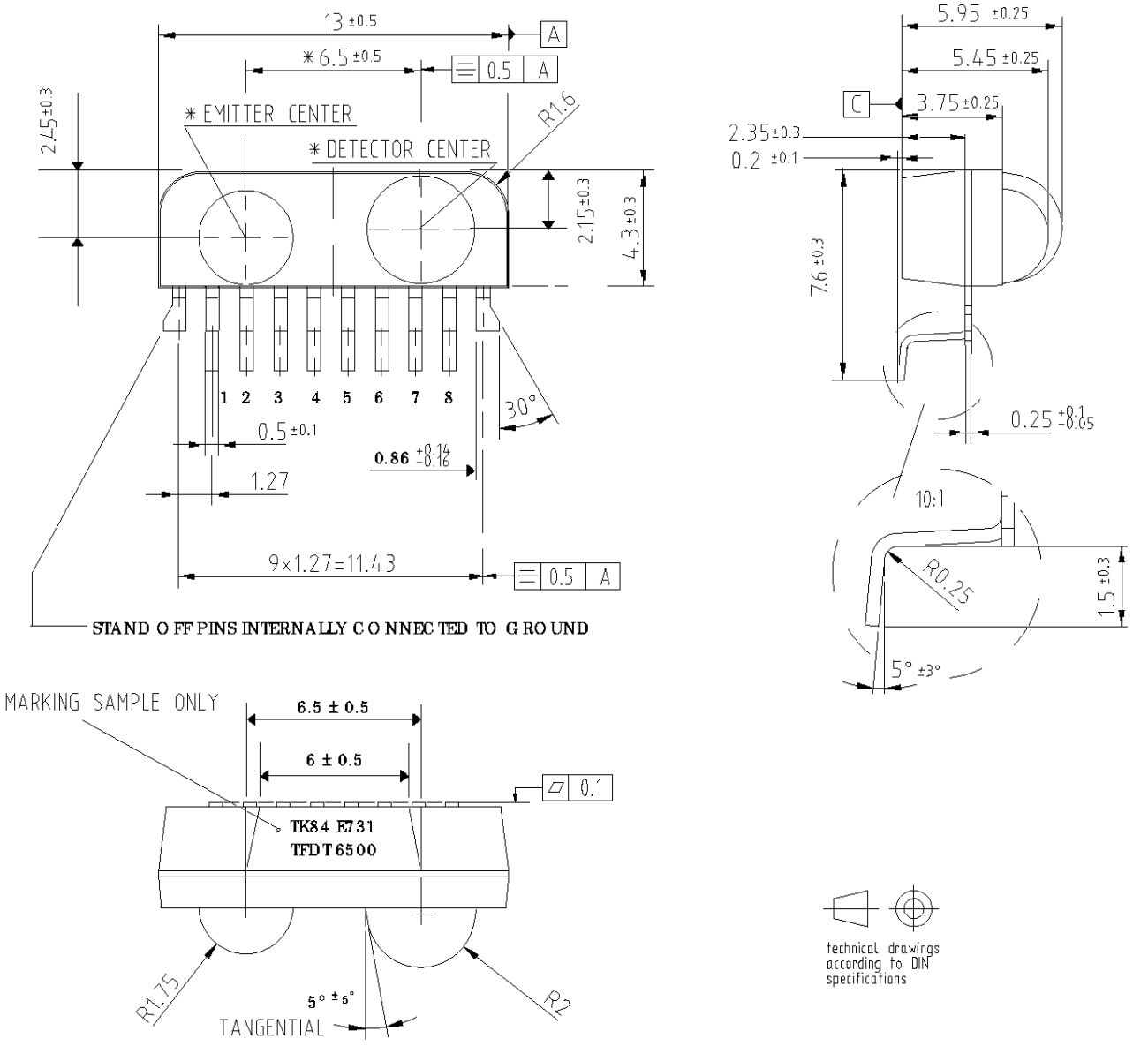
Mechanical Dimensions

TFDT6500E –Top View Package



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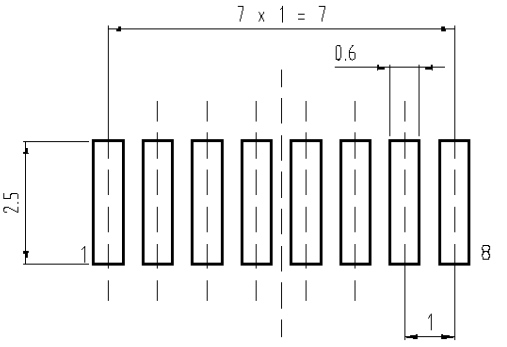
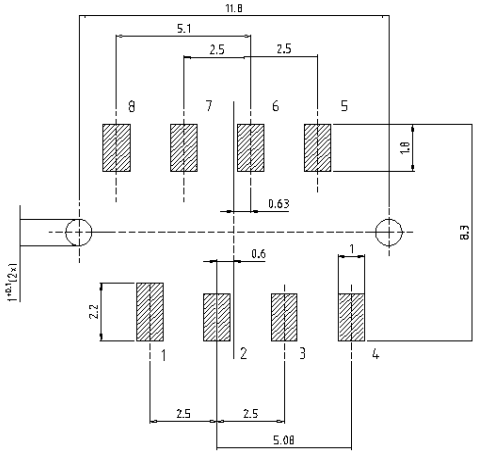
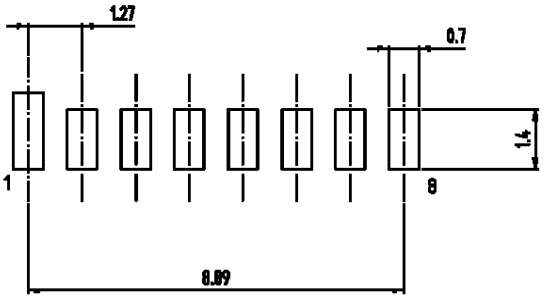
Recommended SMD Pad Layout
(note: device should be soldered in the center position)



TFDU6100E –BabyFace (Universal) Package



TFDS6500E –Side View Package



TFDT6500E –Top View Package

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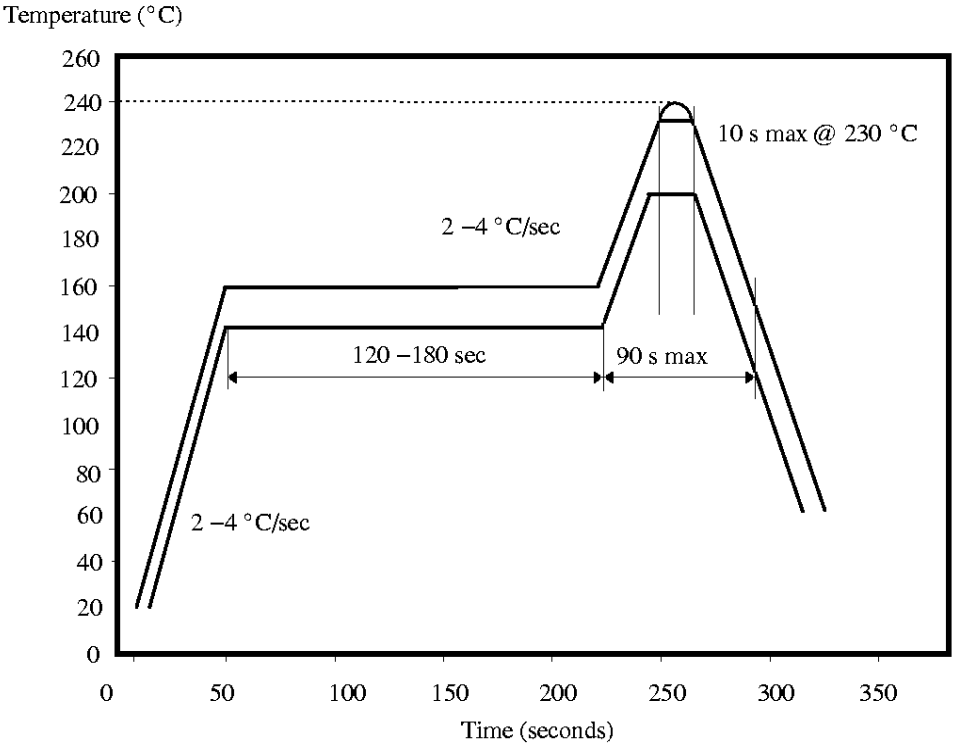
Recommended Solder Profile



Current Derating Curve