# 150-mA Ultra Low-Noise LDO Regulator With Error Flag and Discharge

## FEATURES

- Ultra Low Dropout—130 mV at 150-mA Load
- Low Noise—75 $\mu V_{(rms)}$ (10-Hz to 100-kHz Bandwidth)
- Out−of−Regulation Error Flag (power good)
- Shutdown Control
- 110-µA Ground Current at 150-mA Load
- 1.5% Guaranteed Output Voltage Accuracy
- 300-mA Peak Output Current Capability
- Uses Low ESR Ceramic Capacitors
- Fast Start-Up (50 µs)
- Fast Line and Load Transient Response (≤ 30 µs)
- 1-µA Maximum Shutdown Current
- Output Current Limit
- Reverse Battery Protection
- Built-in Short Circuit and Thermal Protection
- Output, Auto-Discharge In Shutdown Mode
- Fixed 1.2, 1.8, 2.0, 2.2, 2.5, 2.6, 2.7, 2.8, 2.85, 2.9, 3.0, 3.3, 3.5, 3.6, 5.0-V Output Voltage Options
- SC70-5 Package

Product Is Completely Pb-free

## APPLICATIONS

- Cellular Phones, Wireless Handsets
- Noise-Sensitive Electronic Systems, Laptop and Palmtop Computers
- PDAs
- Pagers
- Digital Cameras
- MP3 Player
- Wireless Modem

## DESCRIPTION

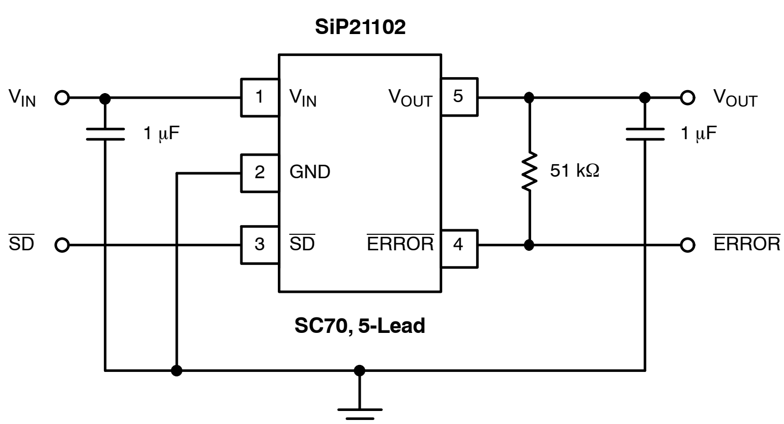
The SiP21102 is a 150-mA CMOS LDO (low dropout) voltage regulator. It is the perfect choice for low voltage, low power applications. An ultra low ground current makes this part attractive for battery operated power systems. The SiP21102 also offers ultra low dropout voltage to prolong battery life in portable electronics. Systems requiring a quiet voltage source, will benefit from the SiP21102's low output noise. The SiP21102 is designed to maintain regulation while delivering 300-mA peak current, making it ideal for systems that have a high surge current upon turn-on.

For better transient response and regulation, an active pull-down circuit is built into the SiP21102 to clamp the output voltage when it rises beyond normal regulation. The SiP21102 automatically discharges the output voltage by connecting the output to ground through a 100-Ω n-channel MOSFET when the device is put in shutdown mode.

The SiP21102 features reverse battery protection to limit reverse current flow to approximately 1-µA in the event reversed battery is applied at the input, thus preventing damage to the IC.

The SiP21102 is available in a lead (Pb)-free 5-pin SC70 package for operation over the industrial operating range (−40 °C to 85 °C).

## TYPICAL APPLICATION CIRCUIT



## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings
Input Voltage, $V_{IN}$ to GND . . . . . . . . . . –6.0 to 6.5 V
$V_{\overline{SD}}$ (See Detailed Description) . . . . . . . . . . –0.3 V to $V_{IN}$
Output Current, $I_{OUT}$ . . . . . . . . . . Short Circuit Protected
Output Voltage, $V_{OUT}$ . . . . . . . . . . –0.3 V to $V_{IN}$ + 0.3 V
Package Power Dissipation, $(P_d)$[b] . . . . . . . . . . 384 mW

Package Thermal Resistance, $(\theta_{JA})$[a] . . . . . . . . . . 207°C/W
Maximum Junction Temperature, $T_{J(max)}$ . . . . . . . . . . 150°C
Storage Temperature, $T_{STG}$ . . . . . . . . . . –65°C to 150°C

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 4.8 mW/°C above $T_A$ = 70°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## RECOMMENDED OPERATING RANGE

Input Voltage, $V_{IN}$ . . . . . . . . . . 2 V to 6 V
Input Voltage, $V_{\overline{SD}}$ . . . . . . . . . . 0 V to $V_{IN}$
*$C_{IN}$ = $C_{OUT}$ = 1 µF (ceramic), $C_{BP}$ = 0.01 µF (ceramic)*
*Maximum ESR of $C_{OUT}$: 0.4 Ω*

Operating Ambient Temperature, $T_A$ . . . . . . . . . . –40°C to 85°C

## SPECIFICATIONS

| Parameter | Symbol | Test Conditions Unless Specified: $T_A$ = 25°C, $V_{IN}$ = $V_{OUT(nom)}$ + 1 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 1 µF, $C_{OUT}$ = 1.0 µF, $V_{\overline{SD}}$ = 1.5 V | Temp[a] | Limits –40 to 85°C Min[b] | Typ[c] | Max[b] | Unit |
|---|---|---|---|---|---|---|---|
| Start-Up BP Current | $I_{OUT}$ | ON/$\overline{OFF}$ = High | Room | | 1 | | mA |
| Input Voltage Range | $V_{IN}$ | | Full | 2 | | 6 | V |
| Output Voltage Accuracy | $V_{OUT}$ | 1 mA ≤ $I_{OUT}$ ≤ 150 mA | Room | –1.5 | 1 | 1.5 | % |
| | | | Full | –2.5 | 1 | 2.5 | |
| Line Regulation ($V_{OUT}$ ≤ 3 V) | $\frac{\Delta V_{OUT} \times 100}{\Delta V_{IN} \times V_{OUT(nom)}}$ | From $V_{IN}$ = $V_{OUT(nom)}$ + 1 V to $V_{OUT(nom)}$ + 2 V | Full | –0.06 | | 0.18 | %/V |
| Line Regulation (3.0 V < $V_{OUT}$ ≤ 3.6 V) | | | Full | 0 | | 0.3 | |
| Line Regulation (5-V Version) | | From $V_{IN}$ = 5.5 V to 6 V | Full | 0 | | 0.4 | |
| Dropout Voltage[d, g] ($V_{OUT(nom)}$ ≥ 2.6 V) | $V_{IN} - V_{OUT}$ | $I_{OUT}$ = 1 mA | Room | | 1 | | mV |
| | | $I_{OUT}$ = 50 mA | Room | | 45 | 80 | |
| | | | Full | | 50 | 90 | |
| | | $I_{OUT}$ = 150 mA | Room | | 130 | 180 | |
| | | | Full | | | 220 | |
| Dropout Voltage[d, g] ($V_{OUT(nom)}$ < 2.6 V, $V_{IN}$ ≥ 2 V) | | $I_{OUT}$ = 50 mA | Room | | 65 | 100 | |
| | | | Full | | | 120 | |
| | | $I_{OUT}$ = 150 mA | Room | | 190 | 250 | |
| | | | Full | | | 300 | |
| Ground Pin Current[e, g] ($V_{OUT(nom)}$ ≤ 3 V) | $I_{GND}$ | $I_{OUT}$ = 0 mA | Room | | 100 | 150 | µA |
| | | | Full | | | 180 | |
| | | $I_{OUT}$ = 150 mA | Room | | 110 | 200 | |
| | | | Full | | | 230 | |
| Ground Pin Current[e] ($V_{OUT(nom)}$ > 3 V) | | $I_{OUT}$ = 0 mA | Room | | 110 | 170 | |
| | | | Full | | | 200 | |
| | | $I_{OUT}$ = 150 mA | Room | | 120 | 200 | |
| | | | Full | | | 230 | |
| Peak Output current | $I_{O(peak)}$ | $V_{OUT}$ ≥ 0.95 x $V_{OUT(nom)}$, $t_{PW}$ = 2 ms | Full | 300 | | | mA |
| Ripple Rejection | $\Delta V_{OUT}/\Delta V_{IN}$ | $I_{OUT}$ = 150 mA, f = 1 kHz | Room | | 60 | | dB |
| | | f = 10 kHz | Room | | 40 | | |
| | | f = 100 kHz | Room | | 30 | | |

## SPECIFICATIONS

| Parameter | Symbol | Test Conditions Unless Specified<br>$T_A$ = 25°C, $V_{IN}$ = $V_{OUT(nom)}$ + 1 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 1 µF, $C_{OUT}$ = 1.0 µF, $V_{\overline{SD}}$ = 1.5 V | Temp[a] | Limits −40 to 85°C Min[b] | Typ[c] | Max[b] | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| Dynamic Line Regulation | $\Delta V_{O(line)}$ | $V_{IN}$ : $V_{OUT(nom)}$ + 1 V to $V_{OUT(nom)}$ + 2 V<br>$t_r/t_f$ = 2 µs, $I_{OUT}$ = 150 mA | Room | | 20 | | mV |
| Dynamic Load Regulation | $\Delta V_{O(load)}$ | $I_{OUT}$ : 1 mA to 150 mA, $t_r/t_f$ = 2 µs | Room | | 20 | | mV |
| Thermal Shutdown Junction Temperature | $T_{J(S/D)}$ | | Room | | 150 | | °C |
| Thermal Hysteresis | $T_{HYST}$ | | Room | | 20 | | °C |
| Reverse current | $I_R$ | $V_{IN}$ = −6.0 V | Room | | 1 | | µA |
| Short Circuit Current | $I_{SC}$ | $V_{OUT}$ = 0 V | Room | | 700 | | mA |
| **Shutdown** | | | | | | | |
| Shutdown Supply Current | $I_{CC(off)}$ | $V_{\overline{SD}}$ = 0 V | Room | | 0.1 | 1 | µA |
| $\overline{SD}$ Pin Input Voltage | $V_{\overline{SD}}$ | High = Regulator ON (Rising) | Full | 1.5 | | $V_{IN}$ | V |
| | | Low = Regulator OFF (Falling) | Full | | | 0.4 | V |
| Auto Discharge Resistance | R_DIS | SiP21102Only | Room | | 100 | | Ω |
| $\overline{SD}$ Pin Input Current[f] | $I_{IN(\overline{SD})}$ | $V_{\overline{SD}}$ = 1.5 V, $V_{IN}$ = 6 V | Room | | 0.7 | | µA |
| $\overline{SD}$ Hysteresis | $V_{HYST(\overline{SD})}$ | | Full | | 150 | | mV |
| $V_{OUT}$ Turn-On Time | $t_{ON}$ | $V_{\overline{SD}}$ (See Figure 1), $I_{LOAD}$ = 100 nA | | | 50 | | µS |
| **ERROR Output** | | | | | | | |
| $\overline{ERROR}$ High Leakage | $I_{OFF}$ | $\overline{ERROR}$ ≤ $V_{IN}$. $V_{OUT}$ in Regulation | Full | | | 1 | µA |
| $\overline{ERROR}$ Low Voltage | $V_{OL}$ | $I_{SINK}$ = 0.5 mA | Full | | | 0.4 | V |
| $\overline{ERROR}$ Voltage Threshold | $V_{\overline{ERROR}}$ | $V_{OUT}$ Below $V_{OUT(nom)}$[g], $V_{IN}$ ≥ 2 V<br>$V_{OUT}$ Falling, $I_{OUT}$ = 1 mA, $V_{OUT(nom)}$ ≥ 2 V | Full | −2 | −4 | −6 | % |
| | | $V_{OUT(nom)}$[g] < 2 V, $V_{IN}$ > 2 V | Full | | −4 | | % |
| $\overline{ERROR}$ Voltage Threshold Hysteresis | $V_{HYST(\overline{ERROR})}$ | | Room | | 1.5 | | % |

Notes
a. Room = 25°C, Full = −40 to 85°C.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing. Typical values for dropout voltage at $V_{OUT}$ ≥ 2 V are measured at $V_{OUT}$ = 3.3 V, while typical values for dropout voltage at $V_{OUT}$ < 2 V are measured at $V_{OUT}$ = 1.8 V.
d. Dropout voltage is defined as the input to output differential voltage at which the output voltage drops 2% below the output voltage measured with a 1-V differential, provided that $V_{IN}$ does not not drop below 2.0 V.
e. Ground current is specified for normal operation as well as “drop-out” operation.
f. The device’s shutdown pin includes a typical 2-MΩ internal pull-down resistor connected to ground.
g. $V_{OUT(nom)}$ is $V_{OUT}$ when measured with a 1-V differential to $V_{IN.}$

## TIMING WAVEFORMS

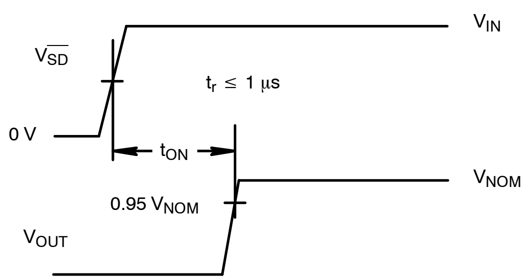
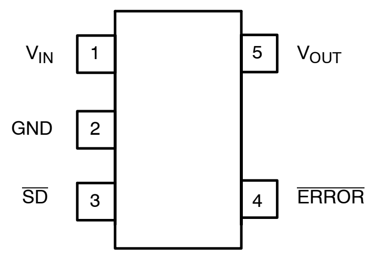



**FIGURE 1.** Timing Diagram for Power-Up

## PIN CONFIGURATION

**SC70, 5-Lead**




## PIN DESCRIPTION

| Pin Number | Name | Function |
|---|---|---|
| 1 | $V_{IN}$ | Input supply pin. Bypass this pin with a 1-μF ceramic or tantalum capacitor to ground |
| 2 | GND | Ground pin. For better thermal capability, directly connected to large ground plane |
| 3 | $\overline{SD}$ | By applying less than 0.4 V to this pin, the device will be turned off. Connect this pin to $V_{IN}$ if unused |
| 4 | $\overline{ERROR}$ | The open drain output is an error flag output which goes low when $V_{OUT}$ drops 4% below its nominal voltage. |
| 5 | $V_{OUT}$ | Output voltage. Connect $C_{OUT}$ between this pin and ground. |

## ORDERING INFORMATION

| Part Number | Marking | Voltage | Temp. Range | Pkg. |
|---|---|---|---|---|
| SiP21102DR-12-E3 | Y0LL | 1.2 | | |
| SiP21102DR-18-E3 | E0LL | 1.8 | | |
| SiP21102DR-20-E3 | E1LL | 2.0 | | |
| SiP21102DR-22-E3 | E2LL | 2.2 | | |
| SiP21102DR-25-E3 | E3LL | 2.5 | | |
| SiP21102DR-26-E3 | E4LL | 2.6 | | |
| SiP21102DR-27-E3 | E5LL | 2.7 | | |
| SiP21102DR-28-E3 | E6LL | 2.8 | –40 to 85°C | SC70-5 |
| SiP21102DR-285-E3 | E7LL | 2.85 | | |
| SiP21102DR-29-E3 | E8LL | 2.9 | | |
| SiP21102DR-30-E3 | E9LL | 3.0 | | |
| SiP21102DR-33-E3 | F0LL | 3.3 | | |
| SiP21102DR-35-E3 | F1LL | 3.5 | | |
| SiP21102DR-36-E3 | F2LL | 3.6 | | |
| SiP21102DR-50-E3 | F3LL | 5.0 | | |

Note: LL = Lot Code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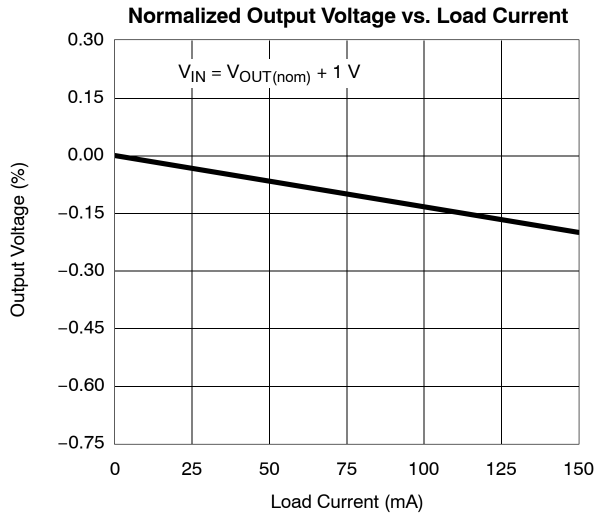
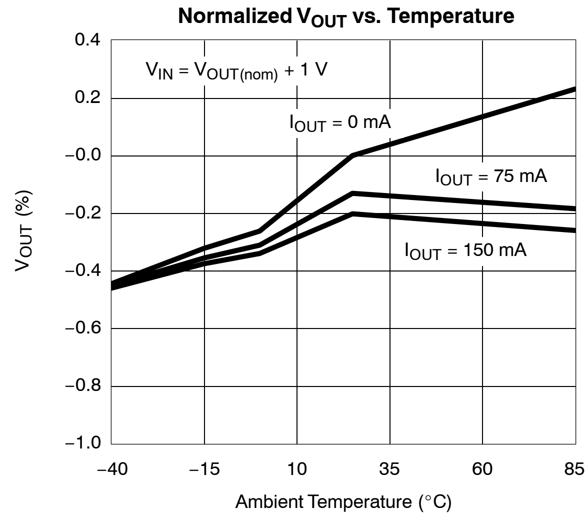
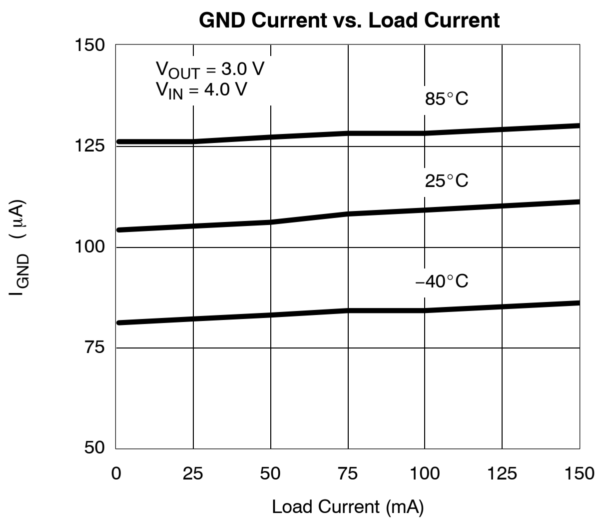
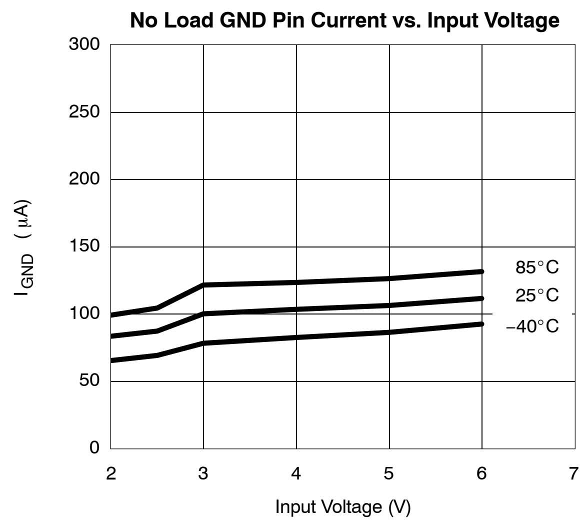
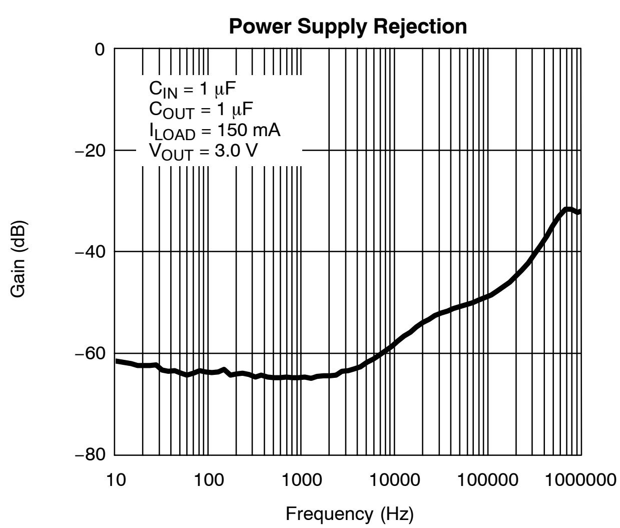
## TYPICAL CHARACTERISTICS (INTERNALLY REGULATED, 25°C UNLESS NOTED)

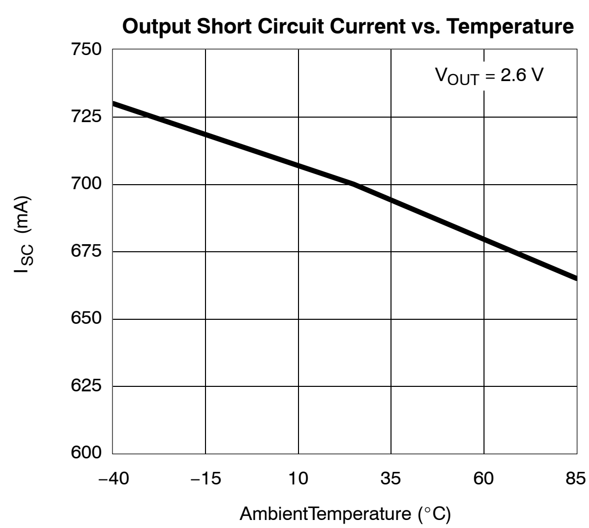


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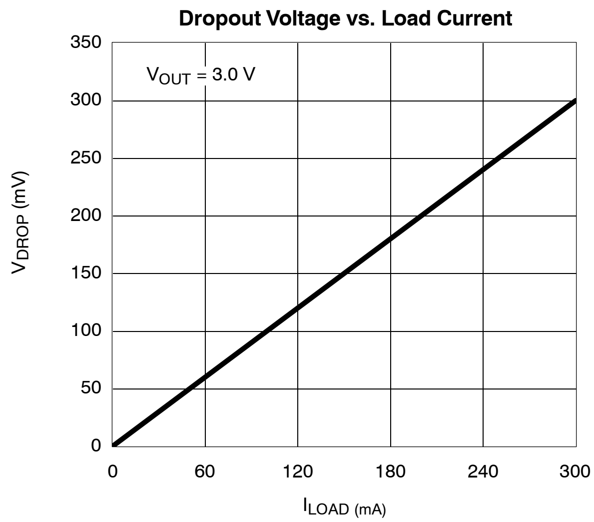
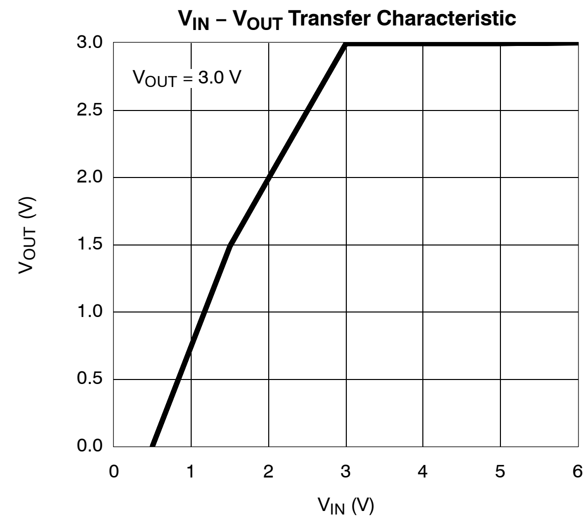
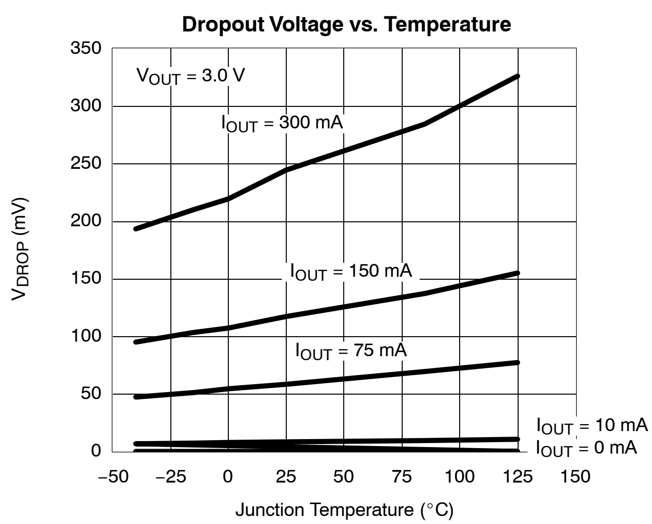
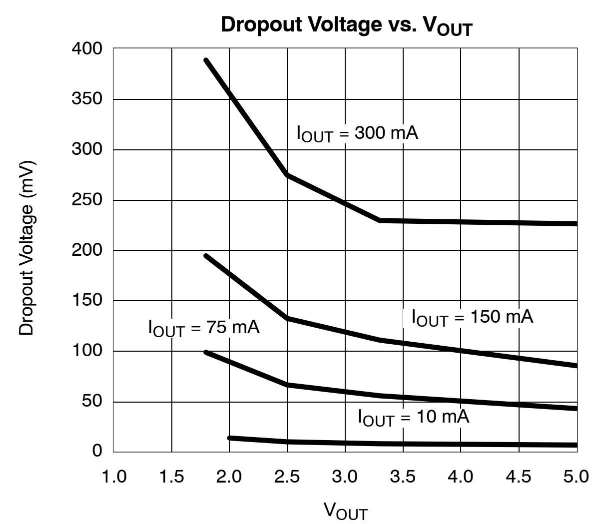


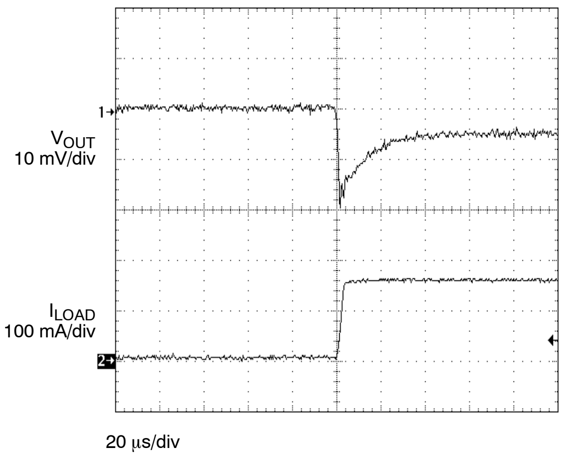



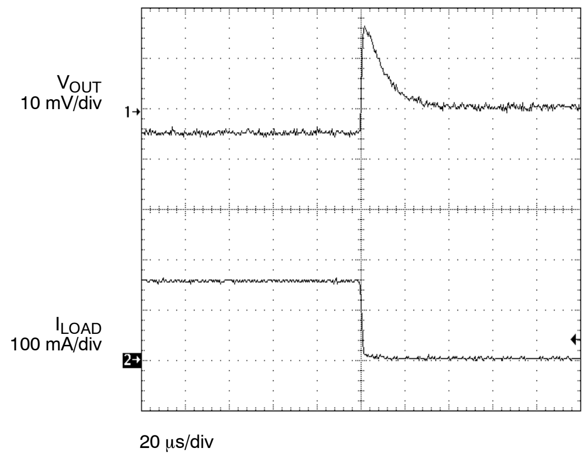
## TYPICAL WAVEFORMS

**Load Transient Response-1**



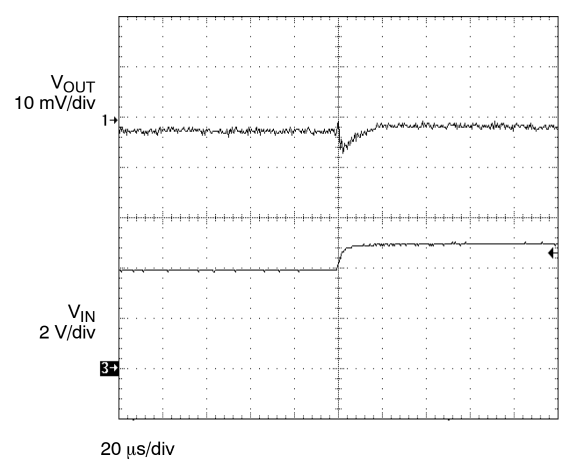

$V_{OUT}$ = 3.0 V
$C_{OUT}$ = 1 µF
$I_{LOAD}$ = 1 to 150 mA
$t_{rise}$ = 2 µsec

**Load Transient Response-2**



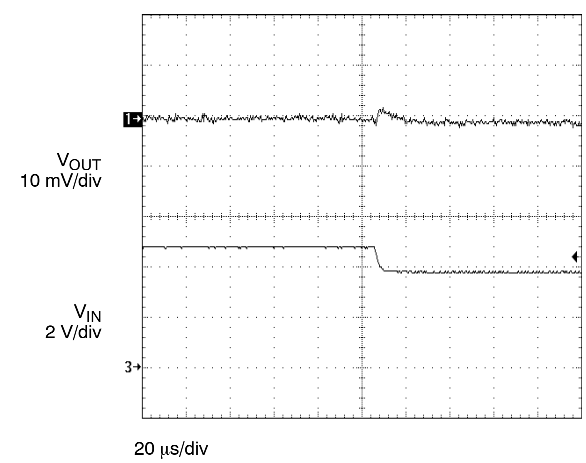

$V_{OUT}$ = 3.0 V
$C_{OUT}$ = 1 µF
$I_{LOAD}$ = 150 to 1 mA
$t_{fall}$ = 2 µsec

**LineTransient Response-1**




$V_{INSTEP}$ = 4 to 5 V
$V_{OUT}$ = 3 V
$C_{OUT}$ = 1 µF
$C_{IN}$ = 1 µF
$I_{LOAD}$ = 150 mA
$t_{rise}$ = 5 µsec

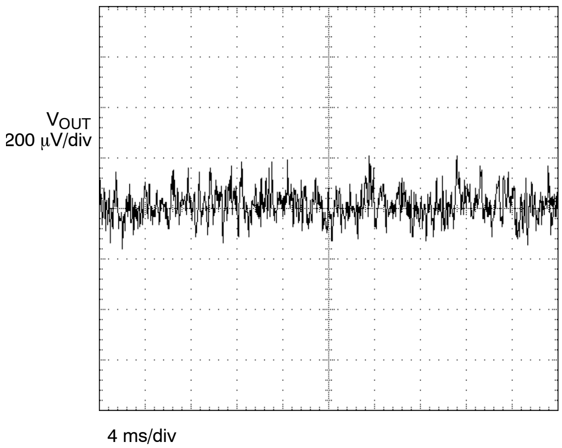
**LineTransient Respons-2**




$V_{INSTEP}$ = 5 to 4 V
$V_{OUT}$ = 3 V
$C_{OUT}$ = 1 µF
$C_{IN}$ = 1 µF
$I_{LOAD}$ = 150 mA
$t_{fall}$ = 5 µsec

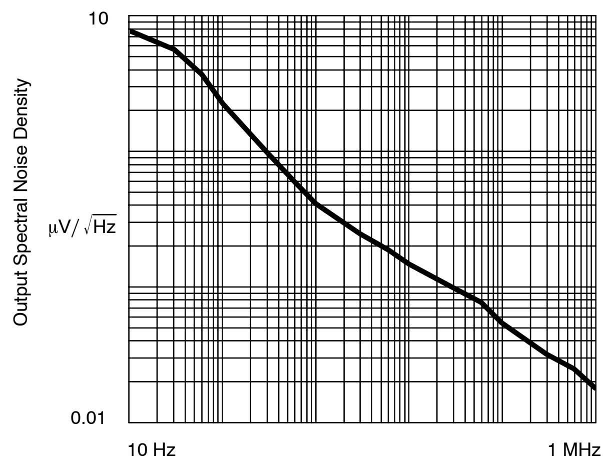
## TYPICAL WAVEFORMS

**Output Noise**



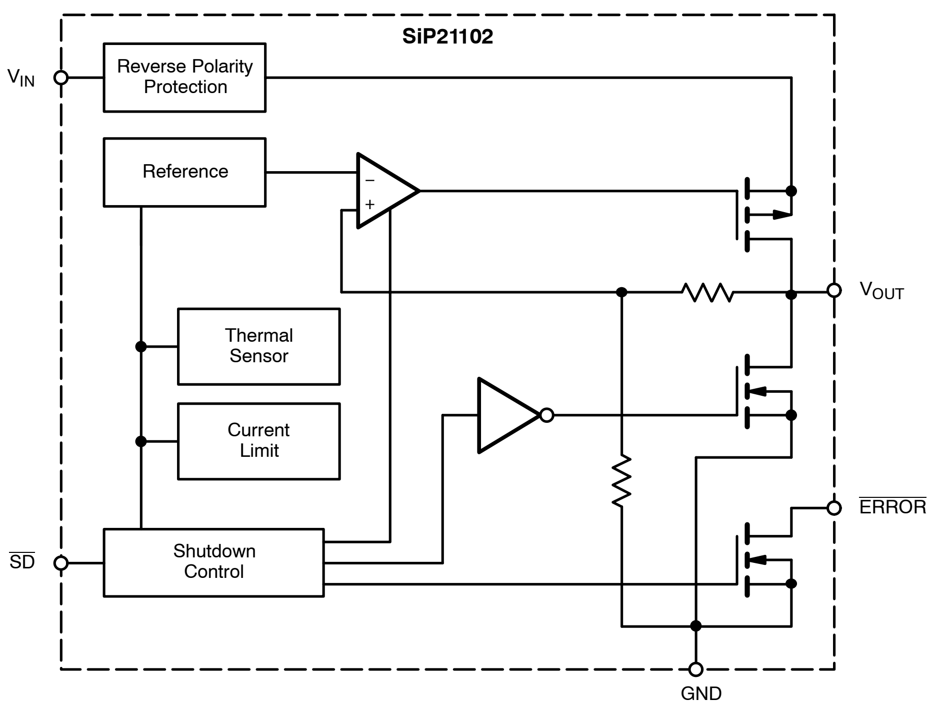

$V_{IN}$ = 4 V
$V_{OUT}$ = 3 V
$I_{OUT}$ = 150 mA
BW = 10 Hz to 100 kHz

**Noise Spectrum**




$V_{IN}$ = 4 V
$V_{OUT}$ = 3 V
$I_{LOAD}$ = 150 mA

## BLOCK DIAGRAM



## DETAILED DESCRIPTION

The SiP21102 is a low-noise, low drop-out and low quiescent current linear voltage regulator, packaged in a small footprint SC70-5 package. The SiP21102 can supply loads up to 300 mA. As shown in the block diagram, the circuit consists of a bandgap reference error, amplifier, p-channel pass transistor and feedback resistor string. An external bypass capacitor connected to the BP pin reduces noise at the output. Additional blocks, not shown in the block diagram, include a precise current limiter, reverse battery and current protection and thermal sensor.

### Thermal Overload Protection

The thermal overload protection limits the total power dissipation and protects the device from being damaged. When the junction temperature exceeds 150°, the device turns the p-channel pass transistor off.

### Reverse Battery Protection

The SiP21102 has a battery reverse protection circuitry that disconnects the internal circuitry when $V_{IN}$ drops below the GND voltage. There is no current drawn in such an event. When the $\overline{SD}$ pin is hardwired to $V_{IN}$, the user must connect the $\overline{SD}$ pin to $V_{IN}$ via a 100-kΩ resistor if reverse battery protection is desired. Hardwiring the $\overline{SD}$ pin directly to the $V_{IN}$ pin is allowed when reverse battery protection is not desired.

### $\overline{ERROR}$

$\overline{ERROR}$ is an open drain output that goes low when $V_{OUT}$ is less than 4% of its normal value. To obtain a logic level output, connect a pull-up resister from $\overline{ERROR}$ to $V_{OUT}$ or any other voltage equal to or less than $V_{IN}$. $\overline{ERROR}$ pin is high impedance (off) when $\overline{SD}$ pin is low.

### Auto-Discharge

$V_{OUT}$ has an internal 100-Ω (typ.) discharge path to ground when the $\overline{SD}$ pin is low.

### Stability

The circuit is stable with only a small output capacitor equal to 6 nF/mA (= 1 μF @ 150 mA). Since the bandwidth of the error amplifier is around 1−3 MHz and the dominant pole is at the output node, the capacitor should be capacitive in this range, i.e., for 150-mA load current, an ESR <0.4 Ω is necessary. Parasitic inductance of about 10 nH can be tolerated.