freescale
飞思卡尔(深圳)功率半导体有限公司

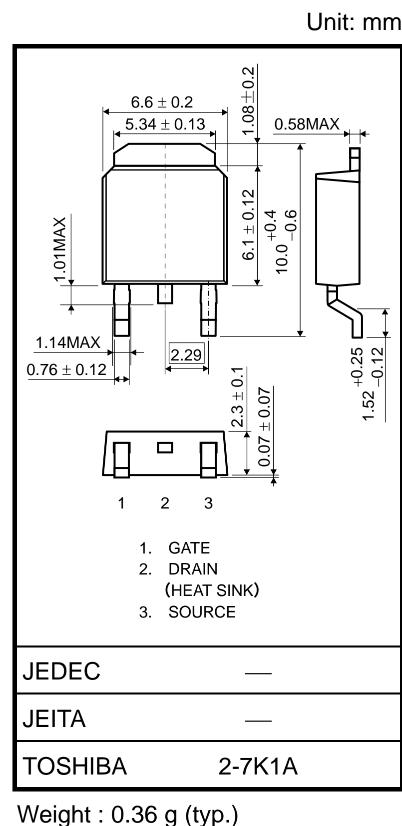
TK12P60W

Silicon N Channel MOS Type (DTMOS**IV**)

Switching Regulator Applications

- Low drain-source ON-resistance : $R_{DS\ (ON)}$ = 0.256Ω (typ.)
  by used to Super Junction Structure : DTMOS
- Easy to control Gate switching
- Enhancement-mode: V_{th} = 2.7 to 3.7 V (V_{DS} = 10 V, I_D = 0.6 mA)

Unit: mm



JEDEC	―
JEITA	―
TOSHIBA	2-7K1A

Weight : 0.36 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	600	V
Gate-source voltage	V_{GSS}	±30	V
Drain current (Continuous) (Note 1)	I_D	11.5	A
Drain current (Pulsed) (Note 1)	I_{DP}	46.0	A
Drain power dissipation (Tc = 25°C)	P_D	100	W
Single pulse avalanche energy (Note 2)	E_{AS}	93	mJ
Avalanche current	I_{AR}	5.8	A
Drain reverse current (Continuous) (Note 1)	I_{DR}	11.5	A
Drain reverse current (Pulsed) (Note 1)	I_{DRP}	46.0	A
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

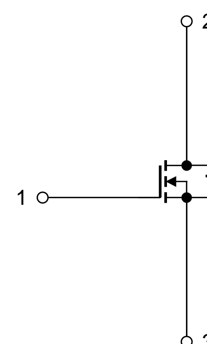
Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	1.25	°C/W

Note 1: Ensure that the channel temperature does not exceed 150°C.

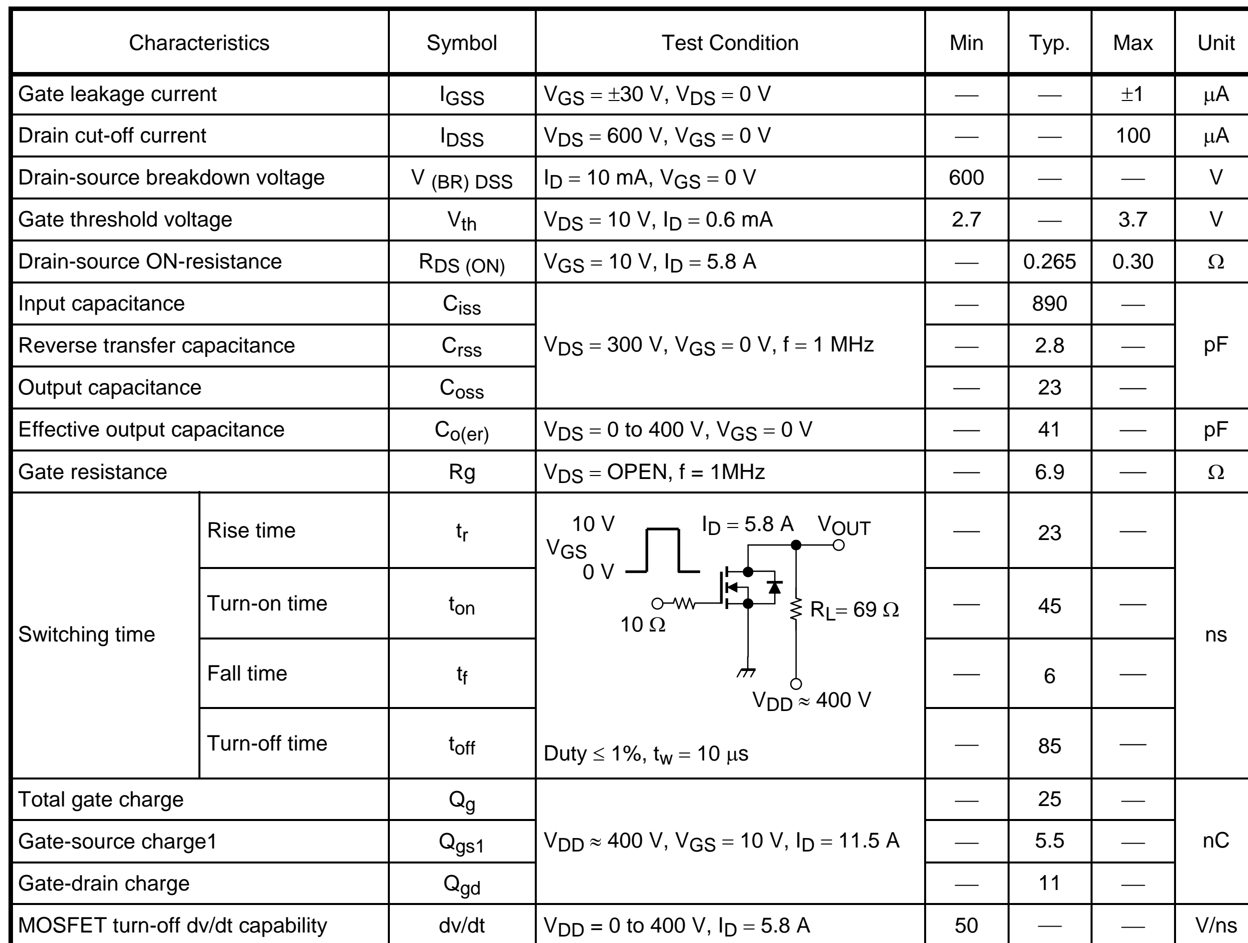
Note 2: V_{DD} = 90 V, T_{ch} = 25°C (initial), L = 4.83 mH, R_G = 25 Ω, I_{AR} = 5.8 A

This transistor is an electrostatic-sensitive device. Handle with care.

Internal Connection



Electrical Characteristics (Ta = 25°C)

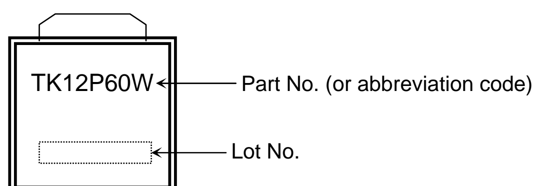


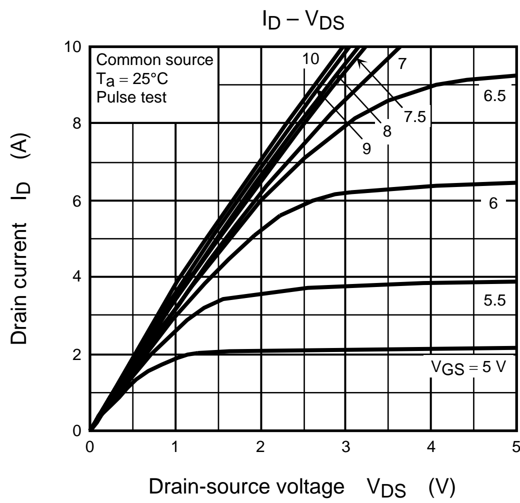
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V	—	—	±1	μA
Drain cut-off current		I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	600	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 0.6 mA	2.7	—	3.7	V
Drain-source ON-resistance		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 5.8 A	—	0.265	0.30	Ω
Input capacitance		C_{iss}	V_{DS} = 300 V, V_{GS} = 0 V, f = 1 MHz	—	890	—	pF
Reverse transfer capacitance		C_{rss}		—	2.8	—	
Output capacitance		C_{oss}		—	23	—	
Effective output capacitance		$C_{o(er)}$	V_{DS} = 0 to 400 V, V_{GS} = 0 V	—	41	—	pF
Gate resistance		Rg	V_{DS} = OPEN, f = 1MHz	—	6.9	—	Ω
Switching time	Rise time	t_r	10 V, V_{GS}, 0 V, 10 Ω, I_D = 5.8 A, V_{OUT}, R_L= 69 Ω, V_{DD} ≈ 400 V	—	23	—	ns
	Turn-on time	t_{on}		—	45	—	
	Fall time	t_f		—	6	—	
	Turn-off time	t_{off}	Duty ≤ 1%, t_w = 10 μs	—	85	—	
Total gate charge		Q_g	V_{DD} ≈ 400 V, V_{GS} = 10 V, I_D = 11.5 A	—	25	—	nC
Gate-source charge1		Q_{gs1}		—	5.5	—	
Gate-drain charge		Q_{gd}		—	11	—	
MOSFET turn-off dv/dt capability		dv/dt	V_{DD} = 0 to 400 V, I_D = 5.8 A	50	—	—	V/ns

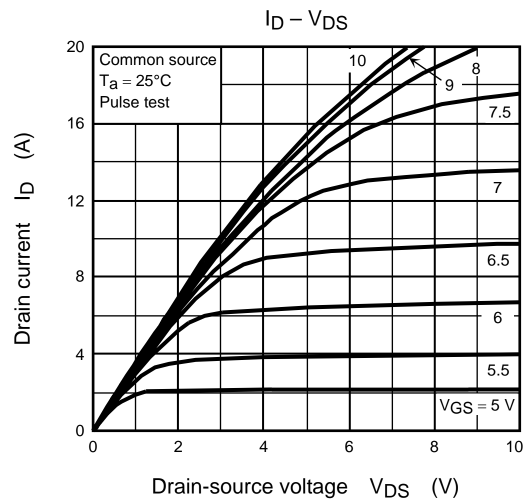
Source-Drain Characteristics (Ta = 25°C)

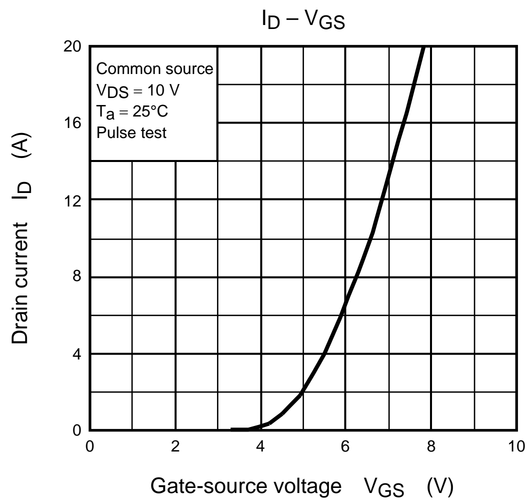
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Forward voltage (diode)	V_{DSF}	I_{DR} = 11.5 A, V_{GS} = 0 V	—	—	–1.7	V
Reverse recovery time	t_{rr}	I_{DR} = 11.5 A, V_{GS} = 0 V, -dI_{DR}/dt = 100 A/μs	—	380	—	ns
Reverse recovery charge	Q_{rr}		—	3.8	—	μC
Reverse recovery peak current	I_{rr}		—	25	—	A
Reverse Diode dv/dt capability	dv/dt	I_{DR} = 11.5 A, V_{GS} = 0 V, V_{DD} = 400 V	15	—	—	V/ns

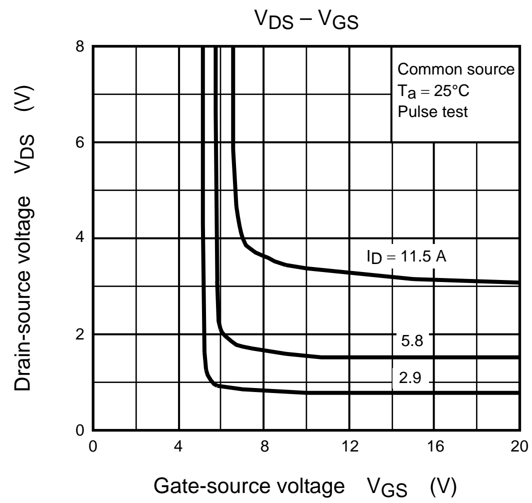
Marking

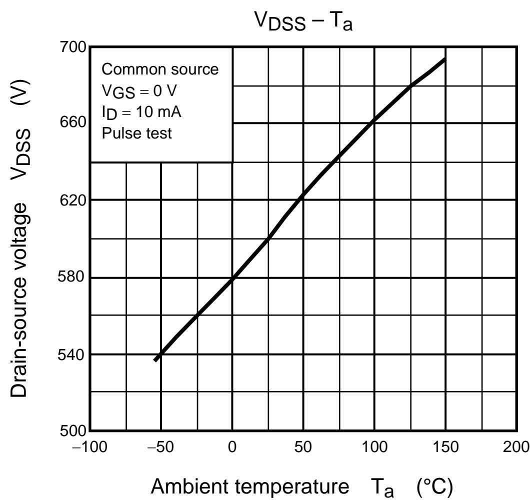


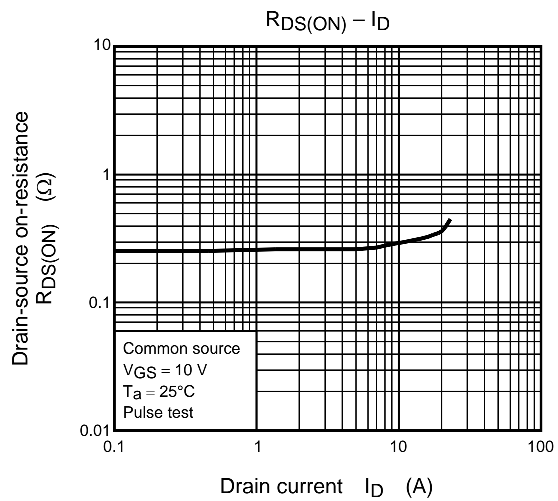

ID – VDS
Common source
Ta = 25°C
Pulse test
10
9
8
7.5
7
6.5
6
5.5
VGS = 5 V
Drain current ID (A)
Drain-source voltage VDS (V)

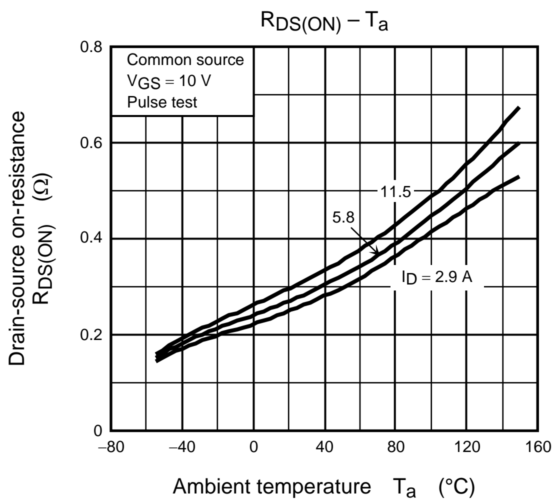

ID – VDS
Common source
Ta = 25°C
Pulse test
10
9
8
7.5
7
6.5
6
5.5
VGS = 5 V
Drain current ID (A)
Drain-source voltage VDS (V)

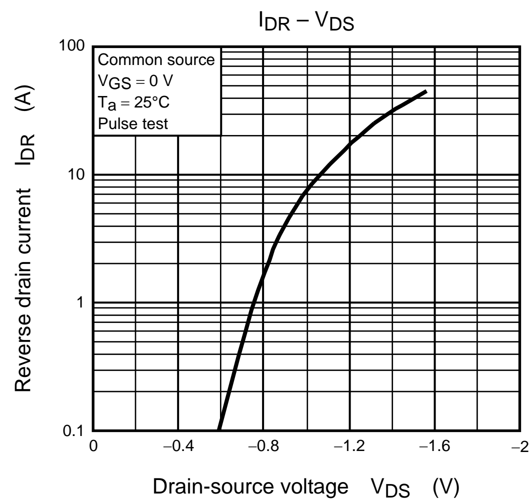

ID – VGS
Common source
VDS = 10 V
Ta = 25°C
Pulse test
Drain current ID (A)
Gate-source voltage VGS (V)

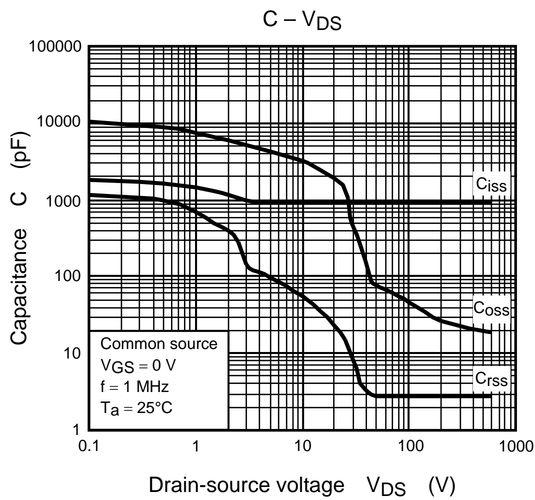

VDS – VGS
Common source
Ta = 25°C
Pulse test
ID = 11.5 A
5.8
2.9
Drain-source voltage VDS (V)
Gate-source voltage VGS (V)

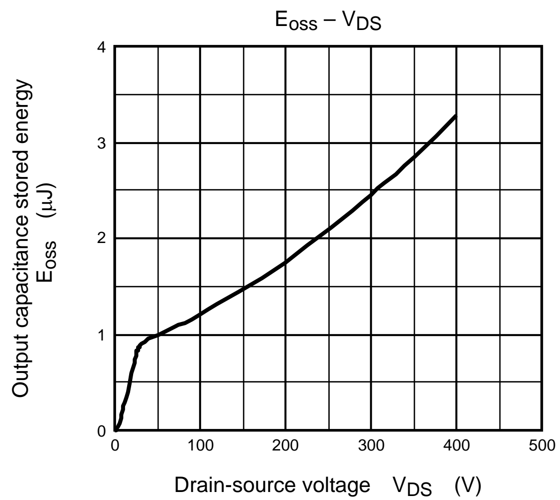

VDSS – Ta
Common source
VGS = 0 V
ID = 10 mA
Pulse test
Drain-source voltage VDSS (V)
Ambient temperature Ta (°C)

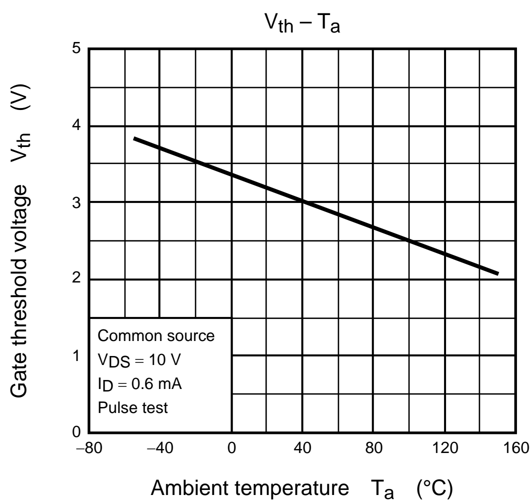

RDS(ON) – ID
Common source
VGS = 10 V
Ta = 25°C
Pulse test
Drain-source on-resistance RDS(ON) (Ω)
Drain current ID (A)

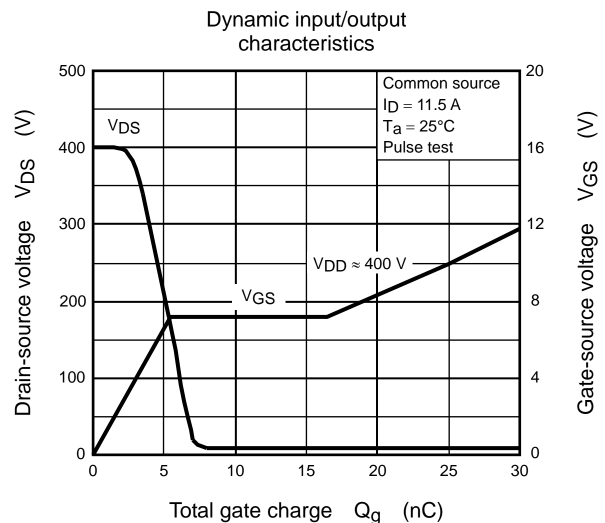

RDS(ON) – Ta
Common source
VGS = 10 V
Pulse test
11.5
5.8
ID = 2.9 A
Drain-source on-resistance RDS(ON) (Ω)
Ambient temperature Ta (°C)

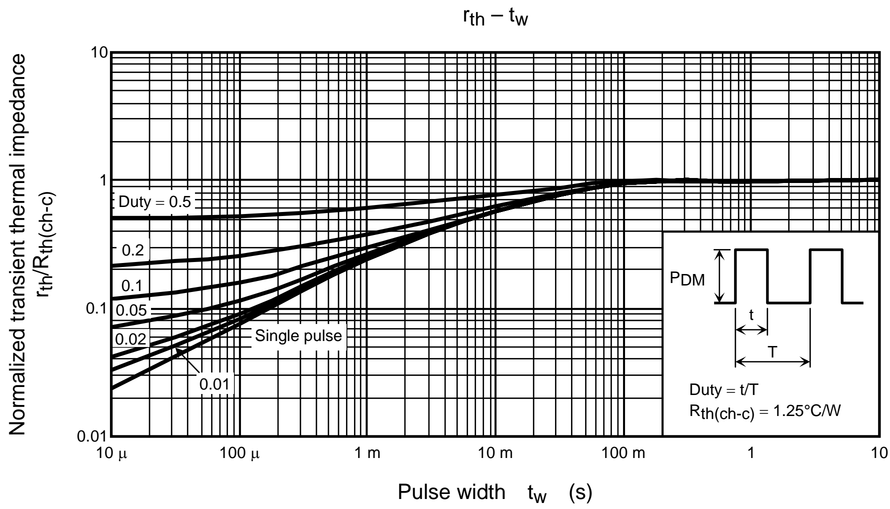

IDR – VDS
Common source
VGS = 0 V
Ta = 25°C
Pulse test
Reverse drain current IDR (A)
Drain-source voltage VDS (V)

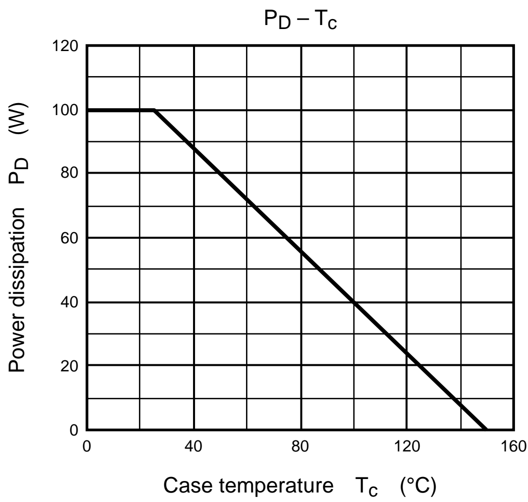

C – VDS
Ciss
Coss
Crss
Common source
VGS = 0 V
f = 1 MHz
Ta = 25°C
Capacitance C (pF)
Drain-source voltage VDS (V)

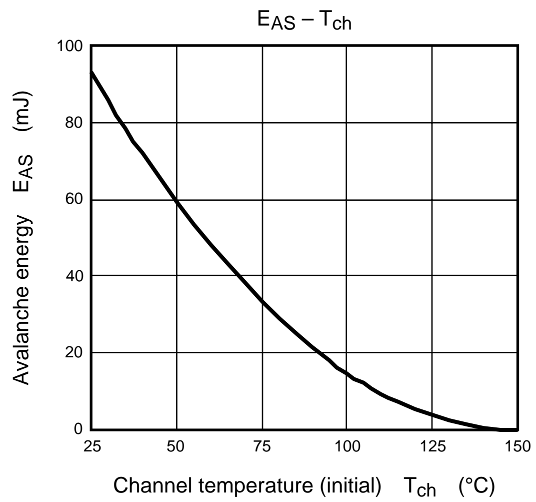

Eoss – VDS
Output capacitance stored energy Eoss (μJ)
Drain-source voltage VDS (V)

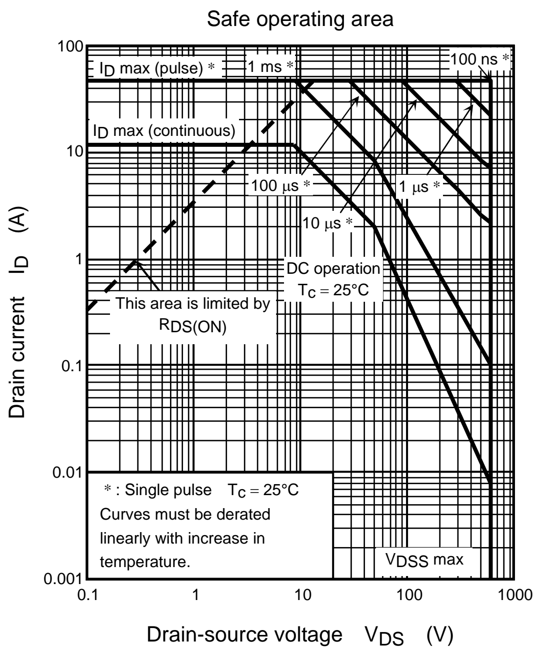

Vth – Ta
Common source
VDS = 10 V
ID = 0.6 mA
Pulse test
Gate threshold voltage Vth (V)
Ambient temperature Ta (°C)

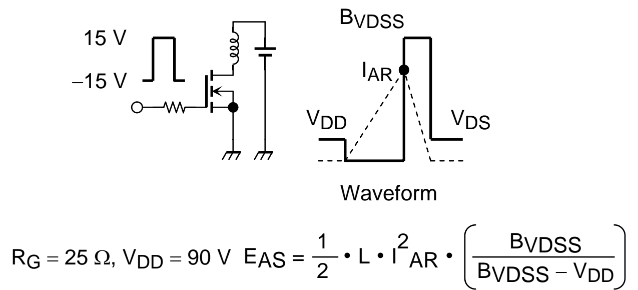

Dynamic input/output characteristics
Common source
ID = 11.5 A
Ta = 25°C
Pulse test
VDS
VDD ≈ 400 V
VGS
Drain-source voltage VDS (V)
Gate-source voltage VGS (V)
Total gate charge Qg (nC)











R_G = 25 Ω, V_{DD} = 90 V $E_{AS} = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$