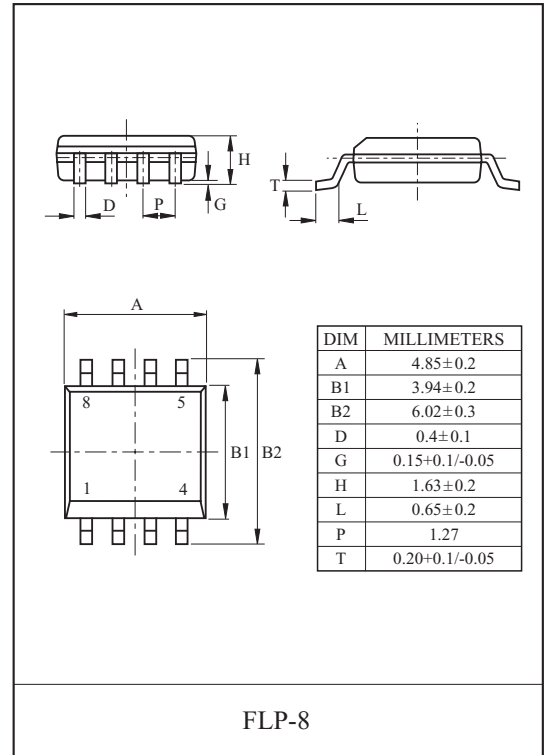


General Description

This Trench MOSFET has better characteristics, such as fast switching time, low on resistance, low gate charge and excellent avalanche characteristics. It is mainly suitable for Back-light Inverter.

FEATURES

- N-Channel
 - : $V_{DSS}=40V$, $I_D=6A$.
 - : $R_{DS(ON)}=31m\ \Omega$ (Max.) @ $V_{GS}=10V$
 - : $R_{DS(ON)}=45m\ \Omega$ (Max.) @ $V_{GS}=4.5V$
- P-Channel
 - : $V_{DSS}=-40V$, $I_D=-5A$.
 - : $R_{DS(ON)}=45m\ \Omega$ (Max.) @ $V_{GS}=-10V$
 - : $R_{DS(ON)}=63m\ \Omega$ (Max.) @ $V_{GS}=-4.5V$
- Super High Dense Cell Design.

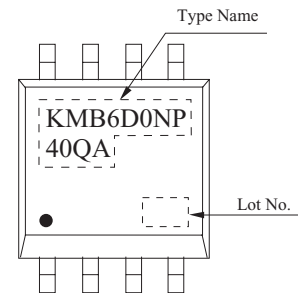


MAXIMUM RATING (Ta=25 °C)

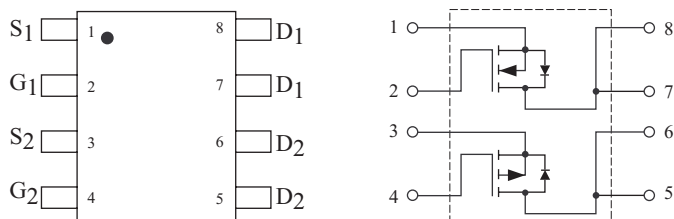
| CHARACTERISTIC | | SYMBOL | N-Ch | P-Ch | UNIT |
|---|--------------------|--------------|-----------|------|--------------|
| Drain-Source Voltage | | V_{DSS} | 40 | -40 | V |
| Gate-Source Voltage | | V_{GSS} | ±20 | ±20 | V |
| Drain Current | DC | I_D^* | 6 | -5 | A |
| | Pulsed | I_{DP}^* | 20 | -20 | |
| Source-Drain Diode Current | | I_S^* | 3.0 | -3.2 | A |
| Drain Power Dissipation | $T_A=25\ ^\circ C$ | P_D^* | 2 | 2 | W |
| | $T_A=70\ ^\circ C$ | | 1.3 | 1.3 | |
| Maximum Junction Temperature | | T_j | 150 | | $^\circ C$ |
| Storage Temperature Range | | T_{stg} | -55 ~ 150 | | $^\circ C$ |
| Thermal Resistance, Junction to Ambient | | R_{thJA}^* | 62.5 | | $^\circ C/W$ |

* : Surface Mounted on FR4 Board.

Marking



PIN CONNECTION (TOP VIEW)



KMB6D0NP40QA

ELECTRICAL CHARACTERISTICS (Ta=25°C)

| CHARACTERISTIC | SYMBOL | TEST CONDITION | | MIN. | TYP. | MAX. | UNIT |
|--|-----------------------|---|------|------|-------|------|------|
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | BV _{DSS} | I _D =250μA, V _{GS} =0V | N-Ch | 40 | - | - | V |
| | | I _D =-250μA, V _{GS} =0V | P-Ch | -40 | - | - | |
| Drain Cut-off Current | I _{DSS} | V _{DS} =32V, V _{GS} =0V | N-Ch | - | - | 1 | μA |
| | | V _{DS} =-32V, V _{GS} =0V | P-Ch | - | - | -1 | |
| Gate Leakage Current | I _{GSS} | V _{GS} = ±20V, V _{DS} =0V | N-Ch | - | - | ±100 | nA |
| | | | P-Ch | - | - | ±100 | |
| Gate Threshold Voltage | V _{th} | V _{DS} =V _{GS} , I _D =250μA | N-Ch | 1.0 | 2.3 | 3.0 | V |
| | | V _{DS} =V _{GS} , I _D =-250μA | P-Ch | -1.0 | -2.0 | -3.0 | |
| Drain-Source ON Resistance | R _{DS(ON)} * | V _{GS} =10V, I _D =6A | N-Ch | - | 19.6 | 31.0 | mΩ |
| | | V _{GS} =-10V, I _D =-5A | P-Ch | - | 31.2 | 45.0 | |
| | | V _{GS} =4.5V, I _D =5A | N-Ch | - | 39.9 | 45.0 | |
| | | V _{GS} =-4.5V, I _D =-2A | P-Ch | - | 47.6 | 63.0 | |
| Forward Transconductance | g _{fs} * | V _{DS} =5V, I _D =6A | N-Ch | - | 2.2 | - | S |
| | | V _{DS} =-5V, I _D =-4A | P-Ch | - | 9.5 | - | |
| Dynamic | | | | | | | |
| Input Capacitance | C _{iss} | | N-Ch | - | 420 | - | |
| | | | P-Ch | - | 850 | - | |
| Output Capacitance | C _{oss} | : V _{DS} =20V, V _{GS} =0V, f=1MHz | N-Ch | - | 160 | - | pF |
| | | | P-Ch | - | 220 | - | |
| Reverse transfer Capacitance | C _{rss} | : V _{DS} =-20V, V _{GS} =0V, f=1MHz | N-Ch | - | 40 | - | |
| | | | P-Ch | - | 82 | - | |
| Total Gate Charge | Q _g * | : V _{DS} =20V, I _D =6A, V _{GS} =10V : V _{DS} =-20V, I _D =-5A, V _{GS} =-10V | N-Ch | - | 12.0 | - | |
| | | | P-Ch | - | 15.0 | - | |
| Gate-Source Charge | Q _{gs} * | : V _{DS} =20V, I _D =6A, V _{GS} =10V | N-Ch | - | 1.6 | - | nC |
| | | | P-Ch | - | 2.0 | - | |
| Gate-Drain Charge | Q _{gd} * | : V _{DS} =-20V, I _D =-5A, V _{GS} =-4.5V | N-Ch | - | 2.6 | - | |
| | | | P-Ch | - | 6.5 | - | |
| Turn-on Delay time | t _{d(on)} * | | N-Ch | - | 9.0 | - | |
| | | | P-Ch | - | 17.0 | - | |
| Turn-on Rise time | t _r * | : V _{DD} =20V, I _D =6A, V _{GS} =10V, R _G =3Ω | N-Ch | - | 8.9 | - | ns |
| | | | P-Ch | - | 13.2 | - | |
| Turn-off Delay time | t _{d(off)} * | : V _{DD} =-20V, V _{GS} =-10V, R _G =3Ω, I _D =-5A | N-Ch | - | 23.6 | - | |
| | | | P-Ch | - | 38.0 | - | |
| Turn-off Fall time | t _f * | | N-Ch | - | 3.4 | - | |
| | | | P-Ch | - | 15.0 | - | |
| Source-Drain Diode Ratings | | | | | | | |
| Source-Drain Diode Forward Voltage | V _{SDr} * | I _S =1.0A, V _{GS} =0V | N-Ch | - | 0.71 | 1.2 | V |
| | | I _S =-1.0A, V _{GS} =0V | P-Ch | - | -0.71 | -1.2 | |
| Note>* Pulse Test : Pulse width <300μs , Duty cycle < 2% | | | | | | | |

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N-Channel

Fig1. $I_D - V_{DS}$

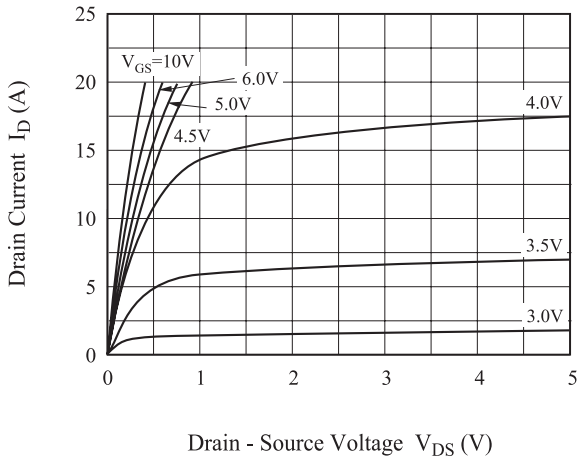


Fig2. $R_{DS(ON)} - I_D$

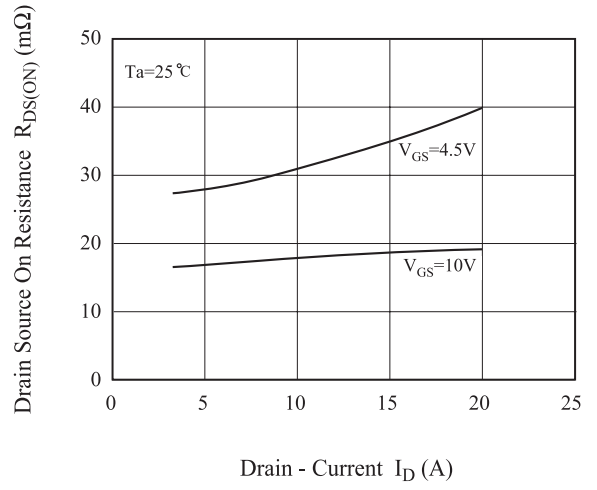


Fig3. $I_D - V_{GS}$

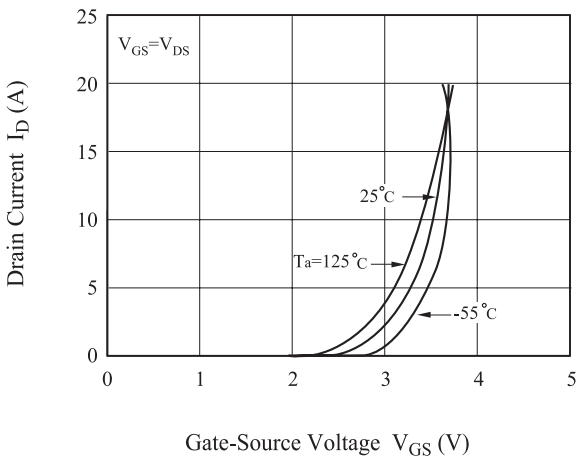


Fig4. $R_{DS(on)} - T_j$

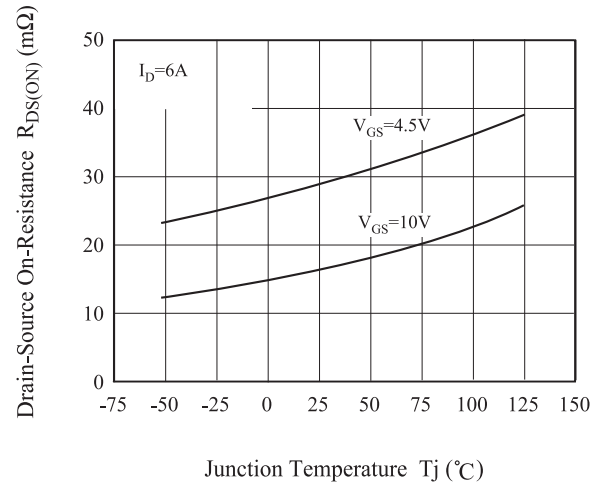


Fig5. $V_{th} - T_j$

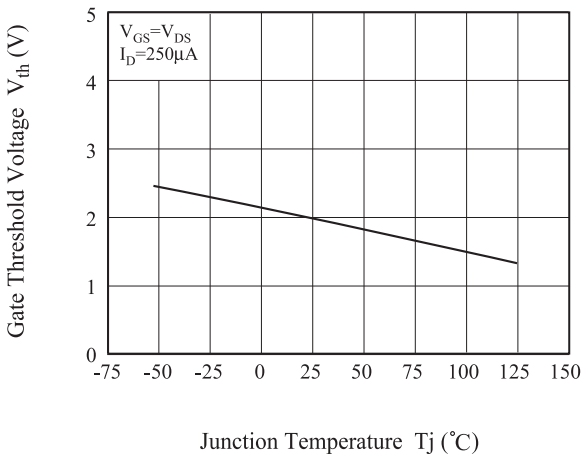
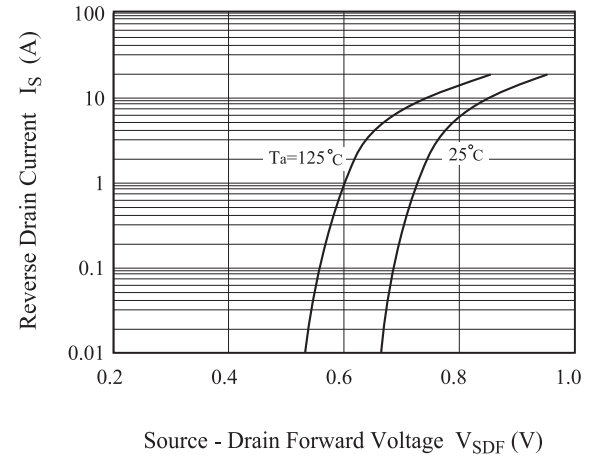


Fig6. $I_S - V_{SDF}$



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Fig 7. $V_{GS} - Q_g$

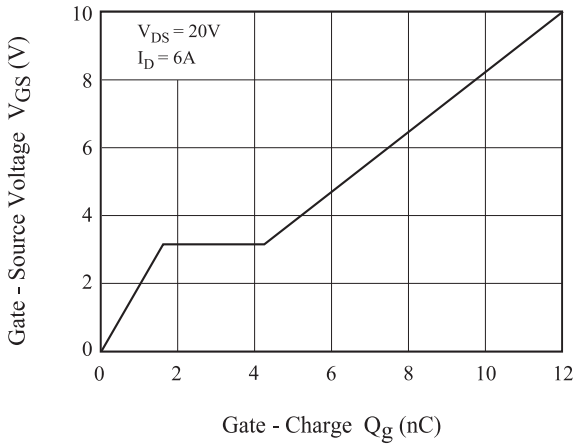


Fig 8. $C - V_{DS}$

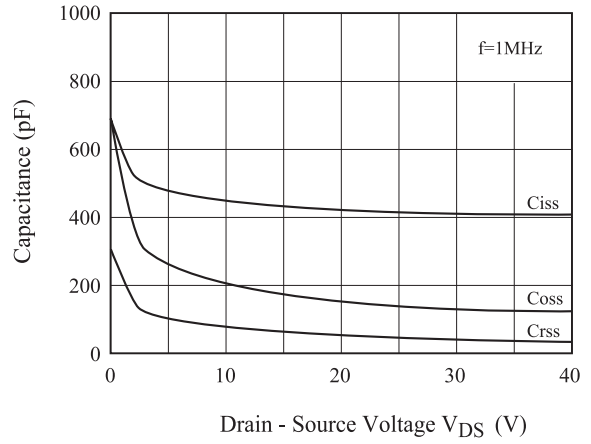


Fig9. Safe Operation Area

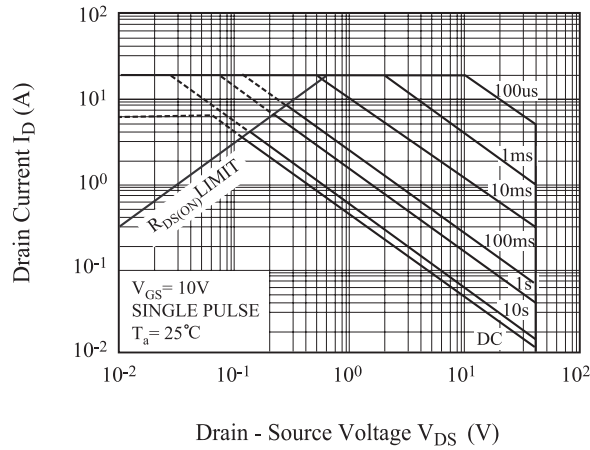
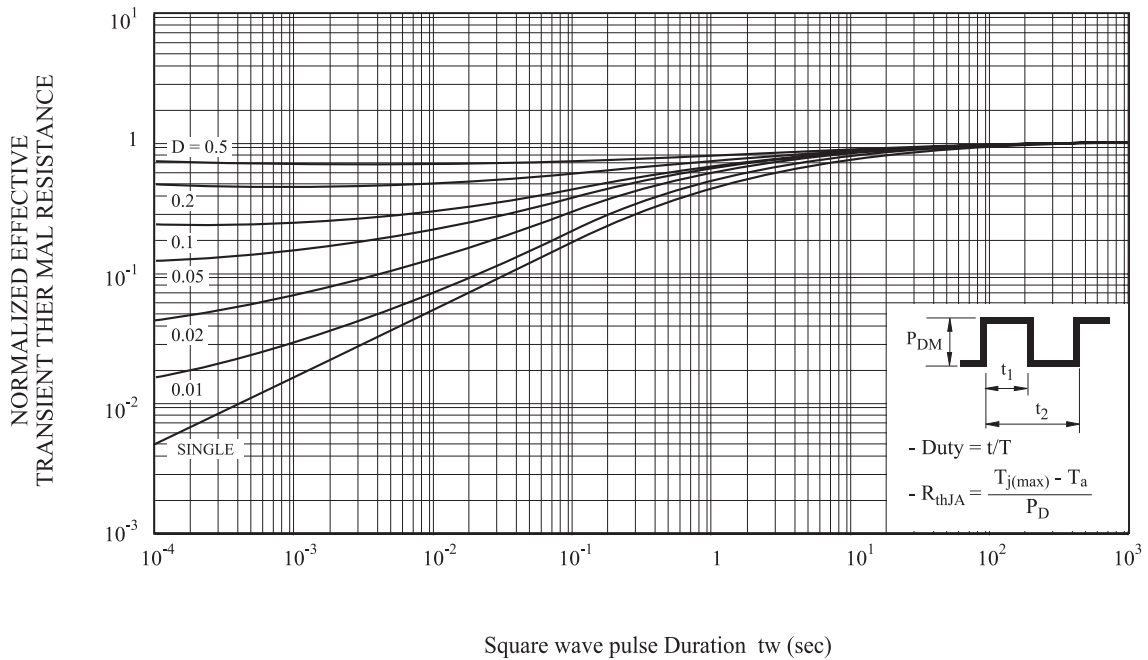


Fig10. Transient Thermal Response Curve



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Fig11. Gate Charge Circuit and Wave Form

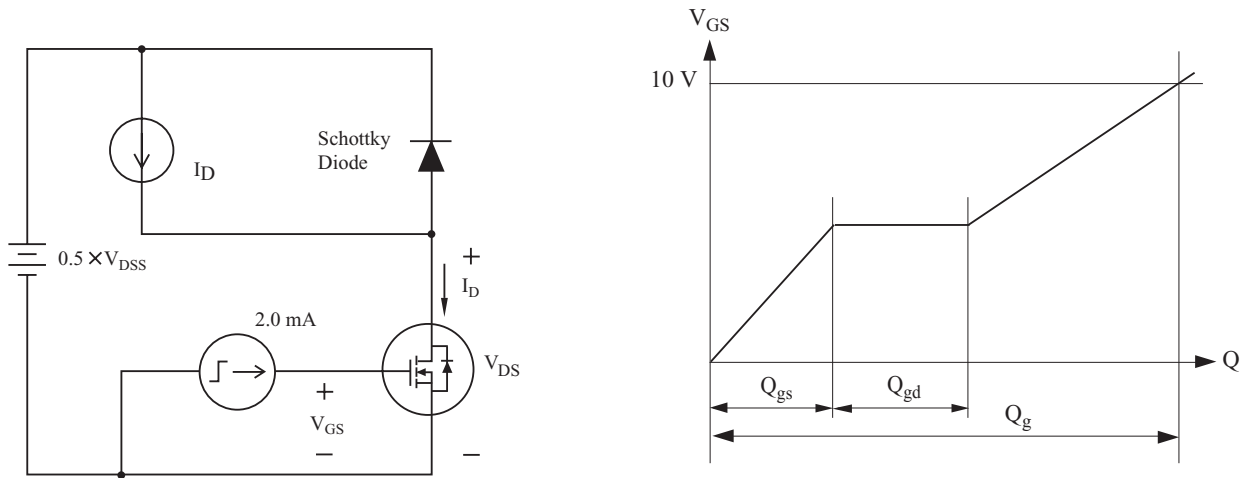
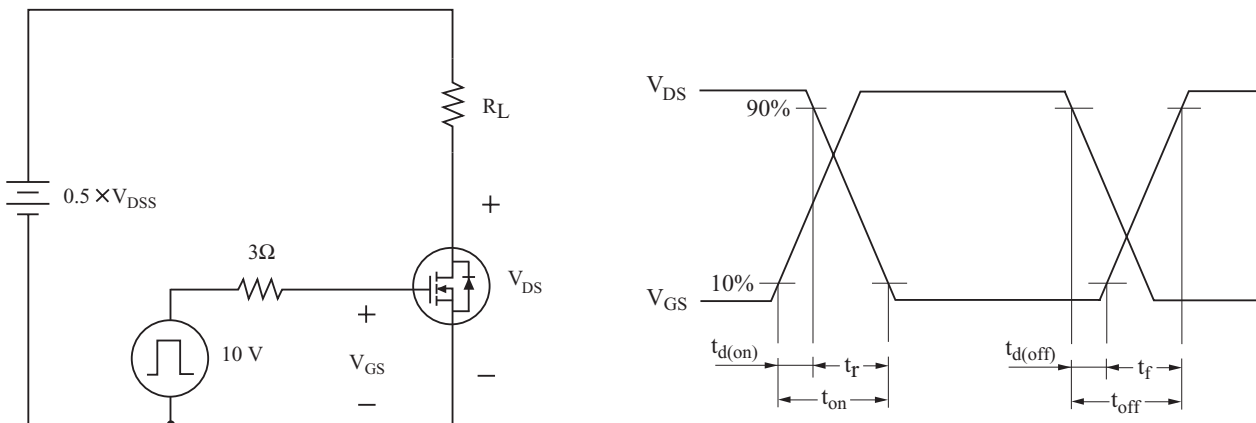


Fig12. Resistive Load Switching



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P-Channel

Fig1. $I_D - V_{DS}$

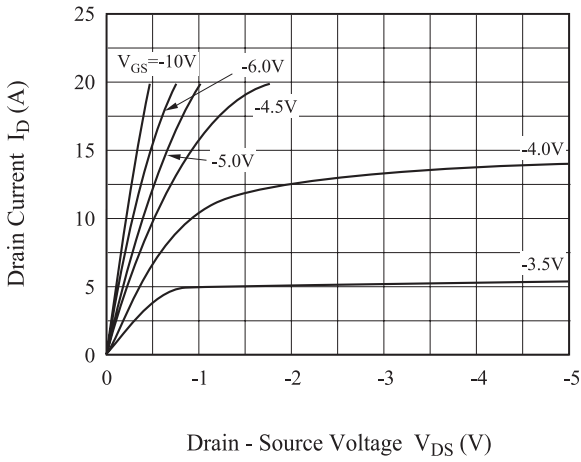


Fig2. $R_{DS(on)} - I_D$

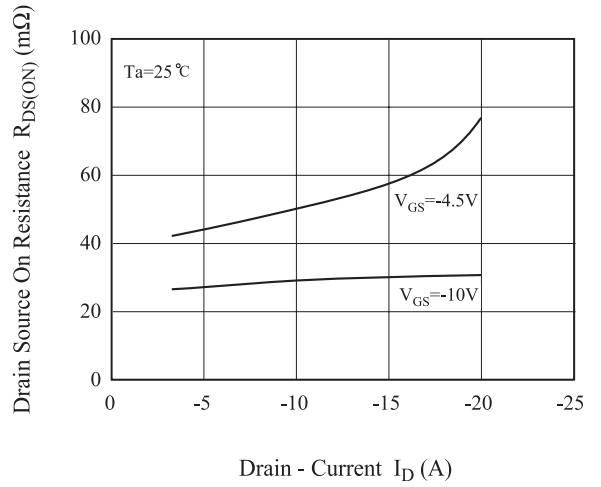


Fig3. $I_D - V_{GS}$

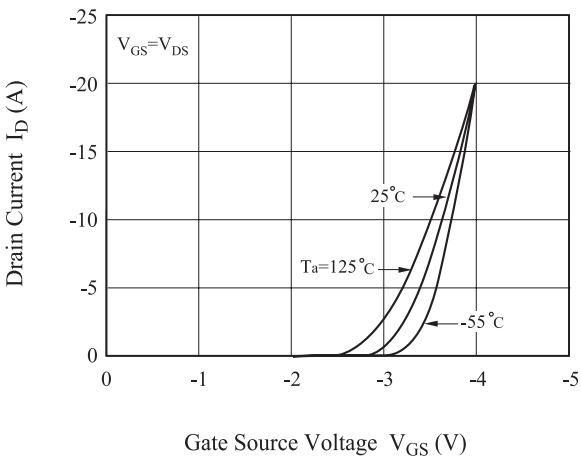


Fig4. $R_{DS(on)} - T_j$

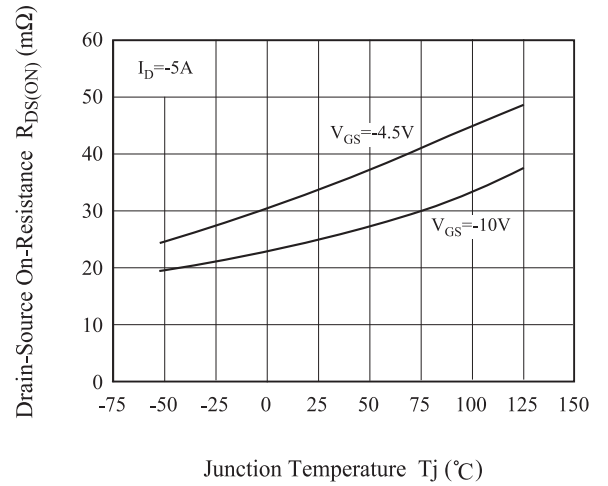


Fig5. $V_{th} - T_j$

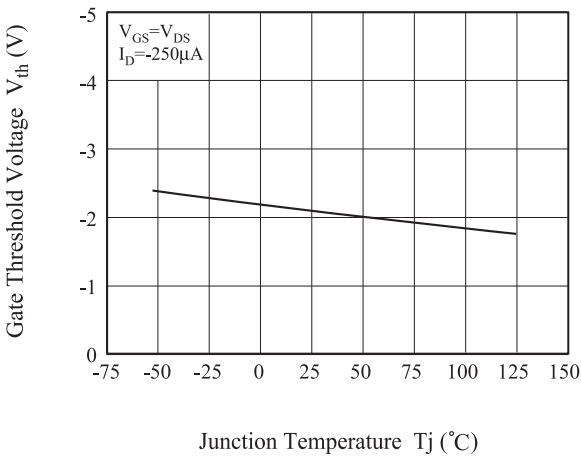
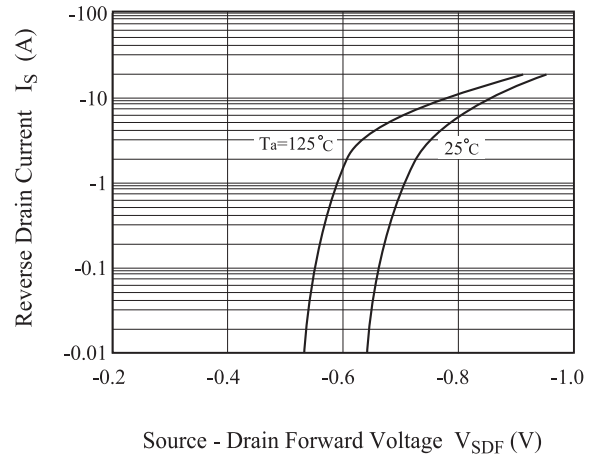


Fig6. $I_S - V_{SDF}$



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Fig 7. $V_{GS} - Q_g$

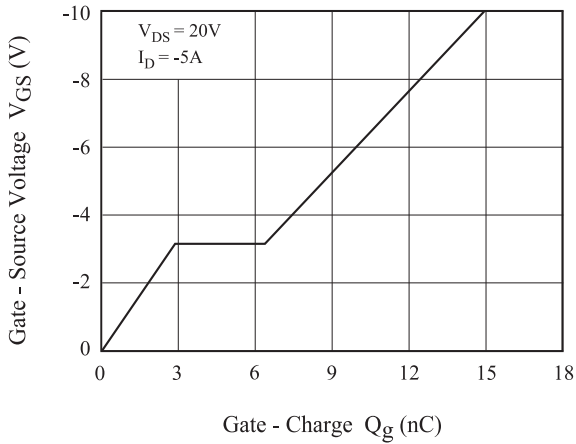


Fig 8. $C - V_{DS}$

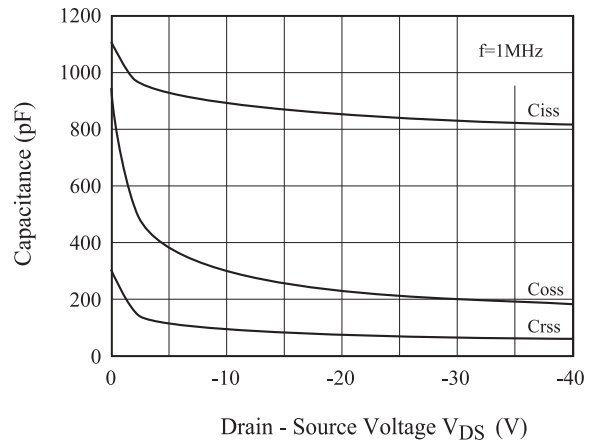


Fig9. Safe Operation Area

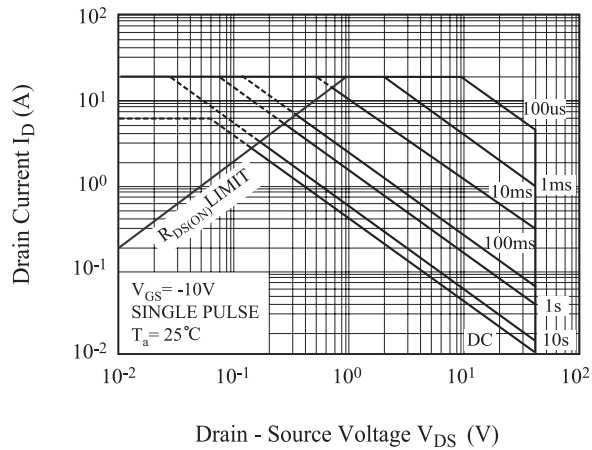
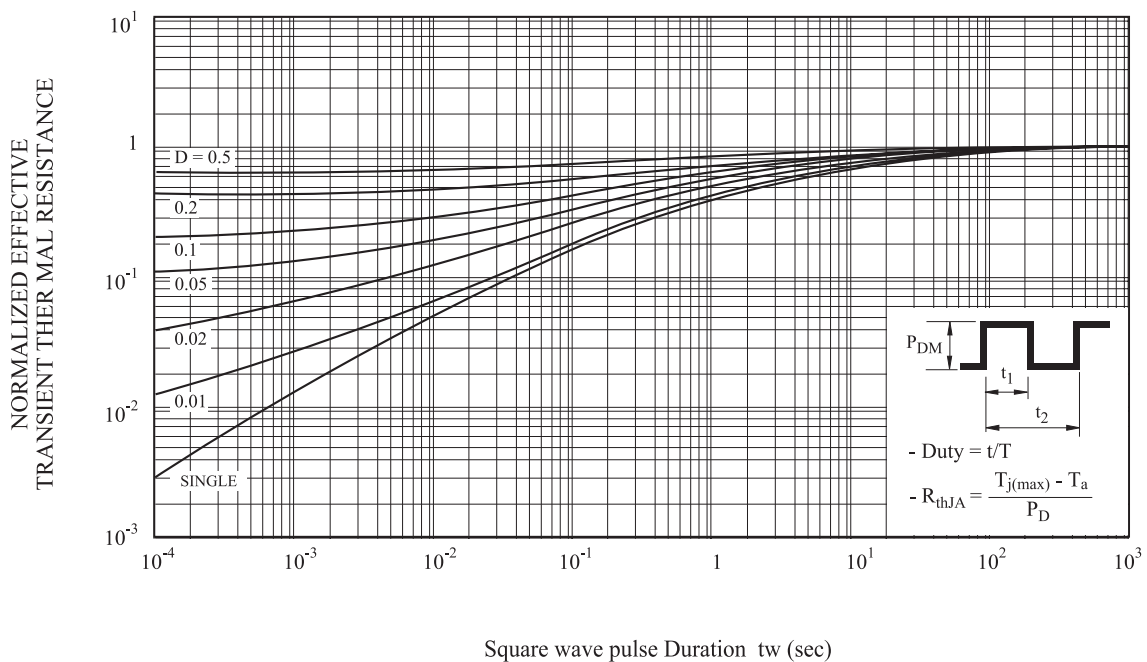


Fig10. Transient Thermal Response Curve



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Fig. 11 Gate Charge

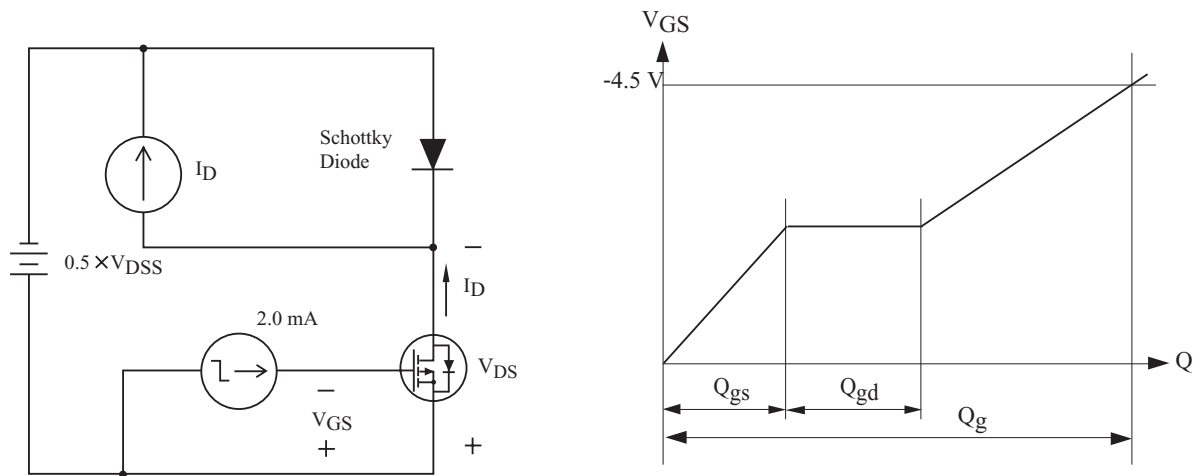


Fig. 12 Resistive Load Switching

