

## IR2213(S) & (PbF)

### HIGH AND LOW SIDE DRIVER

#### Features

- Floating channel designed for bootstrap operation  
 Fully operational to +1200V  
 Tolerant to negative transient voltage  
 dV/dt immune
- Gate drive supply range from 12 to 20V
- Undervoltage lockout for both channels
- 3.3V logic compatible  
 Separate logic supply range from 3.3V to 20V  
 Logic and power ground  $\pm 5V$  offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs
- Also available LEAD-FREE (PbF)

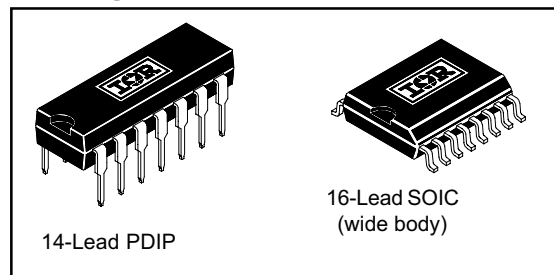
#### Description

The IR2213(S) is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 1200 volts.

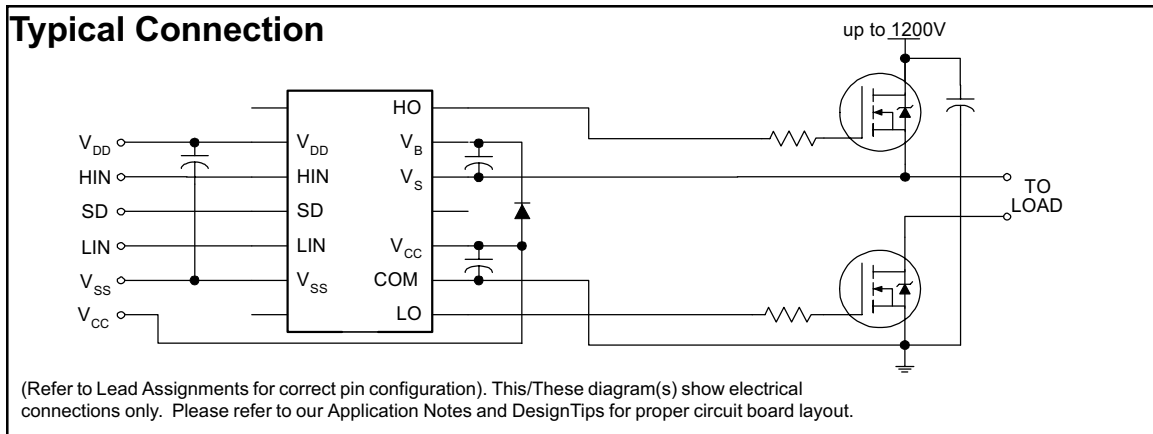
#### Product Summary

|                                  |                         |
|----------------------------------|-------------------------|
| <b>V<sub>OFFSET</sub></b>        | <b>1200V max.</b>       |
| <b>I<sub>O+/-</sub></b>          | <b>1.7A / 2A</b>        |
| <b>V<sub>OUT</sub></b>           | <b>12 - 20V</b>         |
| <b>t<sub>on/off</sub> (typ.)</b> | <b>280 &amp; 225 ns</b> |
| <b>Delay Matching</b>            | <b>30 ns</b>            |

#### Packages



#### Typical Connection



# IR2213(S) & (PbF)

## Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

| Symbol              | Definition   | Min.                  | Max.                  | Units |      |
|---------------------|--|-----------------------|-----------------------|-------|------|
| V <sub>B</sub>      | High Side Floating Supply Voltage                    | -0.3                  | 1225                  |       |      |
| V <sub>S</sub>      | High Side Floating Supply Offset Voltage             | V <sub>B</sub> - 25   | V <sub>B</sub> + 0.3  | V     |      |
| V <sub>HO</sub>     | High Side Floating Output Voltage                    | V <sub>S</sub> - 0.3  | V <sub>B</sub> + 0.3  |       |      |
| V <sub>CC</sub>     | Low Side Fixed Supply Voltage                        | -0.3                  | 25                    |       |      |
| V <sub>LO</sub>     | Low Side Output Voltage                              | -0.3                  | V <sub>CC</sub> + 0.3 |       |      |
| V <sub>DD</sub>     | Logic Supply Voltage                                 | -0.3                  | V <sub>SS</sub> + 25  |       |      |
| V <sub>SS</sub>     | Logic Supply Offset Voltage                          | V <sub>CC</sub> - 25  | V <sub>CC</sub> + 0.3 |       |      |
| V <sub>IN</sub>     | Logic Input Voltage (HIN, LIN & SD)                  | V <sub>SS</sub> - 0.3 | V <sub>DD</sub> + 0.3 |       |      |
| dV <sub>S</sub> /dt | Allowable Offset Supply Voltage Transient (Figure 2) | —                     | 50                    |       | V/ns |
| P <sub>D</sub>      | Package Power Dissipation @ T <sub>A</sub> ≤ +25°C   | (14 Lead PDIP)        | —                     | 1.6   | W    |
|                     |  | (16 Lead SOIC)        | —                     | 1.25  |      |
| R <sub>THJA</sub>   | Thermal Resistance, Junction to Ambient              | (14 Lead PDIP)        | —                     | 75    | °C/W |
|                     |  | (16 Lead SOIC)        | —                     | 100   |      |
| T <sub>J</sub>      | Junction Temperature                                 | —                     | 125                   | °C    |      |
| T <sub>S</sub>      | Storage Temperature                                  | -55                   | 150                   |       |      |
| T <sub>L</sub>      | Lead Temperature (Soldering, 10 seconds)             | —                     | 300                   |       |      |

## Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> and V<sub>SS</sub> offset ratings are tested with all supplies biased at 15V differential.

| Symbol          | Definition                                 | Min.                | Max.                 | Units |
|-----------------|--|---------------------|----------------------|-------|
| V <sub>B</sub>  | High Side Floating Supply Absolute Voltage | V <sub>S</sub> + 12 | V <sub>S</sub> + 20  | V     |
| V <sub>S</sub>  | High Side Floating Supply Offset Voltage   | Note 1              | 1200                 |       |
| V <sub>HO</sub> | High Side Floating Output Voltage          | V <sub>S</sub>      | V <sub>B</sub>       |       |
| V <sub>CC</sub> | Low Side Fixed Supply Voltage              | 12                  | 20                   |       |
| V <sub>LO</sub> | Low Side Output Voltage                    | 0                   | V <sub>CC</sub>      |       |
| V <sub>DD</sub> | Logic Supply Voltage                       | V <sub>SS</sub> + 3 | V <sub>SS</sub> + 20 |       |
| V <sub>SS</sub> | Logic Supply Offset Voltage                | -5 (Note 2)         | 5                    |       |
| V <sub>IN</sub> | Logic Input Voltage (HIN, LIN & SD)        | V <sub>SS</sub>     | V <sub>DD</sub>      |       |

Note 1: Logic operational for V<sub>S</sub> of -5 to +1200V. Logic state held for V<sub>S</sub> of -5V to -V<sub>BS</sub>. (Please refer to the Design Tip DT97-3 for more details).

Note 2: When V<sub>DD</sub><5V, the minimum V<sub>SS</sub> offset is limited to -V<sub>DD</sub>

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ,  $V_{DD}$ ) = 15V,  $C_L$  = 1000 pF,  $T_A$  = 25°C and  $V_{SS}$  = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

| Symbol    | Definition                          | Min. | Typ. | Max. | Units | Test Conditions |
|-----------|-------------------------------------|------|------|------|-------|-----------------|
| $t_{on}$  | Turn-On Propagation Delay           | —    | 280  | —    | ns    | $V_S = 0V$      |
| $t_{off}$ | Turn-Off Propagation Delay          | —    | 225  | —    |       | $V_S = 1200V$   |
| $t_{sd}$  | Shutdown Propagation Delay          | —    | 230  | —    |       | $V_S = 1200V$   |
| $t_r$     | Turn-On Rise Time                   | —    | 25   | —    |       |                 |
| $t_f$     | Turn-Off Fall Time                  | —    | 17   | —    |       |                 |
| MT        | Delay Matching, HS & LS Turn-On/Off | —    | —    | 30   |       |                 |

## Static Electrical Characteristics

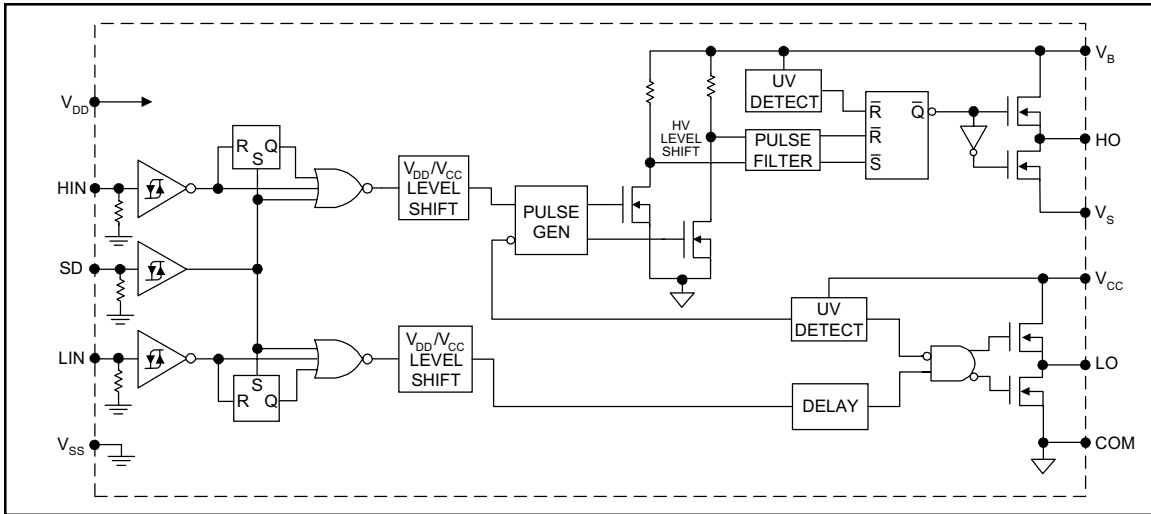
$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ,  $V_{DD}$ ) = 15V,  $T_A$  = 25°C and  $V_{SS}$  = COM unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to  $V_{SS}$  and are applicable to all three logic input leads: HIN, LIN and SD. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

| Symbol      | Definition  | Min. | Typ. | Max. | Units         | Test Conditions                                      |
|-------------|---|------|------|------|---------------|--|
| $V_{IH}$    | Logic "1" Input Voltage                               | 9.5  | —    | —    | V             |  |
| $V_{IL}$    | Logic "0" Input Voltage                               | —    | —    | 6.0  |               |  |
| $V_{OH}$    | High Level Output Voltage, $V_{BIAS} - V_O$           | —    | —    | 1.2  |               | $I_O = 0A$   |
| $V_{OL}$    | Low Level Output Voltage, $V_O$                       | —    | —    | 0.1  |               | $I_O = 0A$   |
| $I_{LK}$    | Offset Supply Leakage Current                         | —    | —    | 50   | $\mu A$       | $V_B = V_S = 1200V$                                  |
| $I_{QBS}$   | Quiescent $V_{BS}$ Supply Current                     | —    | 125  | 230  |               | $V_{IN} = 0V$ or $V_{DD}$                            |
| $I_{QCC}$   | Quiescent $V_{CC}$ Supply Current                     | —    | 180  | 340  |               | $V_{IN} = 0V$ or $V_{DD}$                            |
| $I_{QDD}$   | Quiescent $V_{DD}$ Supply Current                     | —    | 15   | 30   |               | $V_{IN} = 0V$ or $V_{DD}$                            |
| $I_{IN+}$   | Logic "1" Input Bias Current                          | —    | 20   | 40   |               | $V_{IN} = V_{DD}$                                    |
| $I_{IN-}$   | Logic "0" Input Bias Current                          | —    | —    | 1.0  | $V_{IN} = 0V$ |  |
| $V_{BSUV+}$ | $V_{BS}$ Supply Undervoltage Positive Going Threshold | 8.7  | 10.2 | 11.7 | V             |  |
| $V_{BSUV-}$ | $V_{BS}$ Supply Undervoltage Negative Going Threshold | 7.9  | 9.3  | 10.7 |               |  |
| $V_{CCUV+}$ | $V_{CC}$ Supply Undervoltage Positive Going Threshold | 8.7  | 10.2 | 11.7 |               |  |
| $V_{CCUV-}$ | $V_{CC}$ Supply Undervoltage Negative Going Threshold | 7.9  | 9.3  | 10.7 |               |  |
| $I_{O+}$    | Output High Short Circuit Pulsed Current              | 1.7  | 2.0  | —    | A             | $V_O = 0V$ , $V_{IN} = V_{DD}$<br>$PW \leq 10 \mu s$ |
| $I_{O-}$    | Output Low Short Circuit Pulsed Current               | 2.0  | 2.5  | —    |               | $V_O = 15V$ , $V_{IN} = 0V$<br>$PW \leq 10 \mu s$    |

# IR2213(S) & (PbF)

International  
**IR** Rectifier

## Functional Block Diagram



## Lead Definitions

| Symbol          | Description   |
|-----------------|---|
| V <sub>DD</sub> | Logic supply  |
| HIN             | Logic input for high side gate driver output (HO), in phase |
| SD              | Logic input for shutdown                                    |
| LIN             | Logic input for low side gate driver output (LO), in phase  |
| V <sub>SS</sub> | Logic ground  |
| V <sub>B</sub>  | High side floating supply                                   |
| HO              | High side gate drive output                                 |
| V <sub>S</sub>  | High side floating supply return                            |
| V <sub>CC</sub> | Low side supply   |
| LO              | Low side gate drive output                                  |
| COM             | Low side return   |

## Lead Assignments

|                     |                                 |
|---------------------|---------------------------------|
| <p>14 Lead PDIP</p> | <p>16 Lead SOIC (Wide Body)</p> |
| <b>IR2213</b>       | <b>IR2213S</b>                  |
| <b>Part Number</b>  |                                 |

# IR2213(s) & (PbF)

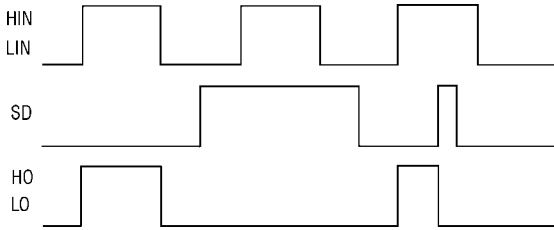


Figure 1. Input/Output Timing Diagram

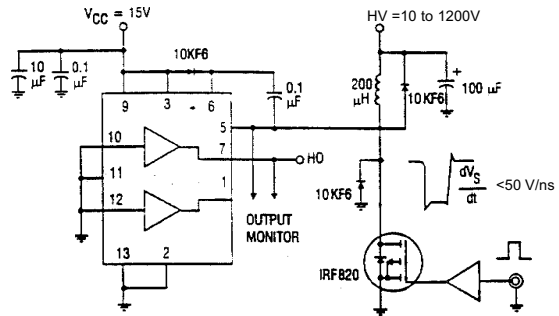


Figure 2. Floating Supply Voltage Transient Test Circuit

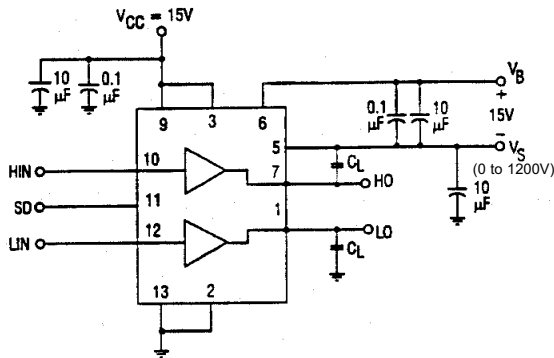


Figure 3. Switching Time Test Circuit

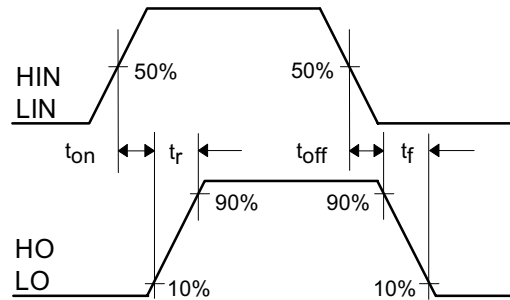


Figure 4. Switching Time Waveform Definition

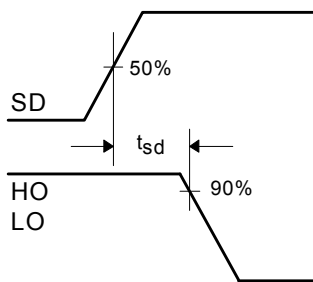


Figure 5. Shutdown Waveform Definitions

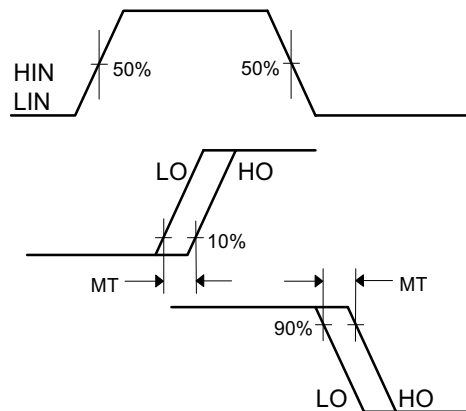
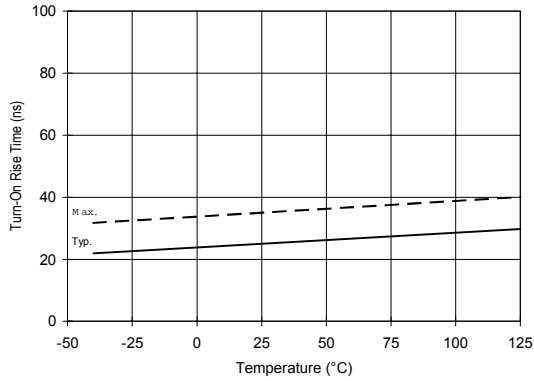
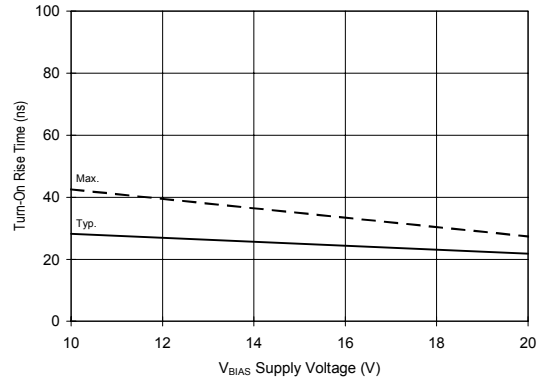


Figure 6. Delay Matching Waveform Definitions

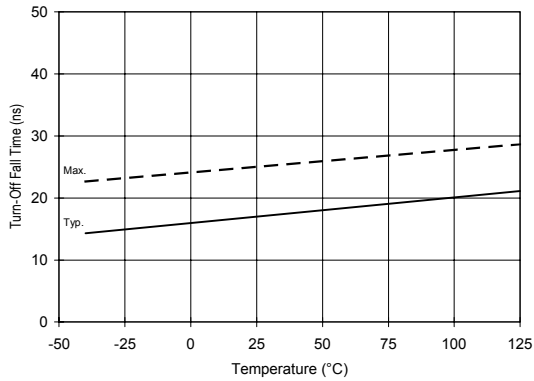
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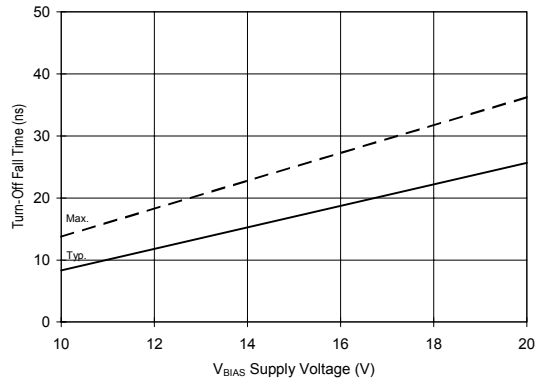
**Figure 10A. Turn-On Rise Time vs. Temperature**



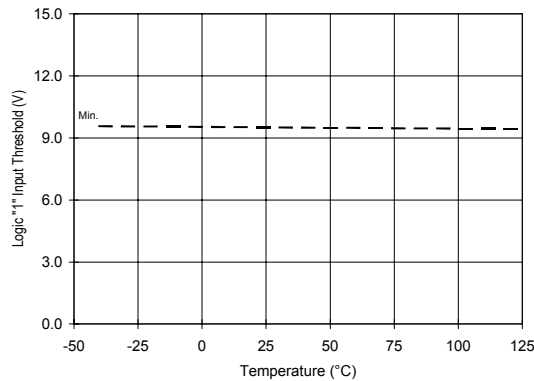
**Figure 10B. Turn-On Rise Time vs. Voltage**



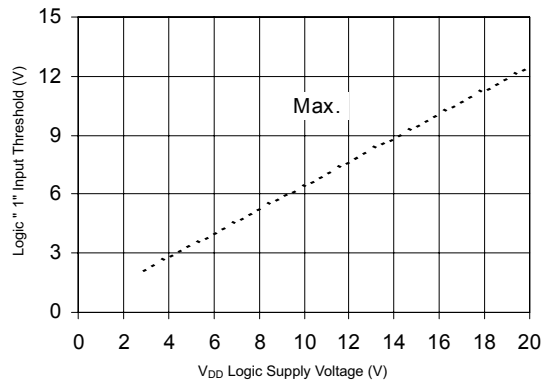
**Figure 11A. Turn-Off Fall Time vs. Temperature**



**Figure 11B. Turn-Off Fall Time vs. Voltage**



**Figure 12A. Logic "1" Input Threshold vs. Temperature**



**Figure 12B. Logic "1" Input Threshold vs. Voltage**

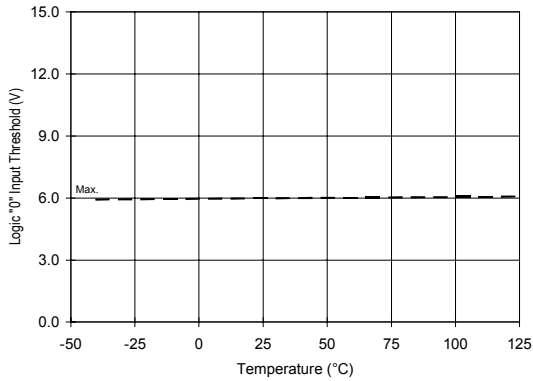


Figure 13A. Logic "0" Input Threshold vs. Temperature

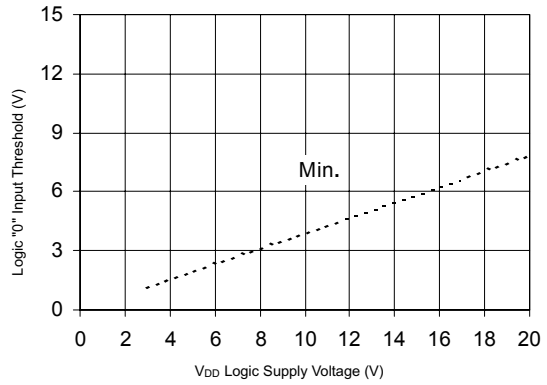


Figure 13B. Logic "0" Input Threshold vs. Voltage

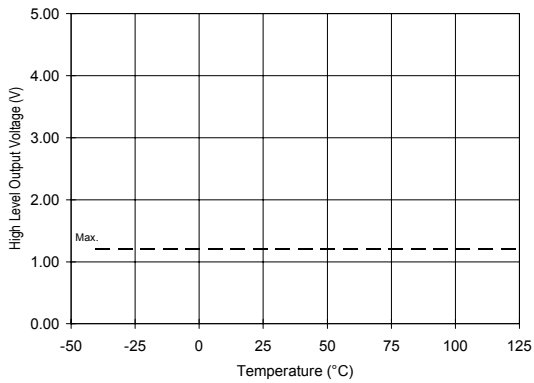


Figure 14A. High Level Output vs. Temperature

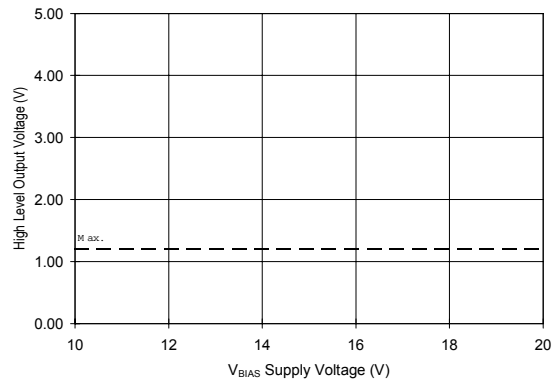


Figure 14B. High Level Output vs. Voltage

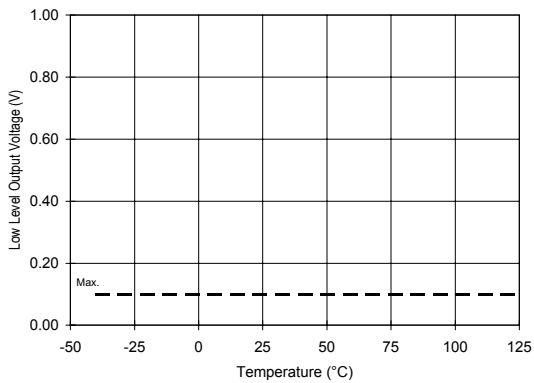


Figure 15A. Low Level Output vs. Temperature

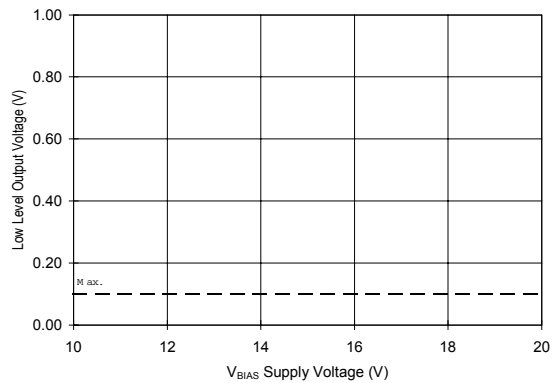


Figure 15B. Low Level Output vs. Voltage

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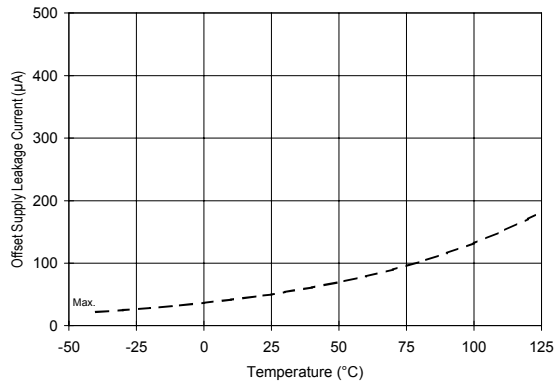


Figure 16A. Offset Supply Current vs. Temperature

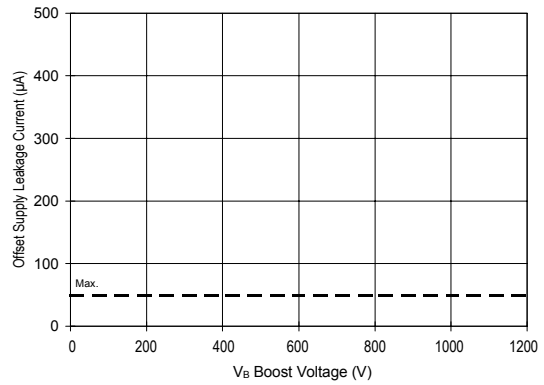


Figure 16B. Offset Supply Current vs. Voltage

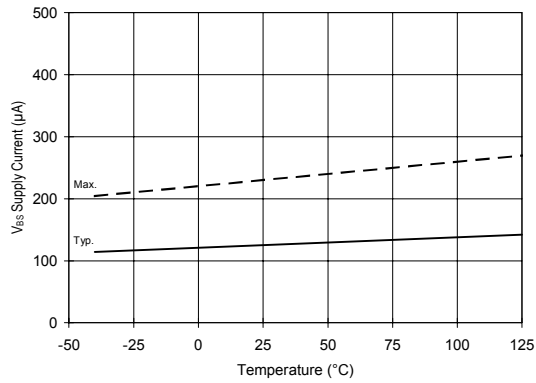


Figure 17A. V<sub>BS</sub> Supply Current vs. Temperature

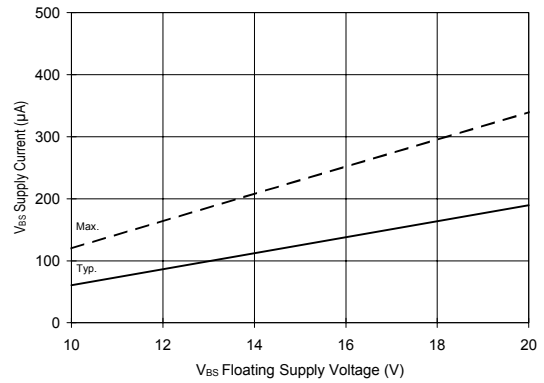


Figure 17B. V<sub>BS</sub> Supply Current vs. Voltage

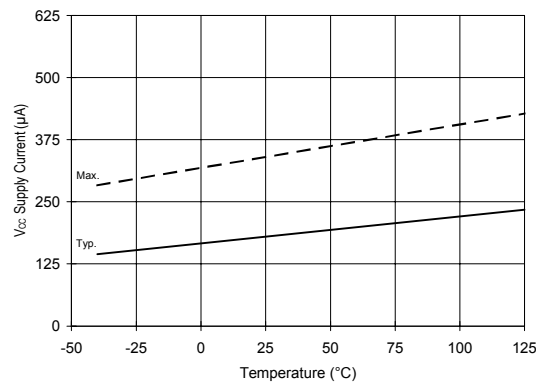


Figure 18A. V<sub>CC</sub> Supply Current vs. Temperature

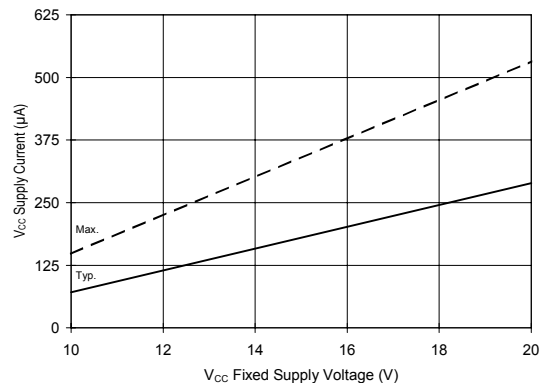


Figure 18B. V<sub>CC</sub> Supply Current vs. Voltage



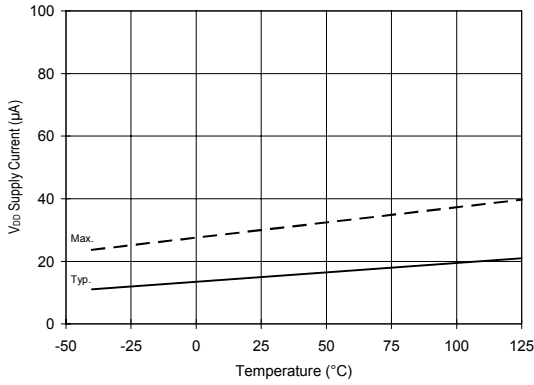


Figure 19A. V<sub>DD</sub> Supply Current vs. Temperature

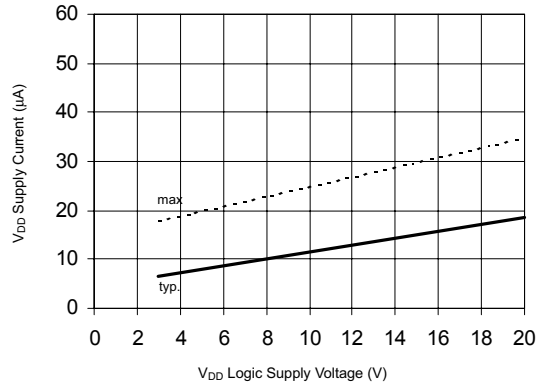


Figure 19B. V<sub>DD</sub> Supply Current vs. V<sub>DD</sub> Voltage

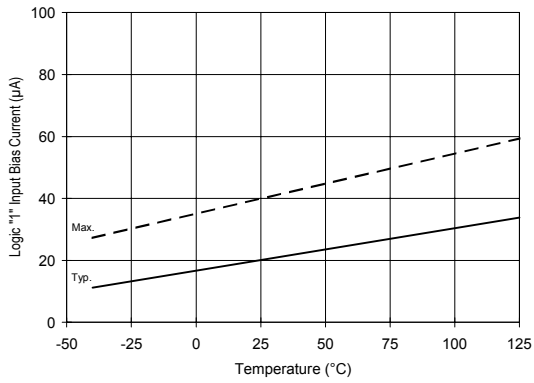


Figure 20A. Logic "1" Input Current vs. Temperature

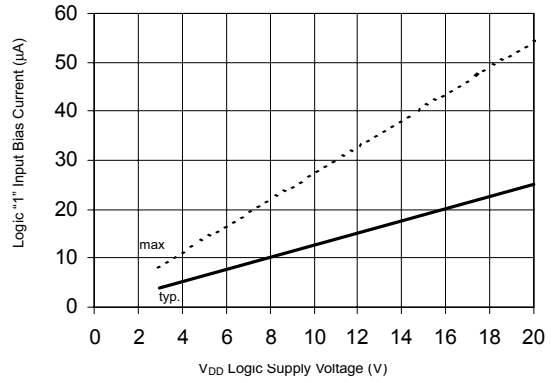


Figure 20B. Logic "1" Input Current vs. V<sub>DD</sub> Voltage

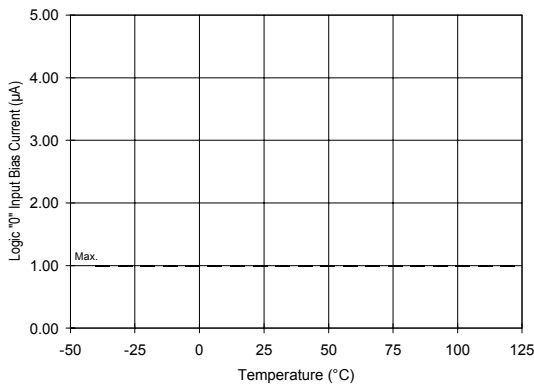


Figure 21A. Logic "0" Input Current vs. Temperature

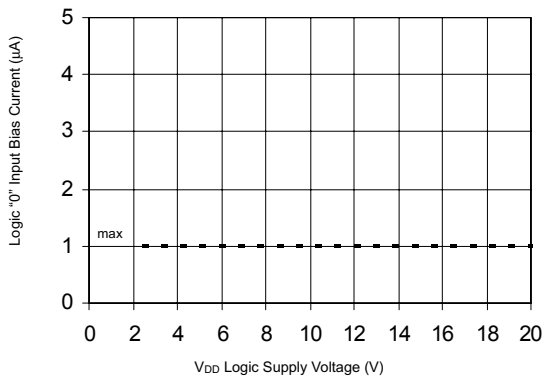
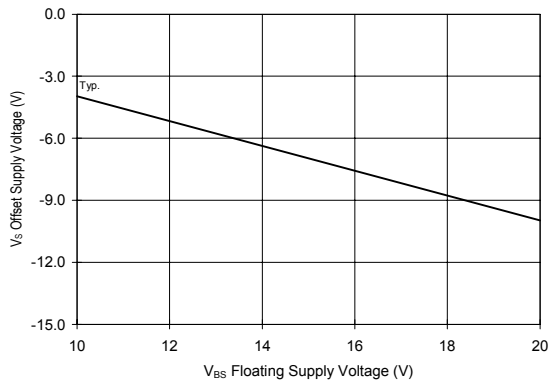
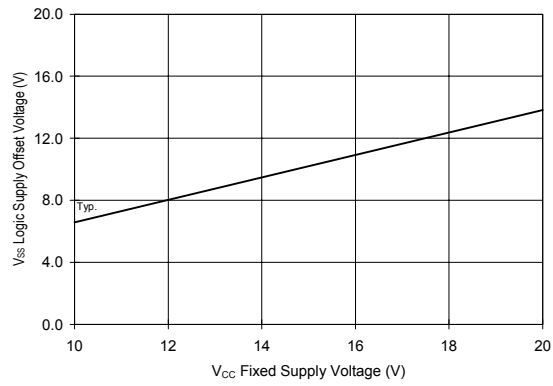


Figure 21B. Logic "0" Input Current vs. V<sub>DD</sub> Voltage

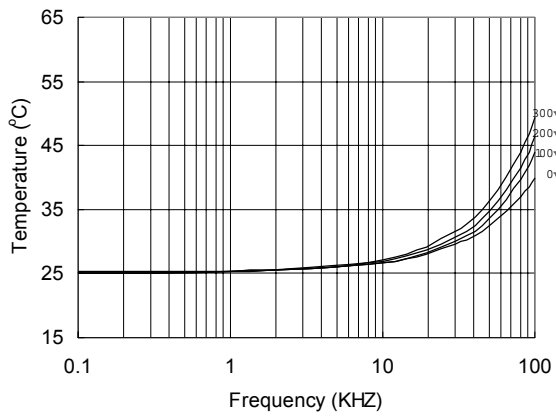
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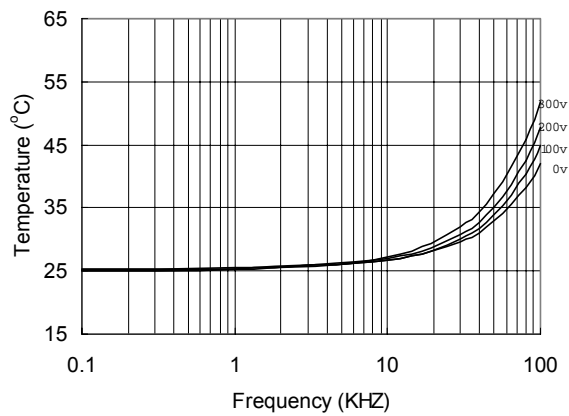
**Figure 22. Maximum V<sub>S</sub> Negative Offset vs. V<sub>BS</sub> Supply Voltage**



**Figure 23. Maximum V<sub>SS</sub> Positive Offset vs. V<sub>CC</sub> Supply Voltage**

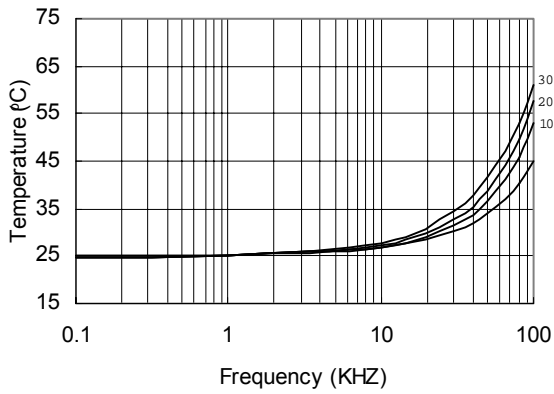


**Figure 24. IR2213s vs. Frequency (IRFBC20)**  
 $R_{gate}=33\Omega, V_{CC}=15V$

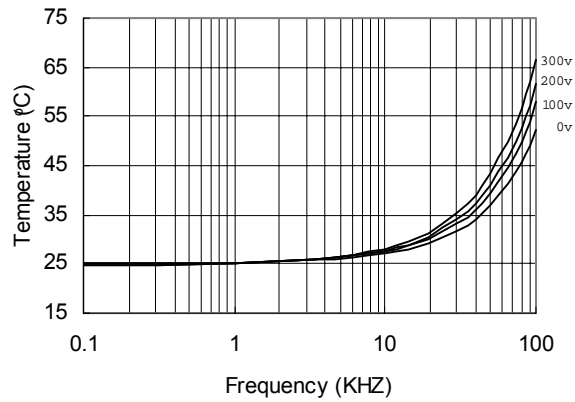


**Figure 25. IR2213s vs. Frequency (IRFBC30)**  
 $R_{gate}=22\Omega, V_{CC}=15V$

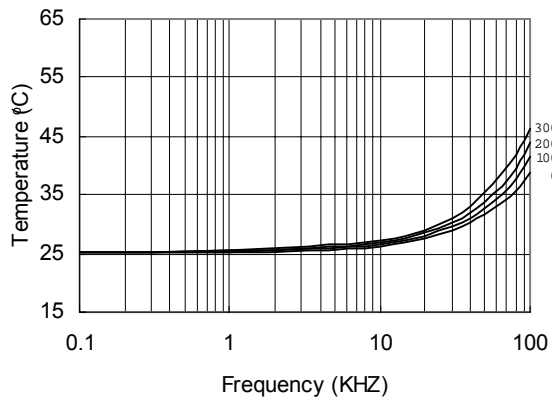
# IR2213(s) & (PbF)



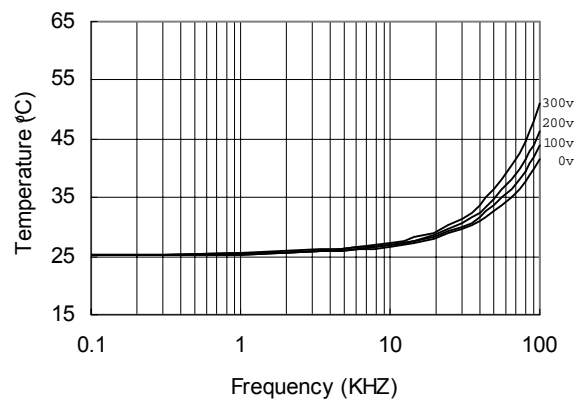
**Figure 26. IR2213s vs. Frequency (IRFBC40)**  
 $R_{gate}=15\Omega, V_{CC}=15V$



**Figure 27. IR2213s vs. Frequency (IRFBC50)**  
 $R_{gate}=10\Omega, V_{CC}=15V$



**Figure 28. IR2213 vs. Frequency (IRFBC20)**  
 $R_{gate}=33\Omega, V_{CC}=15V$



**Figure 29. IR2213 vs. Frequency (IRFBC30)**  
 $R_{gate}=22\Omega, V_{CC}=15V$

# IR2213(S) & (PbF)

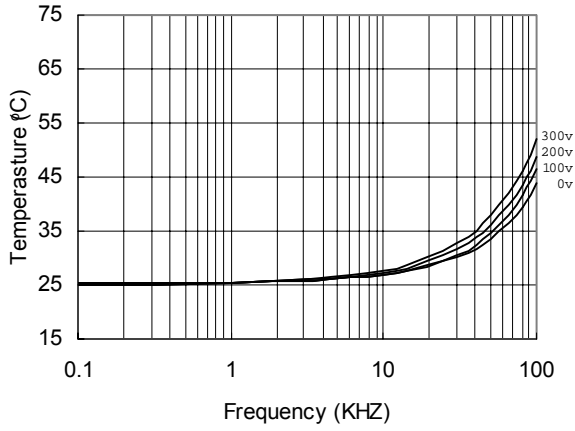


Figure 30. IR2213 vs. Frequency (IRFBC40)  
 $R_{gate}=15\Omega, V_{CC}=15V$

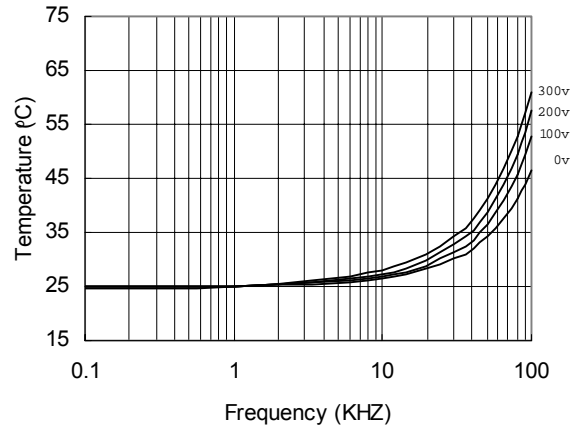
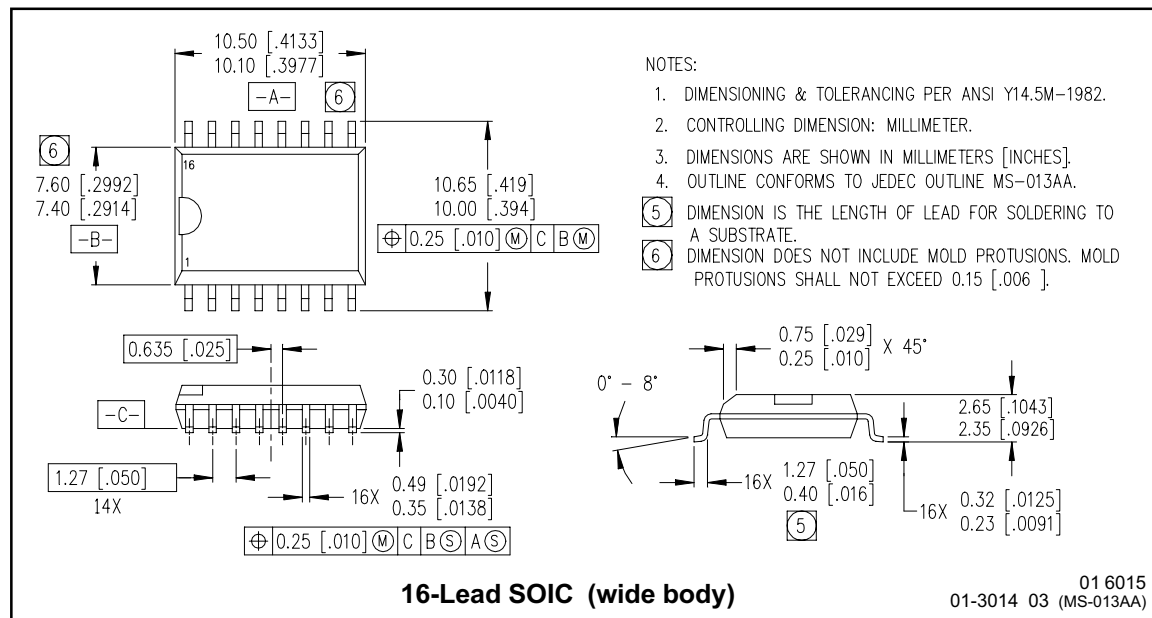
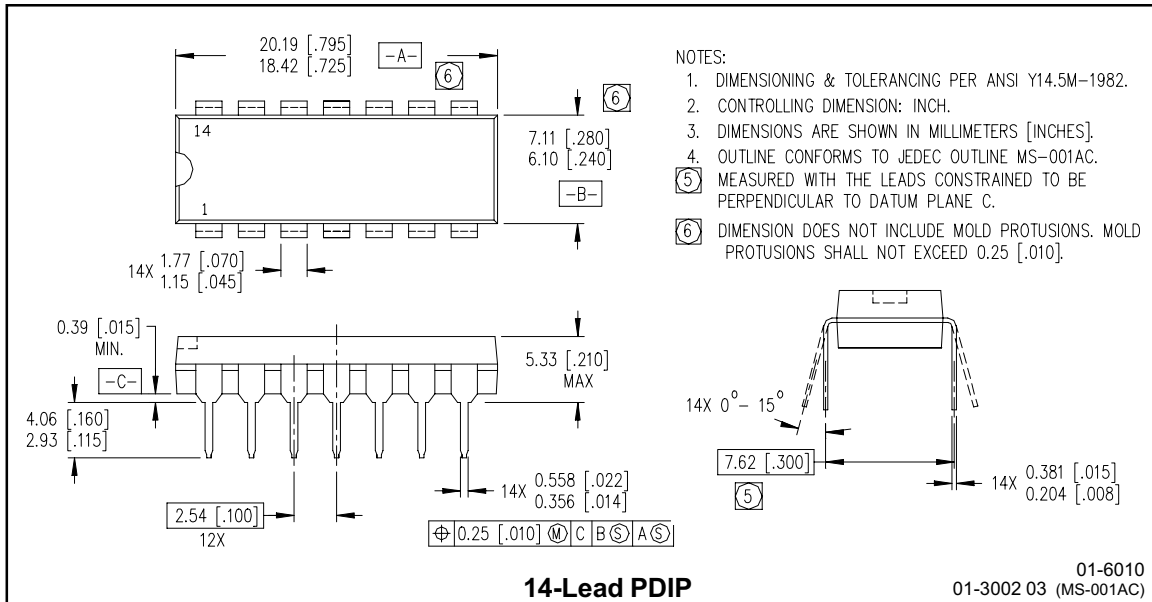


Figure 31. IR213 vs. Frequency (IRFBC50)  
 $R_{gate}=10\Omega, V_{CC}=15V$

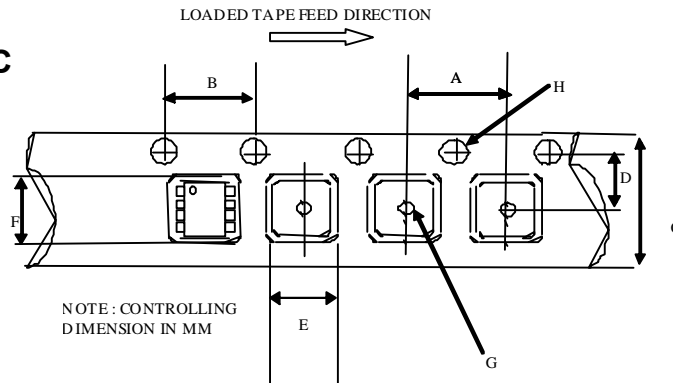
## Case outlines



# IR2213(S) & (PbF)

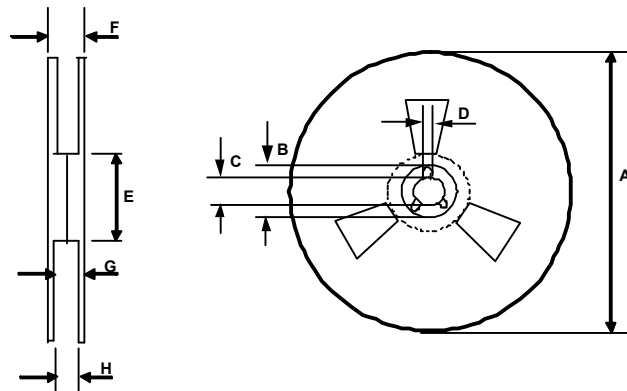
International  
**IR** Rectifier

## Tape & Reel 16-Lead SOIC



CARRIER TAPE DIMENSION FOR 16SOICW

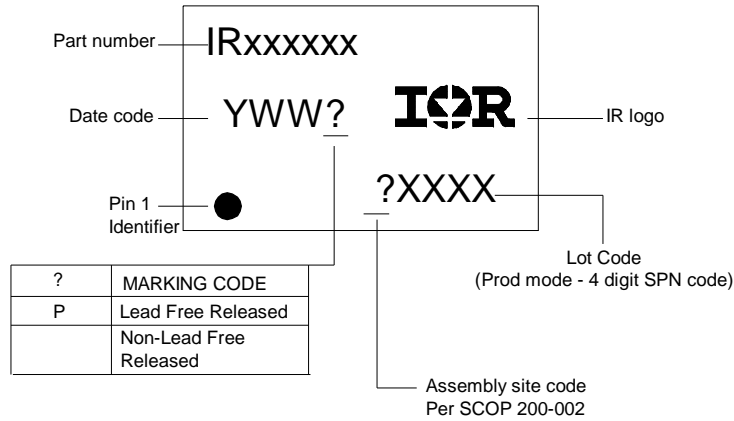
| Code | Metric |       | Imperial |       |
|------|--------|-------|----------|-------|
|      | Min    | Max   | Min      | Max   |
| A    | 11.90  | 12.10 | 0.468    | 0.476 |
| B    | 3.90   | 4.10  | 0.153    | 0.161 |
| C    | 15.70  | 16.30 | 0.618    | 0.641 |
| D    | 7.40   | 7.60  | 0.291    | 0.299 |
| E    | 10.80  | 11.00 | 0.425    | 0.433 |
| F    | 10.60  | 10.80 | 0.417    | 0.425 |
| G    | 1.50   | n/a   | 0.059    | n/a   |
| H    | 1.50   | 1.60  | 0.059    | 0.062 |



REEL DIMENSIONS FOR 16SOICW

| Code | Metric |        | Imperial |        |
|------|--------|--------|----------|--------|
|      | Min    | Max    | Min      | Max    |
| A    | 329.60 | 330.25 | 12.976   | 13.001 |
| B    | 20.95  | 21.45  | 0.824    | 0.844  |
| C    | 12.80  | 13.20  | 0.503    | 0.519  |
| D    | 1.95   | 2.45   | 0.767    | 0.096  |
| E    | 98.00  | 102.00 | 3.858    | 4.015  |
| F    | n/a    | 22.40  | n/a      | 0.881  |
| G    | 18.50  | 21.10  | 0.728    | 0.830  |
| H    | 16.40  | 18.40  | 0.645    | 0.724  |

## LEADFREE PART MARKING INFORMATION



## ORDER INFORMATION

### Basic Part (Non-Lead Free)

- 14-Lead PDIP IR2213 order IR2213
- 16-Lead SOIC IR2213S order IR2213S
- 16-Lead SOIC Tape & Reel order IR2213STR

### Leadfree Part

- 14-Lead PDIP IR2213 order IR2213PbF
- 16-Lead SOIC IR2213S order IR2213SPbF
- 16-Lead SOIC Tape & Reel order IR2213STRPbF