



# STT1NF100

## N-CHANNEL 100V - 0.7Ω - 1A SOT23-6L STripFET™ II POWER MOSFET

PRELIMINARY DATA

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STT1NF100	100V	<0.8Ω	1A

- TYPICAL R<sub>DS(on)</sub> = 0.7Ω
- EXCEPTIONAL dv/dt CAPABILITY
- VERY LOW Q<sub>g</sub>

### DESCRIPTION

This Power MOSFET is the latest development of ST-Microelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

### APPLICATIONS

- DC-DC & DC-AC CONVERTERS
- DC MOTOR CONTROL (DISK DRIVES, etc.)
- SYNCHRONOUS RECTIFICATION

### MARKING

- STQ0

### ABSOLUTE MAXIMUM RATINGS

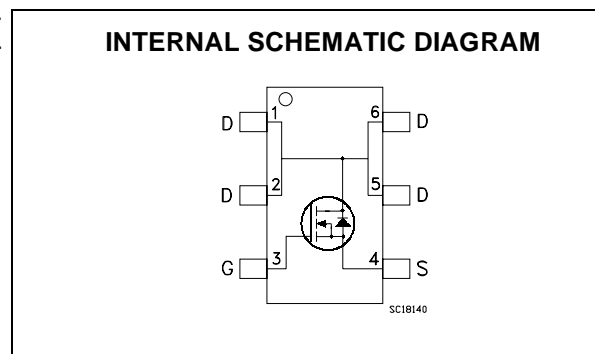
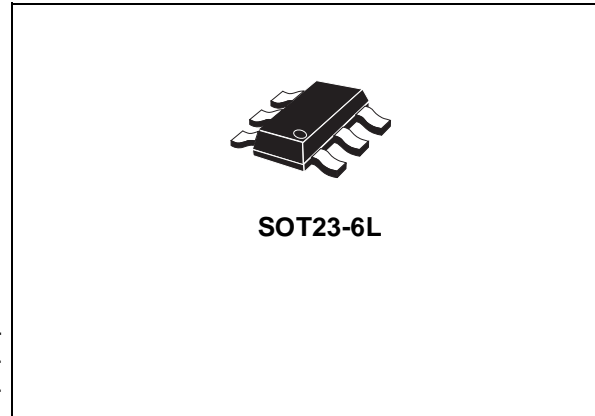
Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	100	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	100	V
V <sub>GS</sub>	Gate- source Voltage	± 20	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	1	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	0.6	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	4	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	1.6	W
	Derating Factor	0.013	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	20	V/ns
T <sub>stg</sub>	Storage Temperature	- 55 to 150	°C
T <sub>j</sub>	Max. Operating Junction Temperature		

(●) Pulse width limited by safe operating area

(1) I<sub>SD</sub> ≤ 1A, di/dt ≤ 350A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>.

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### THERMAL DATA

Rthj-amb(*)	Thermal Resistance Junction-ambient Max	78	°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose	260	°C

(\*) When mounted on FR-4 board of 1inch<sup>2</sup> pad, 0.5oz Cu

### ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	100			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2			V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 0.5 A		0.7	0.8	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> = 15V, I <sub>D</sub> = 1A		1		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		105		pF
C <sub>oss</sub>	Output Capacitance			20		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			9		pF

**ELECTRICAL CHARACTERISTICS (CONTINUED)****SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 50V, I_D = 0.5A$		4		ns
$t_r$	Rise Time	$R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 1)		5.5		ns
$Q_g$	Total Gate Charge	$V_{DD} = 50V, I_D = 1A,$		4	6	nC
$Q_{gs}$	Gate-Source Charge	$V_{GS} = 10V$		1		nC
$Q_{gd}$	Gate-Drain Charge	(see test circuit, Figure 2)		1.5		nC

**SWITCHING OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 50V, I_D = 0.5A,$		13		ns
$t_f$	Fall Time	$R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 1)		6.5		ns

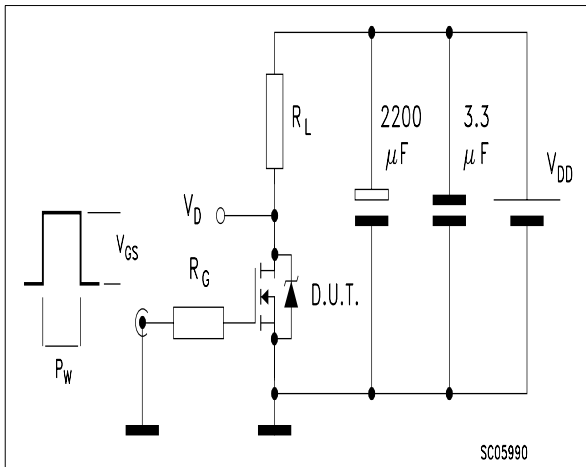
**SOURCE DRAIN DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				1	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				4	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 1A, V_{GS} = 0$			1.2	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 1A, di/dt = 100A/\mu s,$		45		ns
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 20V, T_j = 150^\circ C$		60		nC
$I_{RRM}$	Reverse Recovery Current	(see test circuit, Figure 3)		2.7		A

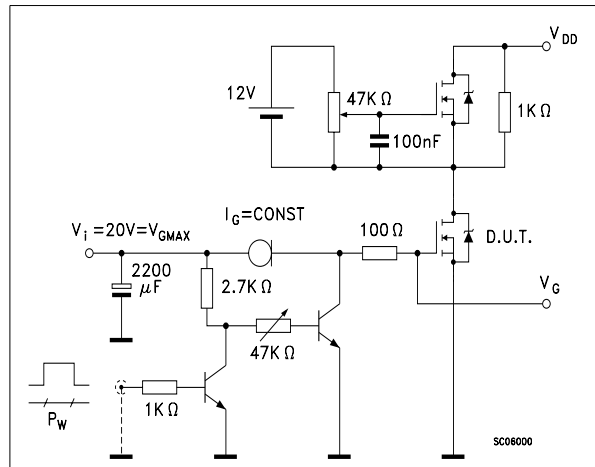
Note: 1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

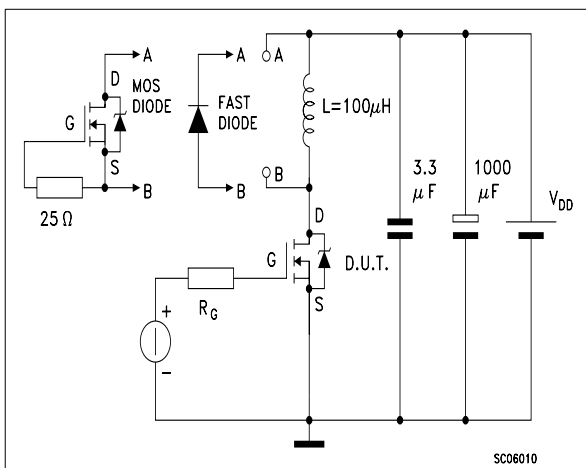
**Fig. 1: Switching Times Test Circuit For Resistive Load**



**Fig. 2: Gate Charge test Circuit**

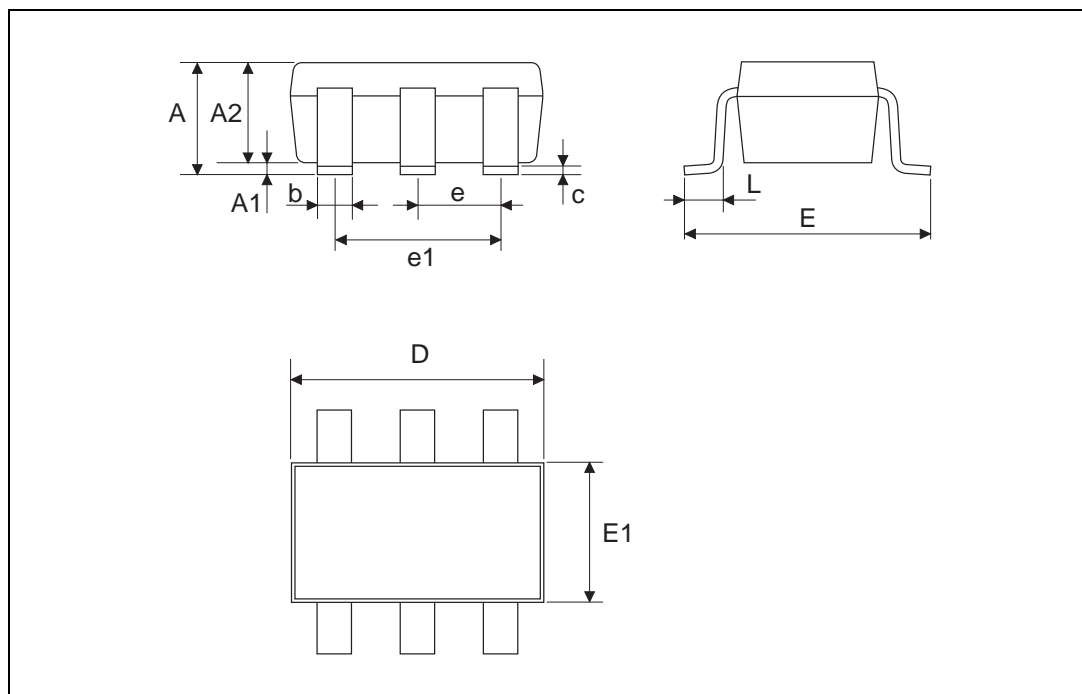


**Fig. 3: Test Circuit For Diode Recovery Behaviour**



<b>TSOP-6 MECHANICAL DATA</b>
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DIM.	mm			mils		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.90		1.45	0.035		0.057
A1	0.00		0.15	0.000		0.006
A2	0.90		1.30	0.035		0.051
b	0.25		0.50	0.010		0.020
C	0.09		0.20	0.004		0.008
D	2.80		3.10	0.110		0.122
E	2.60		3.00	0.102		0.118
E1	1.50		1.75	0.059		0.069
L	0.35		0.55	0.014		0.022
e		0.95			0.037	
e1		1.90			0.075	



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