ADVANCED INFORMATION

CY7C1020V

32K x 16 Static RAM

Features

- **3.3V operation (3.0V–3.6V)**
- **High speed**
  - **— t_{AA} = 12 ns**
- **Low active power**
  - **— 540mW (max.)**
- **Low standby power**
  - **— 3.6mW (max.)**
- **Automatic power-down when deselected**
- **Independent Control of Upper and Lower bytes**
- **Available in 44-pin TSOP II and 400-mil SOJ**

Functional Description

The CY7C1020V is a high-performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

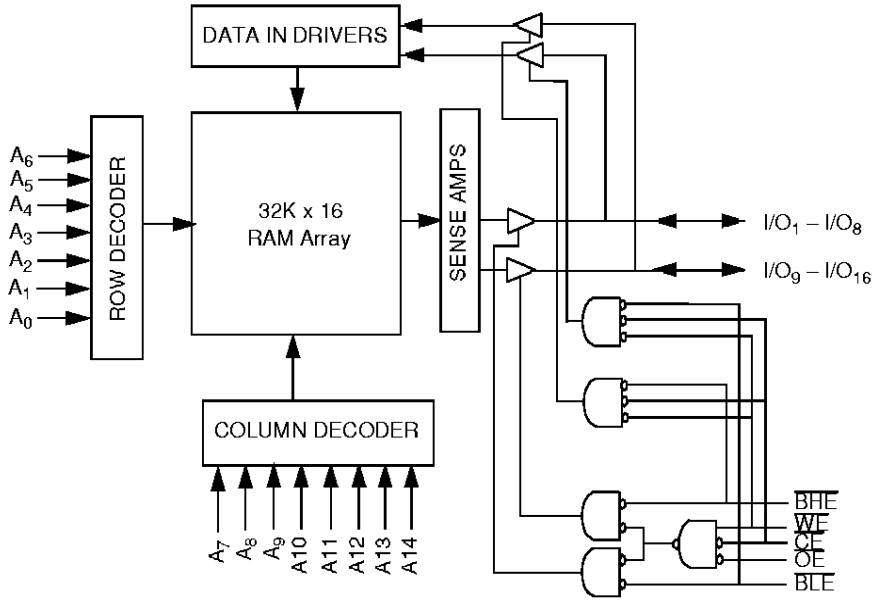
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. If byte low enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_1 through I/O_8), is written into the location specified on the address pins (A_0 through A_{14}). If byte high enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_9 through I/O_{16}) is written into the location specified on the address pins (A_0 through A_{14}).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while forcing the write enable ($\overline{WE}$) HIGH. If byte low enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_1 to I/O_8. If byte high enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_9 to I/O_{16}. See the truth table at the back of this datasheet for a complete description of read and write modes.

The input/output pins (I/O_1 through I/O_{16}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1020V is available in standard 44-pin TSOP type II 400-mil-wide SOJ packages.

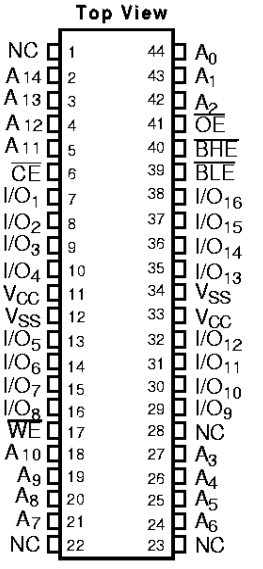
Logic Block Diagram



Pin Configuration

SOJ / TSOP II

Top View



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Selection Guide

	7C1020V-12	7C1020V-15	7C1020V-20	7C1020V-25
Maximum Access Time (ns)	12	15	20	25
Maximum Operating Current (mA)	150	140	130	130
Maximum CMOS Standby Current (mA)	1	1	1	1