

# N-channel enhancement mode MOS transistor

## BSH104

### FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.
- Very low threshold.

### APPLICATIONS

- 'Glue-logic': interface between logic blocks and/or periphery
- Power management
- DC to DC converters
- General purpose switch
- Battery powered applications.

### DESCRIPTION

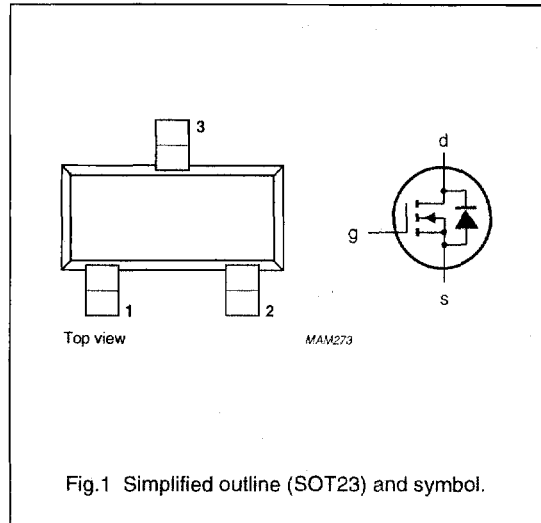
N-channel enhancement mode MOS transistor in a SOT23 SMD package.

#### CAUTION

The device is supplied in an antistatic package.  
The gate-source input must be protected against static discharge during transport or handling.

### PINNING

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain



### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage (DC)		–	12	V
$V_{SD}$	source-drain diode forward voltage	$V_{GD} = 0$ ; $I_S = 0.5$ A	–	1	V
$V_{GS}$	gate-source voltage (DC)		–	$\pm 8$	V
$V_{GSth}$	gate-source threshold voltage	$V_{DS} = V_{GS}$ ; $I_D = 1$ mA	0.4	–	V
$I_D$	drain current (DC)	$T_s = 80$ °C	–	1.1	A
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 2.5$ V; $I_D = 0.65$ A	–	0.3	$\Omega$
$P_{tot}$	total power dissipation	$T_s = 80$ °C	–	0.5	W

# N-channel enhancement mode MOS transistor

BSH104

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage (DC)		–	12	V
$V_{GS}$	gate-source voltage (DC)		–	±8	V
$I_D$	drain current (DC)	$T_s = 80\text{ °C}$ ; note 1	–	1.1	A
$I_{DM}$	peak drain current	note 2	–	4.5	A
$P_{tot}$	total power dissipation	$T_s = 80\text{ °C}$	–	0.5	W
		$T_{amb} = 25\text{ °C}$ ; note 3	–	0.75	W
		$T_{amb} = 25\text{ °C}$ ; note 4	–	0.54	W
$T_{stg}$	storage temperature		–55	+150	°C
$T_j$	operating junction temperature		–55	+150	°C
<b>Source-drain diode</b>					
$I_S$	source current (DC)	$T_s = 80\text{ °C}$	–	0.5	A
$I_{SM}$	peak pulsed source current	note 2	–	2	A

**Notes**

- $T_s$  is the temperature at the soldering point of the drain lead.
- Pulse width and duty cycle limited by maximum junction temperature.
- Device mounted on a printed-circuit board with a  $R_{th\ a\text{-tp}}$  (ambient to tie-point) of 27.5 K/W.
- Device mounted on a printed-circuit board with a  $R_{th\ a\text{-tp}}$  (ambient to tie-point) of 90 K/W.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-s}}$	thermal resistance from junction to soldering point	140	K/W

# N-channel enhancement mode MOS transistor

BSH104

**CHARACTERISTICS** $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0; I_D = 10\text{ }\mu\text{A}$	12	–	–	V
$V_{GSth}$	gate-source threshold voltage	$V_{GS} = V_{DS}; I_D = 1\text{ mA}$	0.4	–	–	V
$I_{DSS}$	drain-source leakage current	$V_{GS} = 0; V_{DS} = 9.6\text{ V}$	–	–	100	nA
$I_{GSS}$	gate leakage current	$V_{DS} = 0; V_{GS} = \pm 8\text{ V}$	–	–	$\pm 100$	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 0.65\text{ A}$	–	–	0.23	$\Omega$
		$V_{GS} = 2.5\text{ V}; I_D = 0.65\text{ A}$	–	–	0.3	$\Omega$
		$V_{GS} = 1.8\text{ V}; I_D = 0.32\text{ A}$	–	–	0.4	$\Omega$
$C_{iss}$	input capacitance	$V_{GS} = 0; V_{DS} = 9.6\text{ V}; f = 1\text{ MHz}$	–	t.b.f.	–	pF
$C_{oss}$	output capacitance	$V_{GS} = 0; V_{DS} = 9.6\text{ V}; f = 1\text{ MHz}$	–	t.b.f.	–	pF
$C_{rss}$	reverse transfer capacitance	$V_{GS} = 0; V_{DS} = 9.6\text{ V}; f = 1\text{ MHz}$	–	t.b.f.	–	pF
$Q_G$	total gate charge	$V_{GS} = 6\text{ V}; V_{DD} = 6\text{ V}; I_D = 0.65\text{ A}; T_{amb} = 25\text{ }^\circ\text{C}$	–	t.b.f.	–	pC
$Q_{GS}$	gate-source charge	$V_{DD} = 6\text{ V}; I_D = 0.65\text{ A}; T_{amb} = 25\text{ }^\circ\text{C}$	–	t.b.f.	–	pC
$Q_{GD}$	gate-drain charge	$V_{DD} = 6\text{ V}; I_D = 0.65\text{ A}; T_{amb} = 25\text{ }^\circ\text{C}$	–	t.b.f.	–	pC
<b>Switching times</b>						
$t_{d(on)}$	turn-on delay time	$V_{GS} = 0\text{ to }6\text{ V}; V_{DD} = 6\text{ V}; I_D = 0.65\text{ A}; R_{gen} = 6\text{ }\Omega$	–	t.b.f.	–	ns
$t_f$	fall time	$V_{GS} = 0\text{ to }6\text{ V}; V_{DD} = 6\text{ V}; I_D = 0.65\text{ A}; R_{gen} = 6\text{ }\Omega$	–	t.b.f.	–	ns
$t_{on}$	turn-on switching time	$V_{GS} = 0\text{ to }6\text{ V}; V_{DD} = 6\text{ V}; I_D = 0.65\text{ A}; R_{gen} = 6\text{ }\Omega$	–	t.b.f.	–	ns
$t_{d(off)}$	turn-off delay time	$V_{GS} = 6\text{ to }0\text{ V}; V_{DD} = 6\text{ V}; I_D = 0.65\text{ A}; R_{gen} = 6\text{ }\Omega$	–	t.b.f.	–	ns
$t_r$	rise time	$V_{GS} = 6\text{ to }0\text{ V}; V_{DD} = 6\text{ V}; I_D = 0.65\text{ A}; R_{gen} = 6\text{ }\Omega$	–	t.b.f.	–	ns
$t_{off}$	turn-off switching time	$V_{GS} = 6\text{ to }0\text{ V}; V_{DD} = 6\text{ V}; I_D = 0.65\text{ A}; R_{gen} = 6\text{ }\Omega$	–	t.b.f.	–	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain diode forward voltage	$V_{GD} = 0; I_S = 0.5\text{ A}$	–	–	1	V
$t_{rr}$	reverse recovery time	$I_S = 0.5\text{ A}; di/dt = -100\text{ A}/\mu\text{s}$	–	t.b.f.	–	ns