Features

- Dual 6-bit Resolution
- 700 MHz Full-power Input Bandwidth (-3 dB)
- Band Flatness (±0.5 dB) from DC to 350 MHz
- 1 Gsps Sampling Rate
- SINAD = 35 dB Typ (5.7 ENOB)
  - THD = -47 dB, SFDR = -48 dB at F_S = 1 Gsps, F_{IN} = 250 MHz, (SFSR = -0.5dB FS)
- 2-tone IMD: -47 dBc Min at 1 Gsps, F_{IN} = 249 MHz, 251 MHz
- DNL = 0.35 LSB Typ, INL = 0.5 LSB Typ
- Channel-to-channel Input Offset Error: ±1 LSB Max, 0 LSB Typ
- Gain Matching (Channel-to-channel): ±0.25 dB Max, 0 dB Typ
- Phase Matching (Channel-to-channel): ±2 deg Max, 0 deg typ
- Channel-to-channel Mean Difference Error: 0.5 LSB (rms)
- Channel-to-channel Max Difference Error: ±2 LSB Typ
- Low Bit Error Rate (10^{-9}) at 1 Gsps
- Very Low Input Capacitance: 1 pF
- 800 mV_{PP} Differential or Single Analog Inputs
- Differential or Single-ended 50Ω PECL-compatible Clock Inputs
- LVDS Output Compatibility (100Ω)
- 1:2 Data Output Demultiplexer per ADC
- LOW Power Consumption:
  - 700 mW at V_{CCA} = V_{CCD} = 3.15V/V_{CCO} = 2.25V
- Power Supply: 3.15V (Analog), 3.15V (Digital), 2.25V (Output)
- Available in 80-lead TQFP Package
- Temperature Range:
  - Industrial -20°C < T_A < 85°C,
  - Commercial 0°C < T_A < 70°C

Applications

- Satellite Receiver
- Direct RF Down-conversion
- Test Instrumentation
- WLAN

Description

The AT76CL610 is a monolithic dual 6-bit analog-to-digital converter, designed for digitizing in-phase (I) and quadrature (Q) wide bandwidth analog signals at very high sampling rates of up to 1 Gsps (giga-samples per second). The ability to directly interface I and Q signals makes the AT76CL610 ideal for use in applications such as direct satellite demodulation.

The AT76CL610 uses an innovative architecture and is fabricated with an advanced high-speed BiCMOS process.

The two on-chip ADC cores have a closely matched 700 MHz full-power input bandwidth, providing excellent dynamic performance in undersampling applications (high IF digitizing).

The samples from each A/D converter are de-multiplexed by a 1:2 ratio and the output data stream is LVDS-compliant.

Dual ADC 6-bit 1 Gsps Converter

AT76CL610

Preliminary Specification

For more information, please contact hotline-bdc@gfo.atmel.com

Rev. 2158A–BDC–04/03

Figure 1. AT76CL610 Symbol

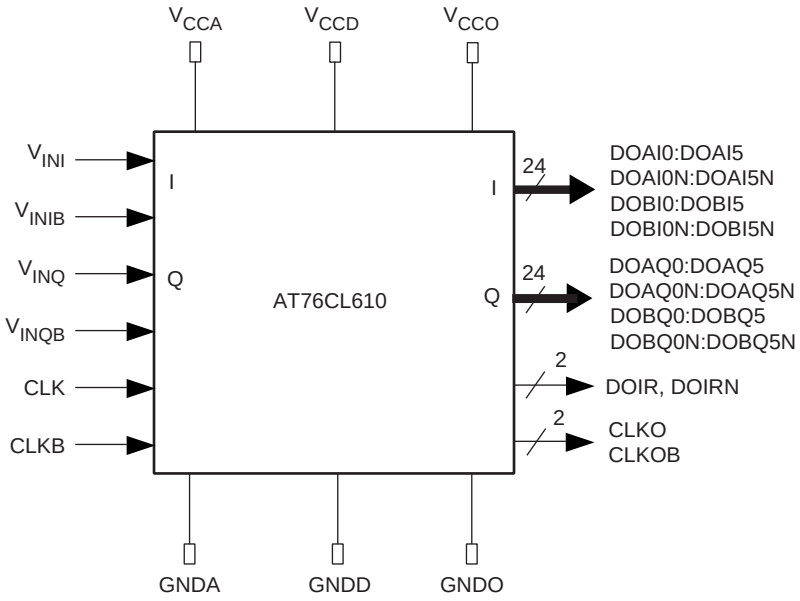


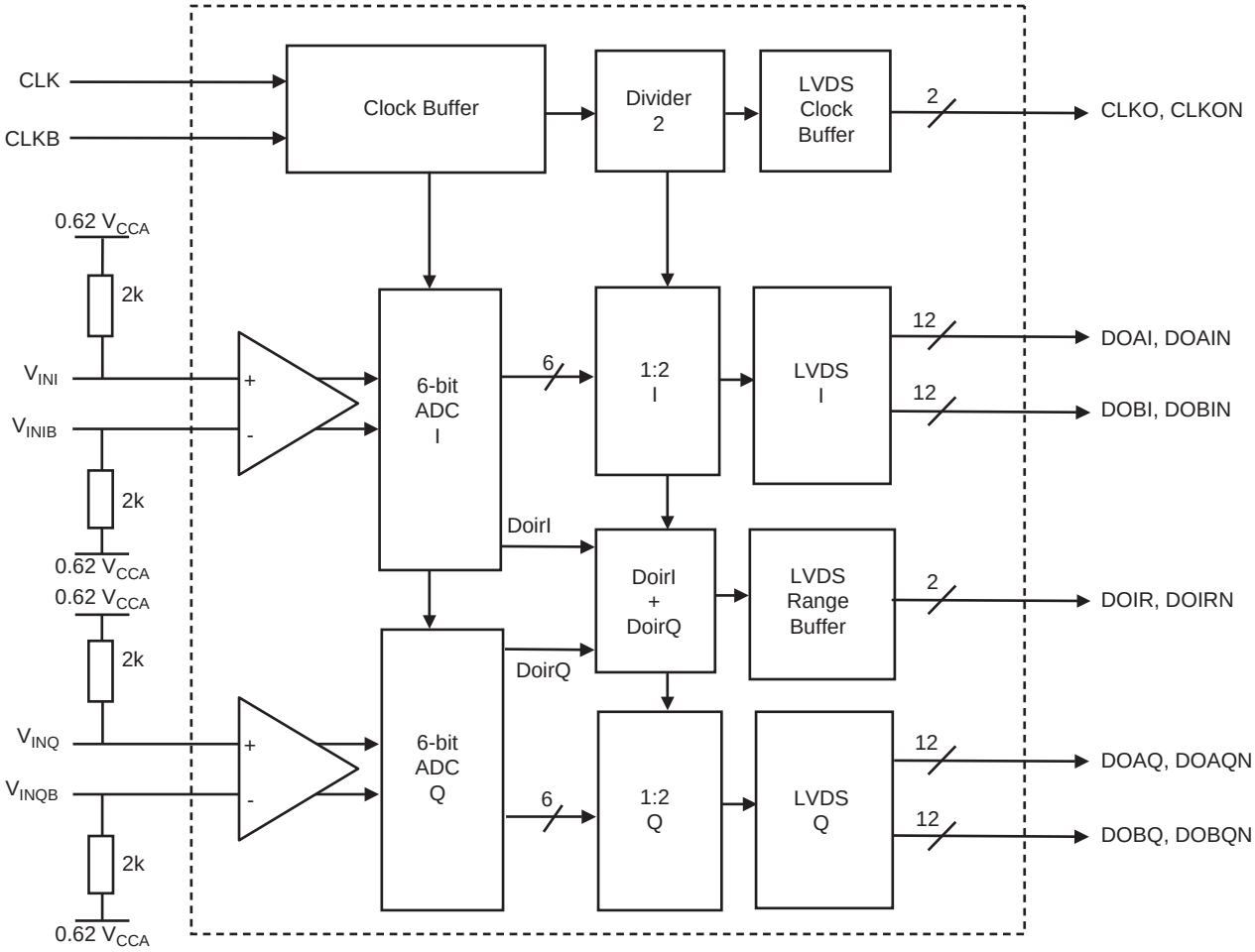
Table 1. Signal Description

Signal Name	Function	Direction
V_{CCA}	Positive analog power supply	I
V_{CCD}	Positive digital power supply	I
V_{CCO}	Positive output power supply	I
GNDA	Analog ground	I
GNDD	Digital ground	I
GNDO	Output ground	I
V_{INI}, V_{INIB}	Differential analog inputs I	I
V_{INQ}, V_{INQB}	Differential analog inputs Q	I
CLK, CLKB	Differential clock inputs	I
CLKO, CLKOB	Differential clock outputs	O
DOAI0:DOAI5; DOAI0N:DOAI5N DOBI0:DOBI5; DOBI0N:DOBI5N	Differential output data port Channel I	O
DOAQ0:DOAQ5; DOAQ0N:DOAQ5N DOBQ0:DOBQ5; DOBQ0N:DOBQ5N	Differential output data port Channel Q	O
DOIR, DOIRN	Combined (I and Q) output in range data	O

Table 2. Digital Output Coding

Differential or Single Analog Input	Voltage Level	Digital Output I or Q Binary	Out of Range
> +406 mV	> Positive full scale + 1/2 LSB	111111	1
+406 mV	Positive full scale + 1/2 LSB	111111	0
+393 mV	Positive full scale - 1/2 LSB	111111	0
+206 mV	Positive 1/2 scale + 1/2 LSB	110000	0
+193 mV	Positive 1/2 scale - 1/2 LSB	101111	0
+6.25 mV	Bipolar zero + 1/2 LSB	100000	0
-6.25 mV	Bipolar zero - 1/2 LSB	011111	0
-206 mV	Negative 1/2 scale + 1/2 LSB	010000	0
-193 mV	Negative 1/2 scale - 1/2 LSB	001111	0
-393 mV	Negative full scale + 1/2 LSB	000000	0
-406 mV	Negative full scale - 1/2 LSB	000000	0
<-406 mV	< Negative full scale - 1/2 LSB	000000	1

Figure 2. AT76CL610 Simplified Block Diagram



Functional Description

The AT76CL610 is a dual 6-bit, 1 Gsps ADC based on an advanced high-speed BiCMOS technology.

Each ADC has a 6-bit Flash-like core architecture. The output data is followed by a 1:2 demultiplexer and LVDS output buffer (100Ω).

A common over-range combiner (DOIR = DOIRI + DOIRQ) is provided for external gain control adjustment.

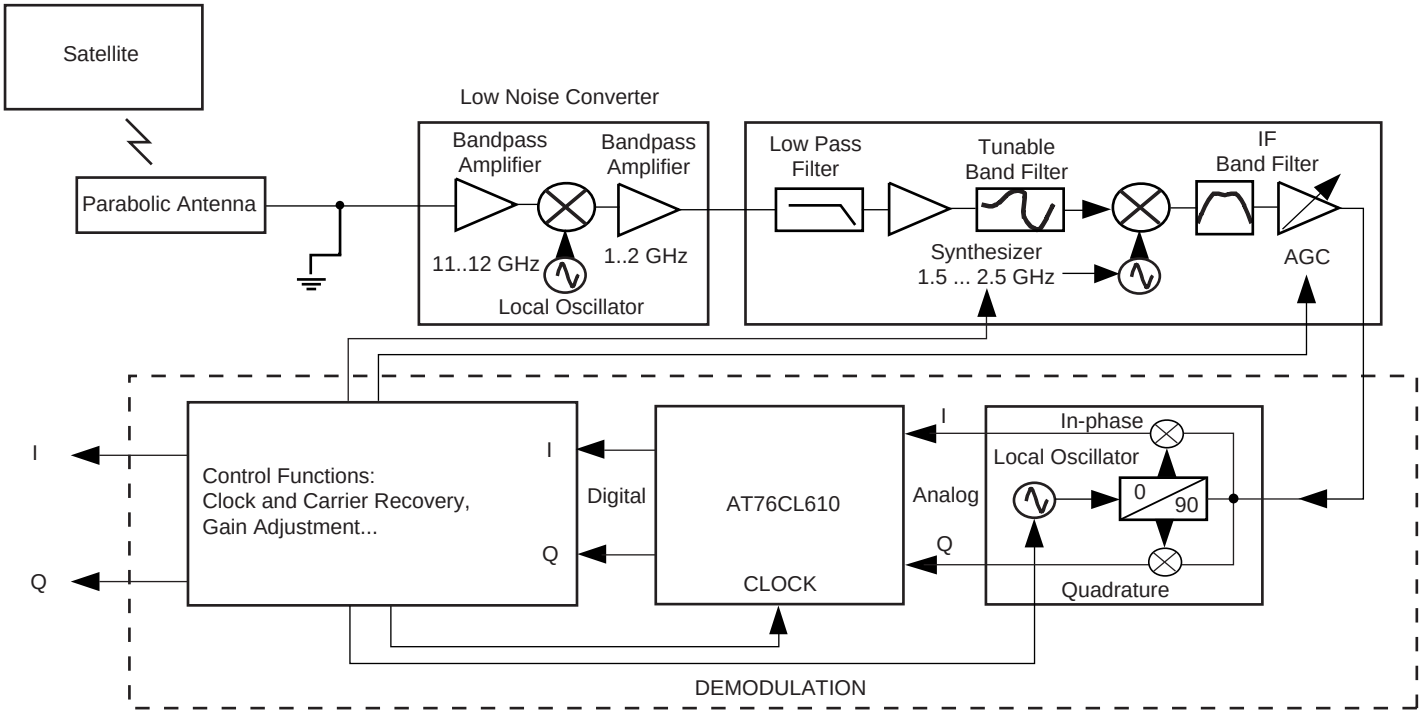
The AT76CL610 works in fully differential mode from analog inputs to digital outputs.

The AT76CL610 features a full-power input bandwidth of 700 MHz.

Application Scenario

Figure 3 shows the AT76CL610 integrated into a typical application scenario for digital signal reception and demodulation.

Figure 3. Functional Application (Typical)



Electrical Characteristics

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CCA}	Analog positive supply voltage	GND to 6	V
V_{CCD}	Digital positive supply voltage	GND to 6	V
Vcco	Output supply voltage	GND to 6	V
DV_{CCA} to V_{CCO}	Maximum difference between V_{CCA} and V_{CCO}	2.4	V
DV_{CCA} to V_{CCD}	Maximum difference between V_{CCA} and V_{CCD}	0.8	V
DV_{CCD} to V_{CCO}	Maximum difference between V_{CCD} and V_{CCO}	1.6	V
V_{INI} - V_{INIB} V_{INQ} - V_{INQB}	Differential analog input voltages	2	V_{PP}
V_{CLK} or V_{CLKB}	Clock input voltage	-0.3 to V_{CCD} + 0.3	V
V_{CLK} - V_{CLKB}	Maximum difference between V_{CLK} and V_{CLKB}	2	V_{PP}
T_J	Maximum junction temperature	+125	°C
T_{STG}	Storage temperature	-65 to +150	°C
T_{LEADS}	Lead temperature (Soldering 10s)	+300	°C

Notes: 1. Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum ratings may affect device reliability.

2. Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). These are stress ratings only and operation of the device at these or at any other conditions above those given in the Electrical Characteristics sections of the specifications is not implied. Exposure to limiting values for extended periods may affect device reliability.

Table 4. Recommended Conditions of Use

Symbol	Parameter	Min	Typ	Max	Unit
V_{CCA}	Analog supply voltage	3.0	3.15	3.3	V
V_{CCD}	Digital supply voltage	3.0	3.15	3.3	V
V_{CCO}	Output supply voltage	2.0	2.25	3.3	V
V_{INI} - V_{INIB} or V_{INQ} - V_{INQB}	Differential or single analog input voltage (full scale)	750	800	850	mV_{PP}
V_{CLK} - V_{CLKB}	Clock input level differential		500		mV_{PP}
T_A	Ambient temperature range	$0 < T_A < 70$ ("C" grade) $-20 < T_A < 85$ ("V" grade)			°C

Operating Characteristics

The following conditions apply to the electrical operating characteristics given in Table 5. The test levels are given in Table 6 on page 10.

V_{CCA} = 3.15V, V_{CCD} = 3.15V, V_{CCO} = 2.25V, V_{INI} - V_{INIB} or V_{INQ} - V_{INQB} = 800 mV_{PP}

-0.5 dB full scale differential input (digital outputs LVDS 100Ω), 50% clock duty cycle

T_A (typical) = 25°C

Table 5. Electrical Operating Characteristics

Symbol	Parameter	Test Level	Min	Typ	Max	Unit
Power Requirements						
V_{CCA}	Power supply voltage analog	I	3.0	3.15	3.3	V
V_{CCD}	Power supply voltage digital	I	3.0	3.15	3.3	V
V_{CCO}	Power supply voltage output digital (LVDS)	I	2.0	2.25	3.3	V
I_{CCA}	Supply current analog	I		52	60	mA
I_{CCD}	Supply current digital	I		110	130	mA
I_{CCO}	Supply current output	I		100	110	mA
PD	Nominal power dissipation	I		700	850	mW
PSRR	Single channel power supply rejection ratio (V_{CCA})	III		TBF		dB
	Resolution			6		bits
Analog Inputs						
V_{INI} or V_{INQ}	Full scale input voltage range (differential mode) 0.62 V_{CCA} common mode voltage	III	750	800	850	mV
V_{INIB} or V_{INQB}	Full scale input voltage range (single mode) 0.62 V_{CCA} common mode voltage	III	750	800	850	mV
C_{IN}	Analog input capacitance I and Q	II, IV		2		pF
R_{IN}	Input resistance I and Q	I	1.3	2		kΩ
FPBW	Full-power input bandwidth (-3 dB)	III	600	700		MHz
Clock Input						
	Logic compatibility for clock inputs		PECL/ECL/LVDS			
V_{IL} - V_{ILh}	Differential logic level	IV		300		mV
	Power level into 50Ω termination		dBm into 50Ω			
	Clock input power level	III	-10	-6	-4	dBm
C_{CLK}	Clock input capacitance	II		2		pF
Digital Outputs						
	Logic compatibility for digital outputs (depending on the value of V_{CCO})		LVDS			
V_{OD}	Differential output voltages swings (assuming V_{CCO} = 2.25V and V_{CCD} = 3.15V)	III, I	250	300	400	mV
	Output Levels (Assuming V_{CCO} = 2.25V and V_{CCD} = 3.15V) 100Ω Differentially Terminated	II				
V_{OL}	Logic 0 voltage	I, III	0.9	1.1	1.2	V

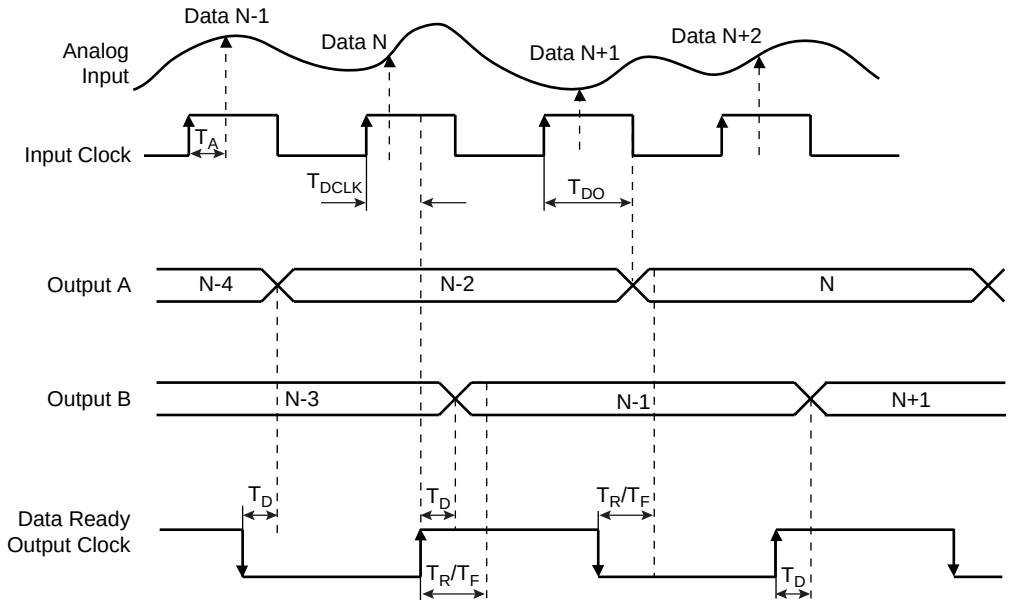
Table 5. Electrical Operating Characteristics (Continued)

Symbol	Parameter	Test Level	Min	Typ	Max	Unit
V_{OH}	Logic 1 voltage	I, III	1.3	1.4	1.47	V
V_{OS}	Output offset voltage (assuming V_{CCO} = 2.25V and V_{CCD} = 3.15V) 100Ω differentially terminated	I, III	1125	1200	1275	mV
	Change in V_{OD} between 0 and 1	III			25	mV
	Change in V_{OS} between 0 and 1	III			25	mV
	Output current (shorted output)	III			12	mA
	Output current (grounded output)			Not Allowed		
	Output level drift with temperature	III		1.4		mV/°C
	Differential output amplitude drift with temperature	III		0.16		mV/°C
DC Accuracy Single-ended 50% clock duty cycle (CLK, CLKB); binary output data format. T_A (typical) = 25°C.						
DNL	Differential non-linearity	I, III		0.25	0.35	LSB
INL	Integral non-linearity	I, III		0.35	0.5	LSB
	No missing codes	Guaranteed over specified temperature range				
	Output offset code (single channel I or Q)	I, III	31	31.5	32	LSB
	Input offset voltage (single channel I or Q)	I, III		0.62 x V_{CCA}		V
	Gain error drift against temperature	III		TBF		mV/°C
	Gain error drift against analog supply	III		TBF		mV/V°
	Input offset matching channel I or Q (static)	I, III	-1	0	1	LSB
	Gain matching channel I or Q (static)	I, III		0	0.25	dB
Transient Performance						
BER	Bit error rate FS = 1 Gsps, F_{IN} = 250 MHz	III		10^{-9}		Error/ Sample
ORT	Overvoltage recovery time	III		TBD		ns
AC Performance Differential input and clock mode; 50% clock duty cycle (CLK, CLKB); T_A = 25°C, unless otherwise specified.						
SINAD	FS = 1 Gsps, F_{IN} = 10 MHz (single-ended input)	I, III	35	36		dB
	FS = 1 Gsps, F_{IN} = 20 MHz	III	35	36		dB
	FS = 1 Gsps, F_{IN} = 250 MHz	III	34	35		dB
ENOB	FS = 1 Gsps, F_{IN} = 10 MHz (single-ended input)	I, III	5.6	5.8		bits
	FS = 1 Gsps, F_{IN} = 20 MHz	III	5.4	5.75		bits
	FS = 1 Gsps, F_{IN} = 250 MHz	III	5.3	5.70		bits

Table 5. Electrical Operating Characteristics (Continued)

Symbol	Parameter	Test Level	Min	Typ	Max	Unit
THD	FS = 1 Gsps, F_{IN} = 10 MHz (single-ended input)	I, III	-42	-49		dBc
	FS = 1 Gsps, F_{IN} = 20 MHz	III	-42	-49		dBc
	FS = 1 Gsps, F_{IN} = 250 MHz	III	-40	-47		dBc
SFDR	FS = 1 Gsps, F_{IN} = 10 MHz (single-ended input)	I, III	-44	-49		dBc
	FS = 1 Gsps, F_{IN} = 20 MHz	III	-44	-49		dBc
	FS = 1 Gsps, F_{IN} = 250 MHz	III	-40	-48		dBc
IMD	Two-tone inter-modulation distortion (single channel)					
	F_{IN1} = 249 MHz, F_{IN2} = 251 MHz at F_S = 1 Gsps	III		-48		dBc
Gf	Gain flatness: ±0.5 db	III	250	350		MHz
dG	Gain matching (Channel I and Q) F_{IN} = 250 MHz, FS = 1 GHz	III		0	0.25	dB
dΦ	Phase matching (channel I and Q), F_{IN} = 250 MHz, FS = 1 GHz	III	-2	0	2	deg
Cr	Crosstalk channel I versus channel Q, F_{IN} = 250 MHz, FS = 1 GHz	III			<<- 52	dB
Switching Performance and Characteristics – See Figure 4 on page 10						
F_S	Maximum clock frequency	II	1			Gsps
F_S	Minimum clock frequency	II		10		Msps
TC1	Minimum clock pulse width (high)	II	0.400	0.500	50	ns
TC2	Minimum clock pulse width (low)	II	0.400	0.500	50	ns
TA	Aperture delay	II		+350		ps
Jitter	Aperture uncertainty	II		0.4		ps(rms)
Tdclk	Clock output delay between input clock and output clock (50%)	III	tbd	1.03	tbd	ns
Tdo	Data output delay between input clock and data	III	tbd	1.28	tbd	ns
	Data output skew	III		50	100	ps
TR/TF	Output rise/fall time for data ready (10% - 90%) with 7 pF load	III	300	350	500	ps
Td	Data output delay 50% with data ready	III	tbd	250	tbd	ps
Pd	Data pipeline delay		1 for port B 2 for port A			clock cycles

Figure 4. Timing Diagram



Test Levels

Only minimum and maximum values are guaranteed (typical values are issued from characterization results).

Table 6. Test Levels

D	100% wafer tested at +25°C(1)
I	100% production tested at +25°C(1) (for packaged device)
II	Parameter is guaranteed by design
III	Characterization testing: thermal steady-state conditions at specified temperature)
IV	Parameter is a typical value only

Note: 1. Unless otherwise specified, all tests are pulsed tests: therefore $T_J = T_C = T_A$, where T_J, T_C and T_A are junction, case and ambient temperature respectively.

Equivalent Input/Output Schematics

Figure 5. Simplified Input Model for Signal

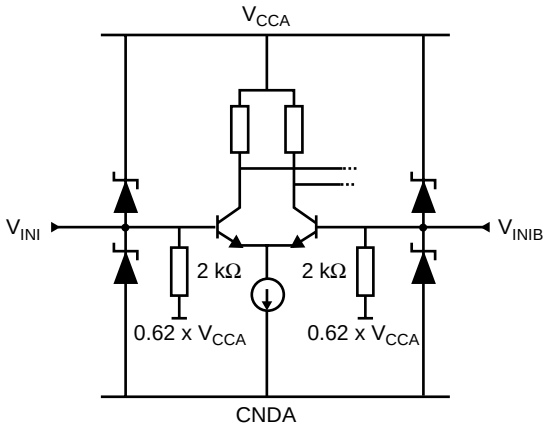


Figure 6. Simplified LVDS Output Model

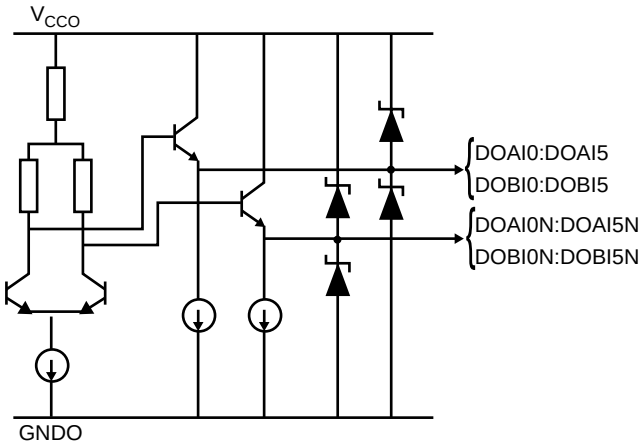
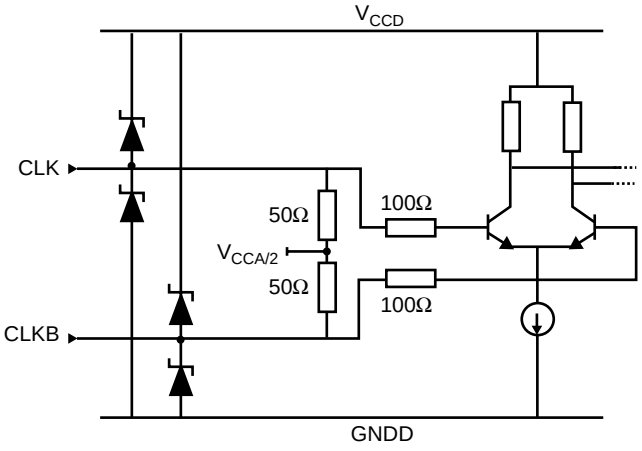


Figure 7. Simplified Input Model for Clock



Applying the AT76CL610

Power Supplies Decoupling, Bypassing and Grounding

Here are the recommended bypassing, decoupling and grounding schemes for the Dual 6-bit 1 Gsps ADC power supplies.

Figure 8. V_{CCD} and V_{CCA} Bypassing and Grounding Scheme

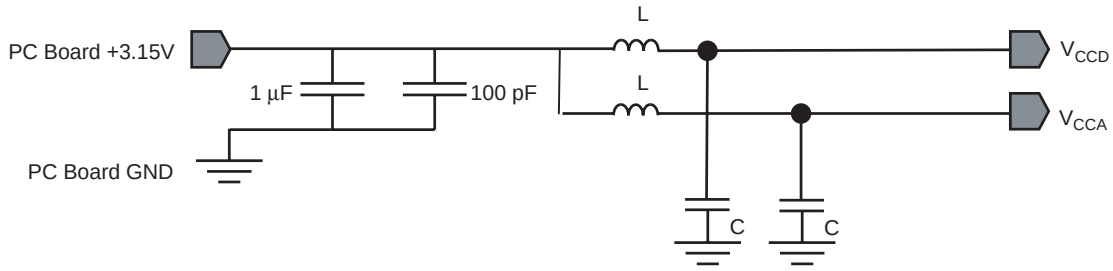


Figure 9. V_{CCO} Bypassing and Grounding Scheme

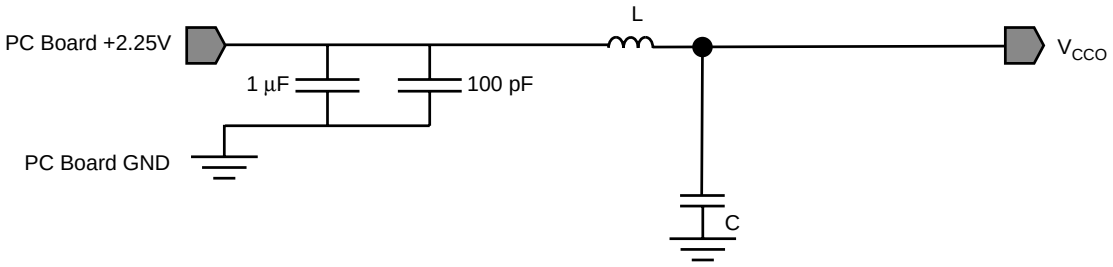
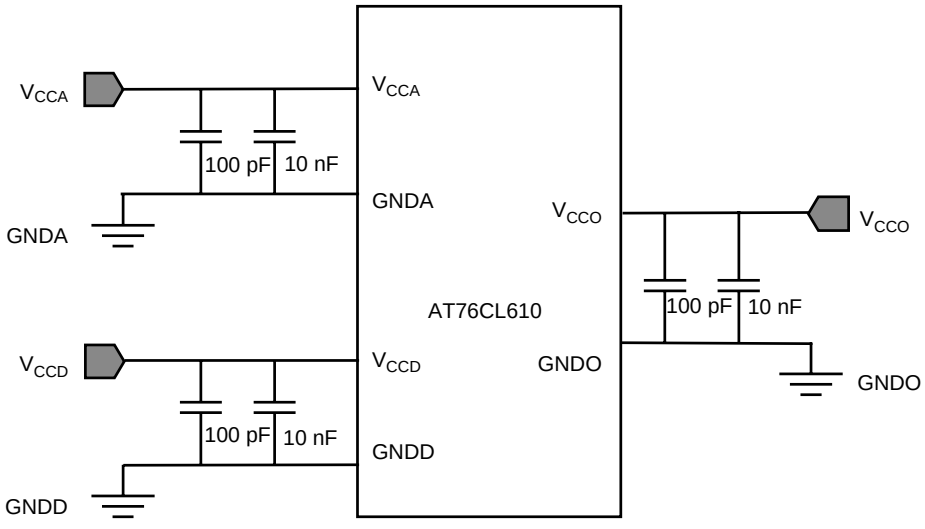


Figure 10. Power Supplies Decoupling Scheme

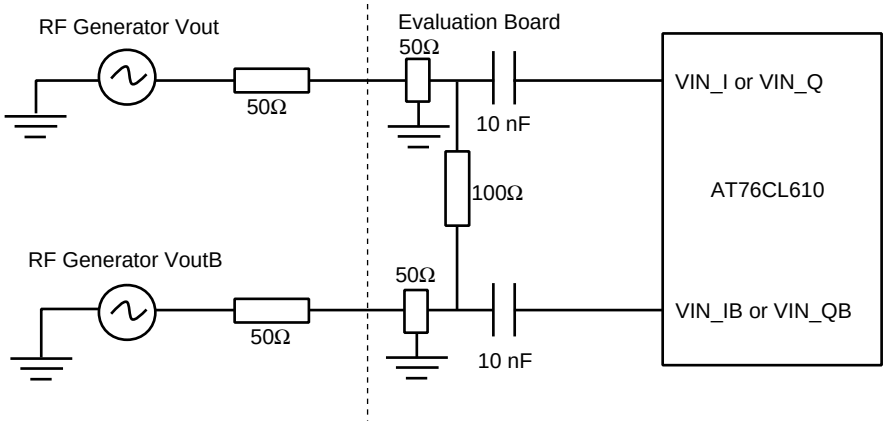


Note: The bypassing capacitors (1 µF and 100 pF) should be placed as close as possible to the board connectors, whereas the decoupling capacitors (100 pF, 10 nF) should be placed as close as possible to the device.

Analog Inputs

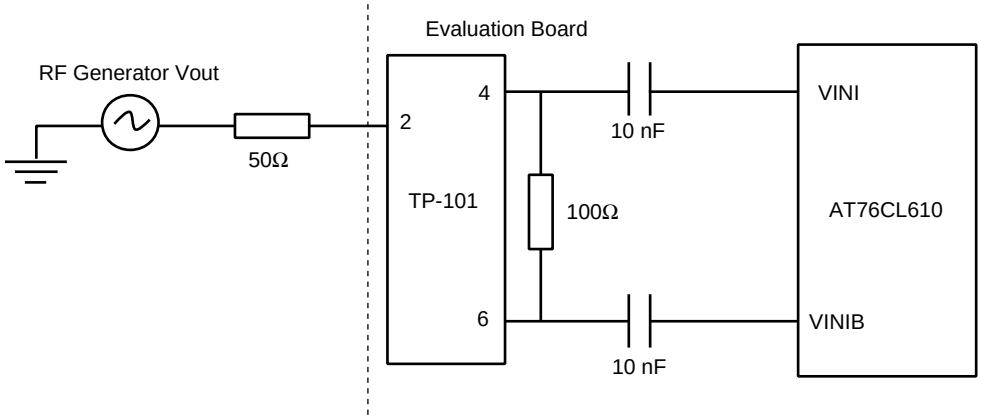
The analog inputs can be entered only in differential mode. A DC decoupling capacitance of 10 nF allows the removal of an input common mode voltage of 0.62 V_{CCA}. A terminal load of 100Ω is located on-board. The analog input resistance of the AT76CL610 is equal to 2 kΩ.

Figure 11. Differential RF Generator and Dual 6-bit Configuration



Note: The user should use an RF generator with a differential output signal or use an external splitter to create a differential signal.

Figure 12. RF Generator Single-ended and Differential Input

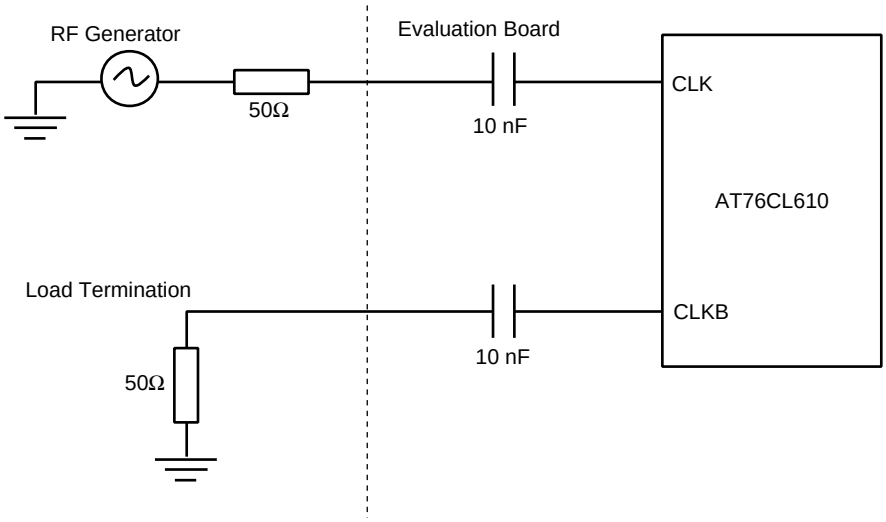


Clock Inputs

The clock inputs can be entered in differential or single-ended mode. Moreover, it is possible for the clock input common mode to be 0V. An AC coupling capacitance (10 nF) can be used to remove the input common mode voltage. It is not necessary to have an on-board 100Ω terminal load as it exists inside the AT76CL610.

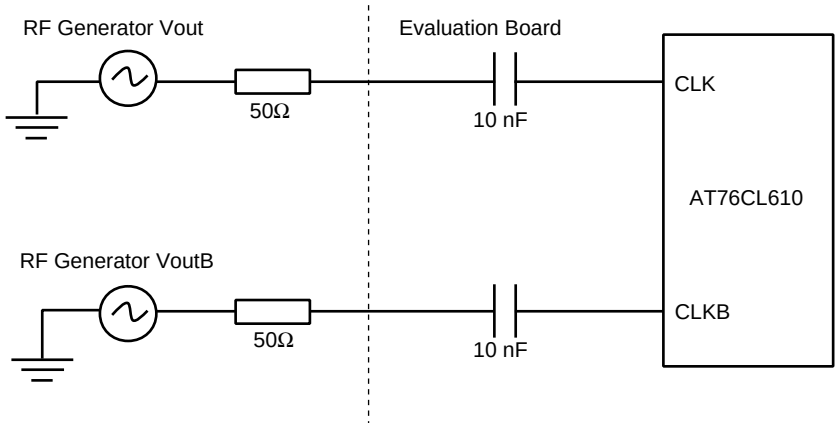
An RF generator is used in single mode for the CLK signal. The CLKBB SMA must be terminated by a 50Ω load.

Figure 13. Single-ended Configuration



An RF generator with a differential output signal for I and Q or an external splitter can also be used in order to create a differential signal.

Figure 14. Input Differential Configuration



2158A–BDC–04/03

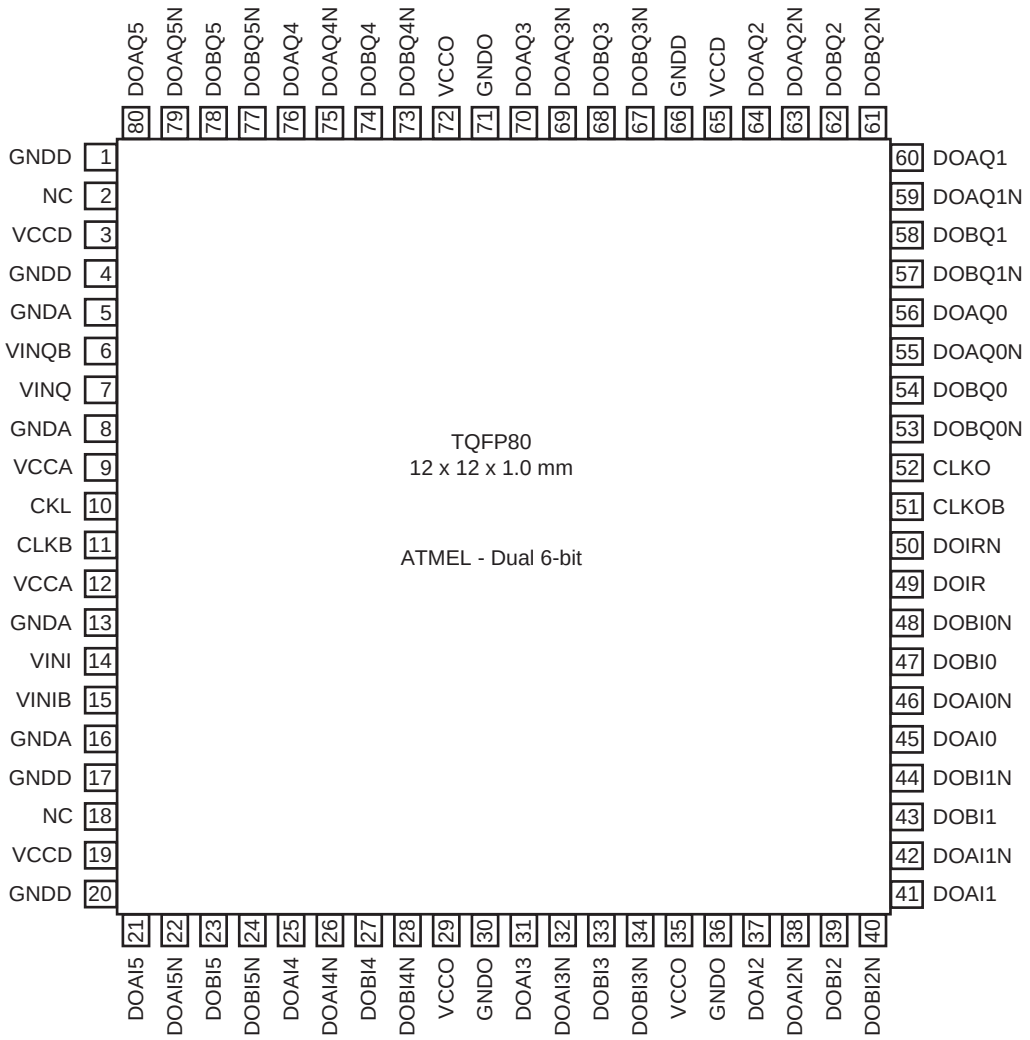
Package Description

80-lead TQFP Pin Description

Table 7. AT76CL610 80-lead TQFP Pin Description

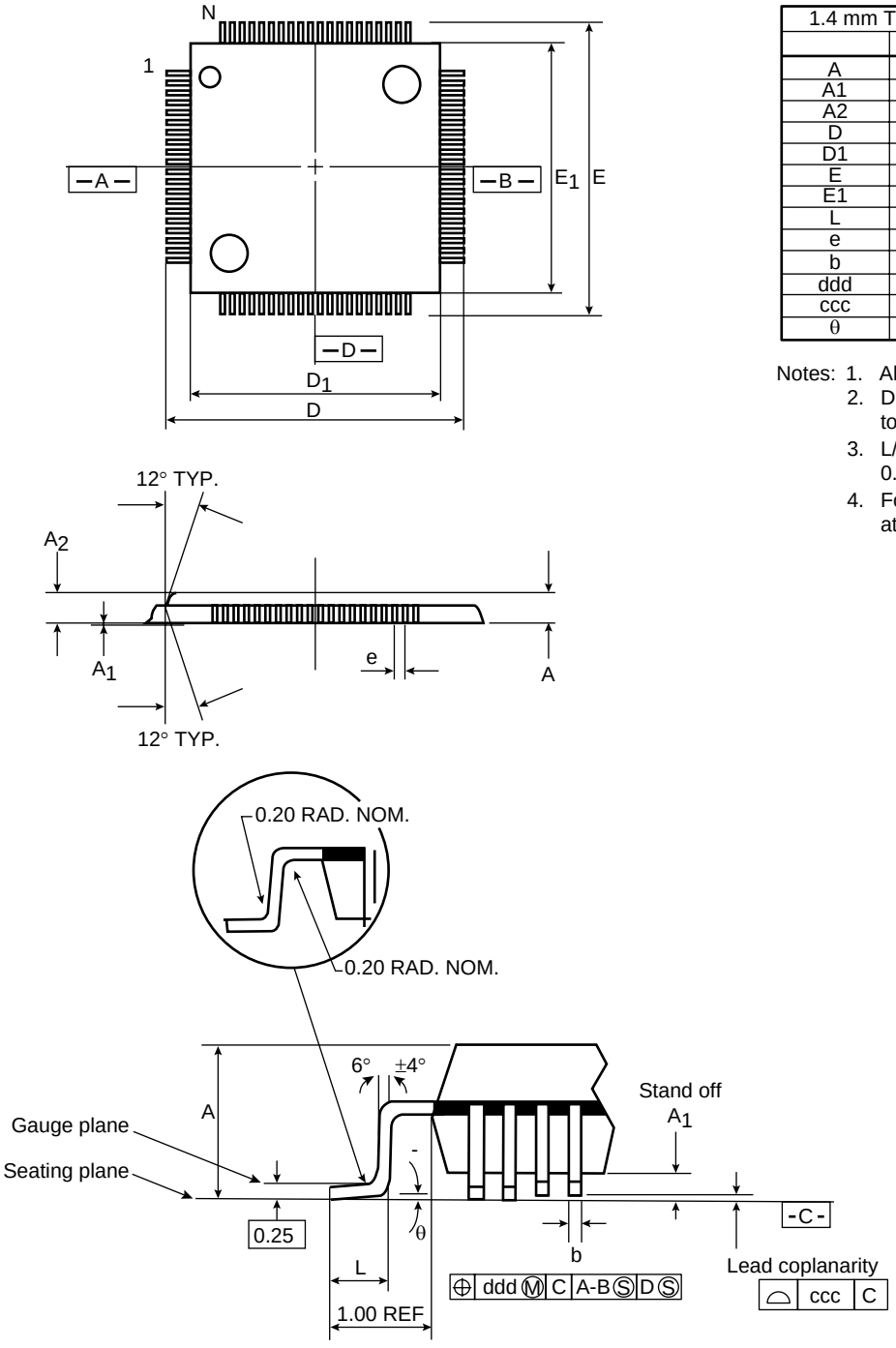
Symbol	Pin Number	Function
GNDA, GNDD, GNDO	1, 4, 5, 8, 13, 16, 17, 20, 30, 36, 66, 71	Ground pins. To be connected to external ground plane.
V_{CCA}	9, 12	Analog positive supply: 3.15V typ.
V_{CCD}	3, 19, 65	+3.15V digital supply
V_{CCO}	29, 35, 72	+2.25V output supply
V_{INI}	14	In-phase (+) analog input signal of the sample and hold differential preamplifier channel I
V_{INIB}	15	Inverted phase (-) of analog input signal (V_{INI})
V_{INQ}	7	In-phase (+) analog input signal of the sample and hold differential preamplifier channel Q
V_{INQB}	6	Inverted phase (-) of analog input signal (V_{INQ})
CLK	10	In-phase (+) clock input signal. The analog input is sampled and held on the rising edge of the CLK signal.
CLKB	11	Inverted phase (-) of clock input signal (CLK)
DOAI0:DOAI5	21, 25, 31, 37, 41, 45	In-phase (+) digital outputs first phase demultiplexer DOAI0 is the LSB. D0AI5 is the MSB. Channel I.
DOAI0N:DOAI5N	22, 26, 32, 38, 42, 46	In-phase (-) digital outputs first phase demultiplexer DOAI0N is the LSB. D0AI5N is the MSB. Channel I.
DOBI0:DOBI5	23, 27, 33, 39, 43, 47	In-phase (+) digital outputs second phase demultiplexer DOBI0 is the LSB. D0BI5 is the MSB. Channel I.
DOBI0N:DOBI5N	43, 47, 53, 57, 61, 65	In-phase (-) digital outputs second phase demultiplexer DOBI0N is the LSB. D0BI5N is the MSB. Channel I.
DOAQ0:DOAQ5	56, 60, 64, 70, 76, 80	In-phase (+) digital outputs first phase demultiplexer DOAI0 is the LSB. D0AI5 is the MSB. Channel Q.
DOAQ0N:DOAQ5N	55, 59, 63, 69, 75, 79	In-phase (-) digital outputs first phase demultiplexer DOAI0N is the LSB. D0AI5N is the MSB. Channel Q.
DOBQ0:DOBQ5	54, 58, 62, 68, 74, 78	In-phase (+) digital outputs second phase demultiplexer DOBQ0 is the LSB. D0BQ5 is the MSB. Channel Q.
DOBQ0N:DOBQ5N	53, 57, 61, 67, 73, 77	In-phase (-) digital outputs second phase demultiplexer DOBQ0N is the LSB. D0BQ5N is the MSB. Channel Q.
DOIR	49	Combined (I and Q) in-phase (+) out-of-range bit first phase demultiplexer. Out-of-range is high on the leading edge of code 0 and code 64.
DOIRN	50	Combined (I and Q) in-phase (-) out-of-range bit first phase demultiplexer
CLKO	52	Output clock in-phase (+),1/2 input clock frequency
CLKOB	51	Output clock in-phase (-),1/2 input clock frequency
NC	2, 18	Not connected

Figure 15. 80-lead TQFP Pinout



Package Dimensions

Figure 16. 80-lead TQFP Package Dimensions



1.4 mm Thickness - Body +2.00 mm Footprint		
	Dimensions	Tolerances
A	1.20	Max.
A1	0.05 Min./0.15 Max.	
A2	1.00	±0.50
D	14.00	±0.20
D1	12.00	±0.05
E	14.00	±0.20
E1	12.00	±0.05
L	0.60	+0.15/-0.10
e	0.50	Basic
b	0.22	±0.05
ddd	0.08	Max.
ccc	0.08	Max.
θ	0° - 7°	

Notes:
1. All dimensions are in millimeters.
2. Dimensions shown are nominal with tolerances as indicated.
3. L/F: Eftec 64T copper, 0.127 mm (0.005") thick.
4. Foot length: "L" is measured at gauge plane, at 0.25 mm above the seating plane.

Table 8. 80-lead TQFP Package Characteristics

Package Type	θ JA (°C/W)
80-lead TQFP	39.0

Definition of Terms

Table 9. Definition of Terms

BER	Bit error rate	Probability of exceeding a specified error threshold for a sample. An error code is a code that differs by more than ±4 LSBs from the correct code.
FPBW	Full-power input bandwidth	Analog input frequency for which the fundamental component in the digitally reconstructed output has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at full scale.
SINAD	Signal-to-noise and distortion ratio	Ratio expressed in dB of the RMS signal amplitude, set to 1 dB below full scale, to the RMS sum of all other spectral components, including the harmonics except DC.
THD	Total harmonic distortion	Ratio expressed in dBc of the RMS sum of the first five harmonic components, to the RMS value of the measured fundamental spectral component.
SFDR	Spurious free dynamic range	Ratio expressed in dB of the RMS signal amplitude, set at 1 dB below full scale, to the RMS value of the next highest spectral component (peak spurious spectral component). SFDR is the key parameter for selecting a converter to be used in a frequency domain application (radar systems, digital receiver, network analyzer...). It may be reported in dBc (i.e., degrades as signal levels are lowered), or in dBFS (i.e., always related back to converter full scale).
ENOB	Effective number of bits	$ENOB = \frac{SINAD - 1.76 + 20 \log (A/V/2)}{6.02}$ where A is the actual input amplitude and V is the full scale range of the ADC under test
DNL	Differential non-linearity	The differential non-linearity for an output code (I) is the difference between the measured step size of code (I) and the ideal LSB step size. DNL (I) is expressed in LSBs. DNL is the maximum value of all DNL (I). A DNL error specification of less than 1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic. Measured with a histogram method.
INL	Integral non-linearity	The integral non-linearity for an output code (I) is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (I) is expressed in LSBs, and is the maximum value of all |INL (I)|. Measured with a histogram method.
TA	Aperture delay	Delay between the rising edge of the differential clock inputs (CLK, CLKB) (zero crossing point), and the time at which (V_{IN}, V_{INB}) is sampled.
JITTER	Aperture uncertainty	Sample-to-sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.
ORT	Overvoltage recovery time	Time to recover 0.2% accuracy at the output, after a 150% full scale step applied on the input is reduced to mid-scale.
TDO	Digital data output delay	Delay from the falling edge of the differential clock inputs (CLK, CLKB) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.
TD	Time delay from clock ready to data	Time delay from data transition ready to data.
TPD	Pipeline delay	Number of clock cycles between the sampling edge of input data and the associated output data being made available (not taking in account the TDO).
TR	Rise time	Time delay for the output data signals to rise from 10% to 90% of the delta between low level and high level.
TF	Fall time	Time delay for the output data signals to fall from 90% to 10% of the delta between low level and high level.

Table 9. Definition of Terms (Continued)

PSRR	Power supply rejection ratio	Ratio of input offset variation to a change in power supply voltage.
OFFI,Q	Offset output code I or Q	Mean output code with no input signal applied.
IMD	Inter-modulation distortion	The two-tone intermodulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermodulation products. The input tone levels are at -7 dB full scale.

Ordering Information

Table 10. Ordering Information

Part Number	Package	Temperature Range	Screening	Comments
AT76CL610-10AX	TQFP 80	Ambient	Prototype	Prototype
AT76CL610-10AC	TQFP 80	"C" grade 0°C < T_A < 70°C	Standard	
AT76CL610-10AI	TQFP 80	"I" grade -20°C < T_A < 85C	Standard	
AT76CL610-EB	TQFP 80	Ambient	Prototype	Evaluation Kit

Datasheet Status Description

Table 11. Datasheet Status

Datasheet Status		Validity
Objective specification	This datasheet contains target and goal specifications for discussion with the customer and application validation.	Before design phase
Target specification	This datasheet contains target or goal specifications for product development.	Valid during the design phase
Preliminary specification α-site	This datasheet contains preliminary data. Additional data may be published later and could include simulation results.	Valid before characterization phase
Preliminary specification β-site	This datasheet contains characterization results.	Valid before the industrialization phase
Product specification	This datasheet contains final product specifications.	Valid for production purposes
Limiting Values		
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application Information		
Where application information is given, it is advisory and does not form part of the specification.		

Life Support Applications

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Atmel customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Atmel for any damages resulting from such improper use or sale.

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