

## 74F378 Parallel D Register with Enable

### General Description

The 'F378 is a 6-bit register with a buffered common Enable. This device is similar to the 'F174, but with common Enable rather than common Master Reset.

- Positive edge-triggered D-type inputs
- Fully buffered common clock and enable inputs
- Input clamp diodes limit high-speed termination effects
- Full TTL and CMOS compatible

### Features

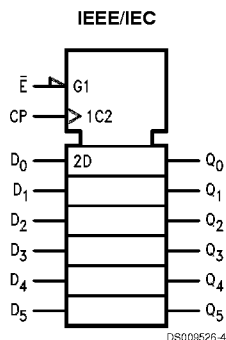
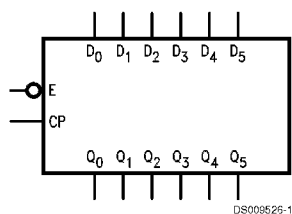
- 6-bit high-speed parallel register

### Ordering Code:

Commercial	Military	Package Number	Package Description
74F378PC		N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
	54F378DM (QB)	J16A	16-Lead Ceramic Dual-In-Line
74F378SC (Note 1)		M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F378SJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F378FM (QB)	W16A	16-Lead Cerpack
	54F378LM (QB)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

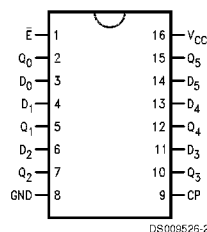
Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

### Logic Symbols

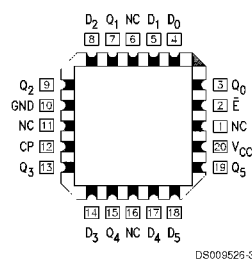


### Connection Diagrams

#### Pin Assignment for DIP, SOIC and Flatpak



#### Pin Assignment for LCC



## Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\bar{E}$	Enable Input (Active LOW)	1.0/1.0	20 $\mu A$ / -0.6 mA
$D_0$ - $D_5$	Data Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu A$ / -0.6 mA
$Q_0$ - $Q_5$	Outputs	50/33.3	-1 mA / 20 mA

## Functional Description

The 'F378 consists of six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable ( $\bar{E}$ ) inputs are common to all flip-flops.

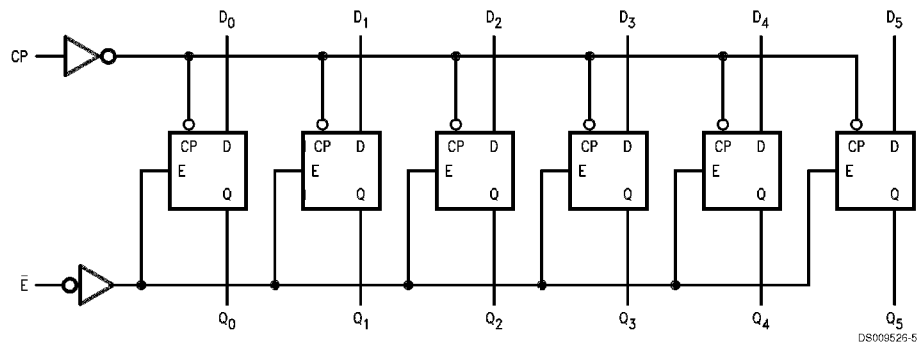
When the  $\bar{E}$  input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the  $\bar{E}$  input is HIGH the register will retain the present data independent of the CP input.

## Truth Table

Inputs			Output
$\bar{E}$	CP	$D_n$	$Q_n$
H		X	No Change
L		H	H
L		L	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 = LOW-to-HIGH Clock Transition

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output	

in LOW State (Max)

twice the rated I<sub>OL</sub> (mA)

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**Note 2:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 3:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage		0.8			V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage		-1.2			V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5			V	Min	I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5					
		74F 5% V <sub>CC</sub>	2.7					
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>	0.5			V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>	0.5					
I <sub>IH</sub>	Input HIGH Current	54F	20.0			μA	Max	V <sub>IN</sub> = 2.7V
		74F	5.0					
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F	100			μA	Max	V <sub>IN</sub> = 7.0V
		74F	7.0					
I <sub>CEX</sub>	Output HIGH Leakage Current	54F	250			μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F	50					
V <sub>ID</sub>	Input Leakage Test	74F	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F	3.75			μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current		-0.6			mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current		-60			mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		30	45		mA	Max	V <sub>O</sub> = LOW

## AC Electrical Characteristics

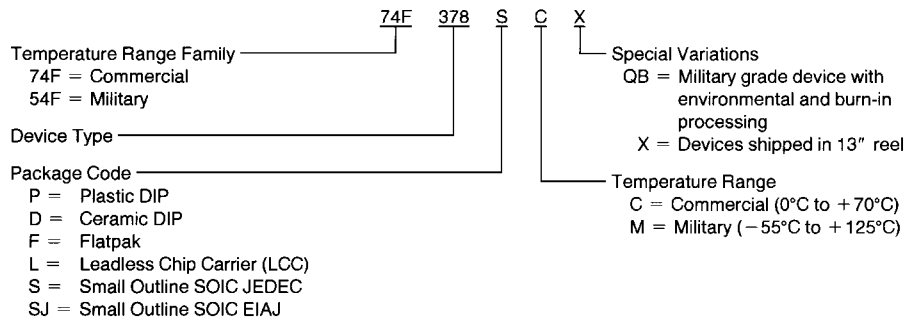
Symbol	Parameter	74F			54F		74F		Units
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = MII C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f <sub>max</sub>	Maximum Input Frequency	80	100		70		80	MHz	
t <sub>PLH</sub>	Propagation Delay	3.0	5.5	7.5	3.0	10.0	3.0	8.5	ns
t <sub>PHL</sub>	CP to Q <sub>n</sub>	3.5	6.0	8.5	3.5	10.5	3.5	9.5	

## AC Operating Requirements

Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{MII}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	Min	Max	
$t_s(\text{H})$	Setup Time, HIGH or LOW	4.0		5.0		4.0		ns
$t_s(\text{L})$	$D_n$ to CP	4.0		5.0		4.0		
$t_h(\text{H})$	Hold Time, HIGH or LOW	0		2.0		0		ns
$t_h(\text{L})$	$D_n$ to CP	0		2.0		0		
$t_s(\text{H})$	Setup Time, HIGH or LOW	6.0		4.5		6.0		ns
$t_s(\text{L})$	$\bar{E}$ to CP	10.0		13.0		10.0		
$t_h(\text{H})$	Hold Time, HIGH or LOW	0		0		0		ns
$t_h(\text{L})$	$\bar{E}$ to CP	0		0		0		
$t_w(\text{H})$	CP Pulse Width	4.0		5.0		4.0		ns
$t_w(\text{L})$	HIGH or LOW	6.0		7.5		6.0		

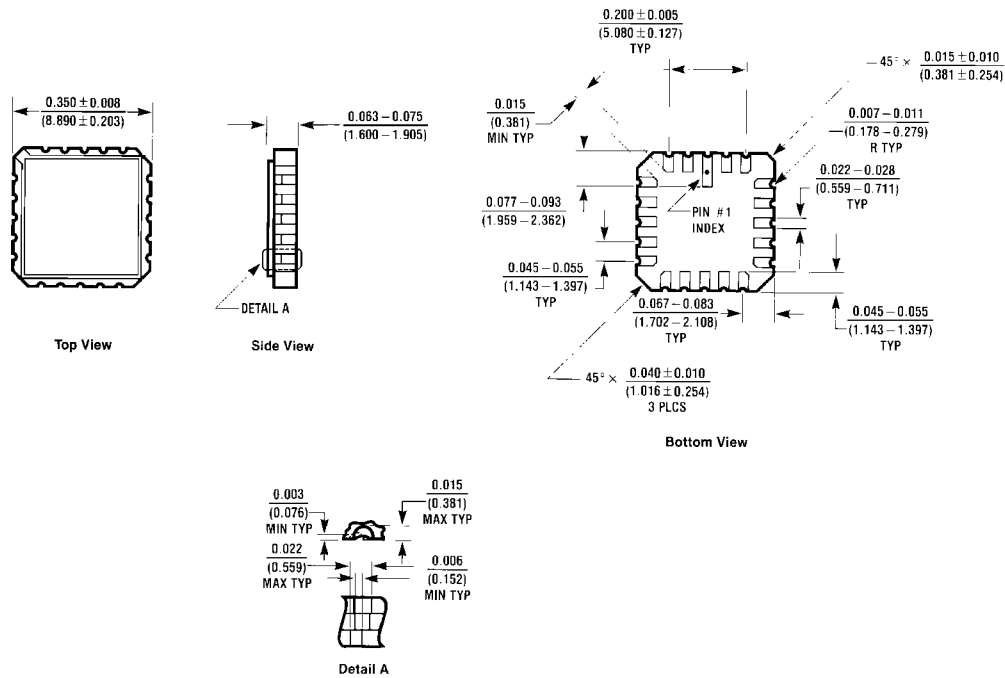
## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



DS009526-6

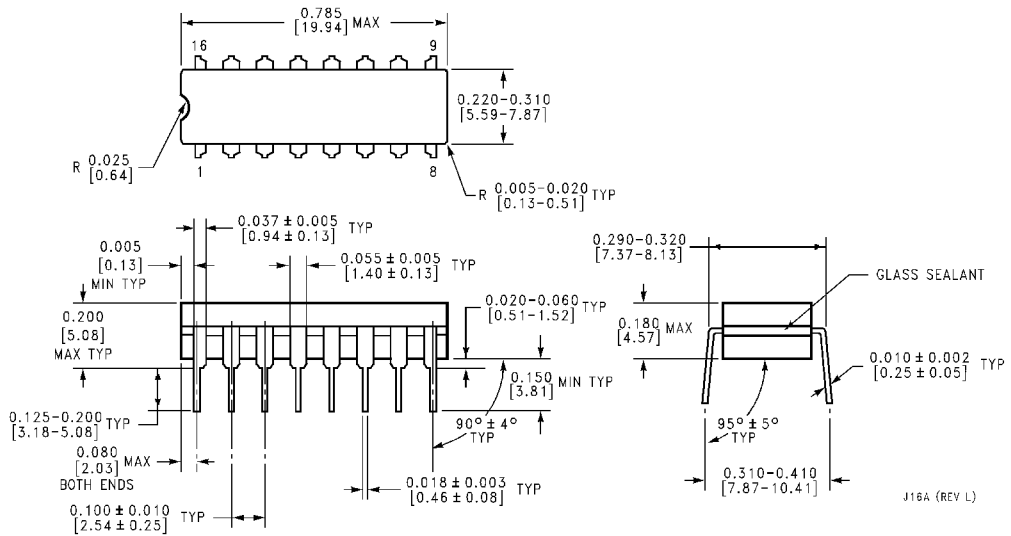
## Physical Dimensions inches (millimeters) unless otherwise noted



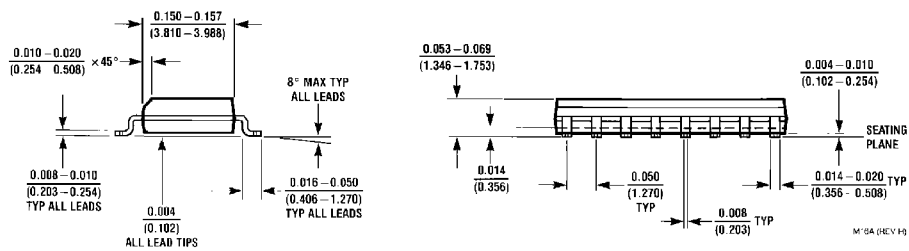
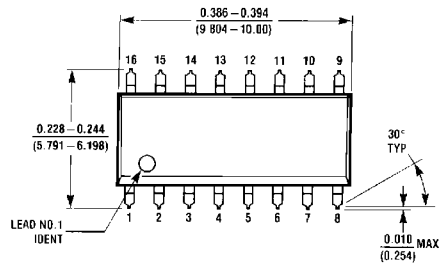
EDA, REV D

**20-Lead Ceramic Leadless Chip Carrier (L)  
 Package Number E20A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

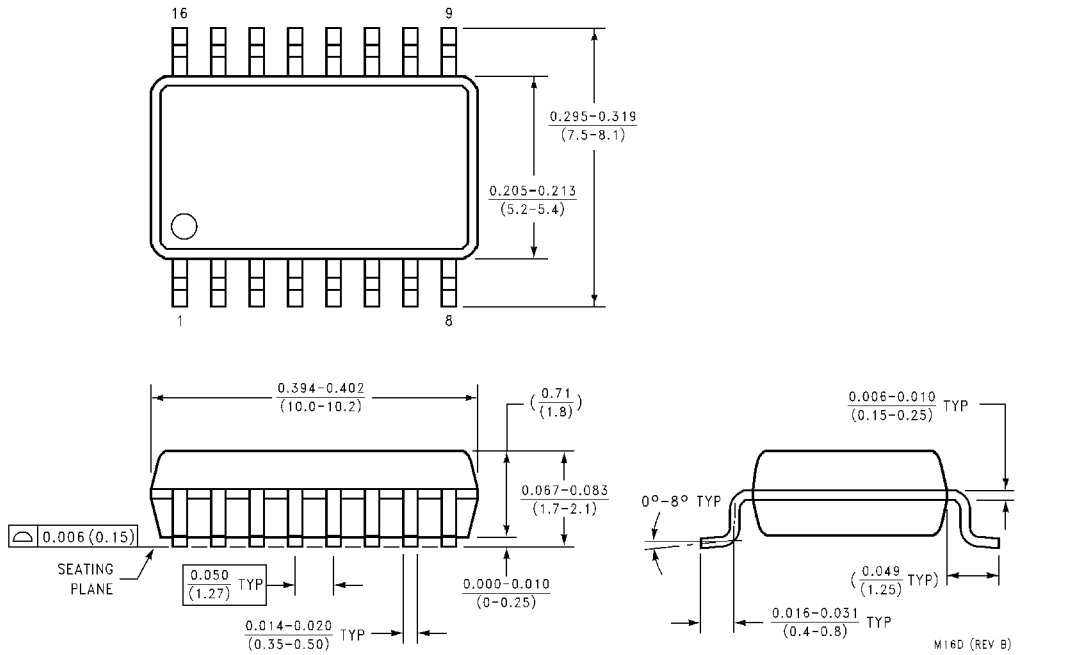


**16-Lead Ceramic Dual-In-Line Package (D)**  
Package Number J16A

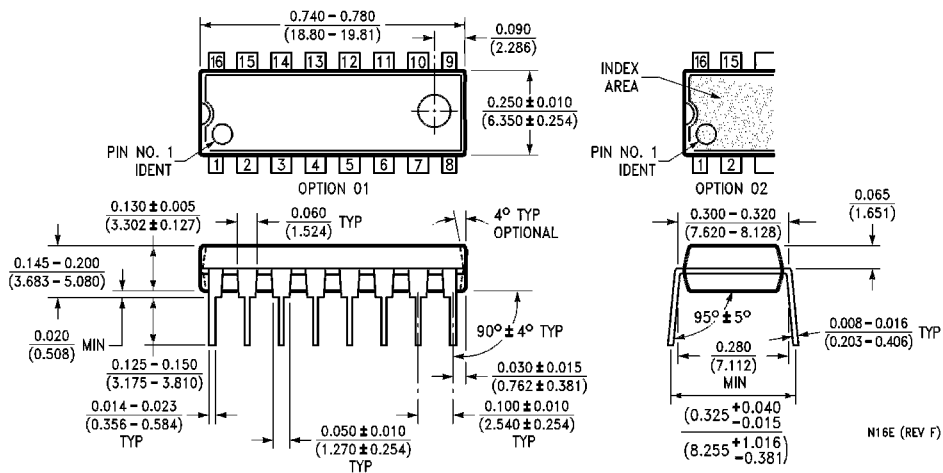


**16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC**  
Package Number M16A

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

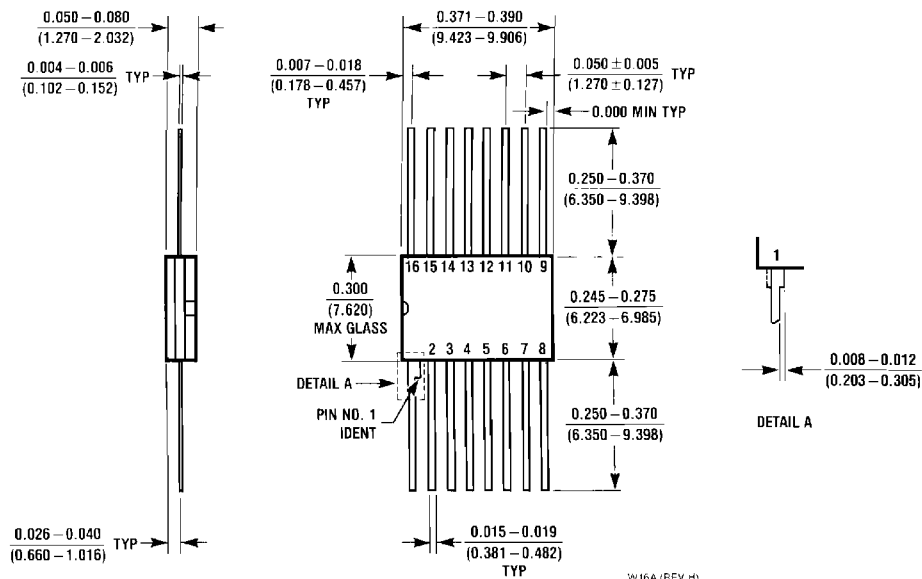


**16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)  
 Package Number M16D**



**16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)  
 Package Number N16E**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Ceramic Flatpak (F)  
Package Number W16A**

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