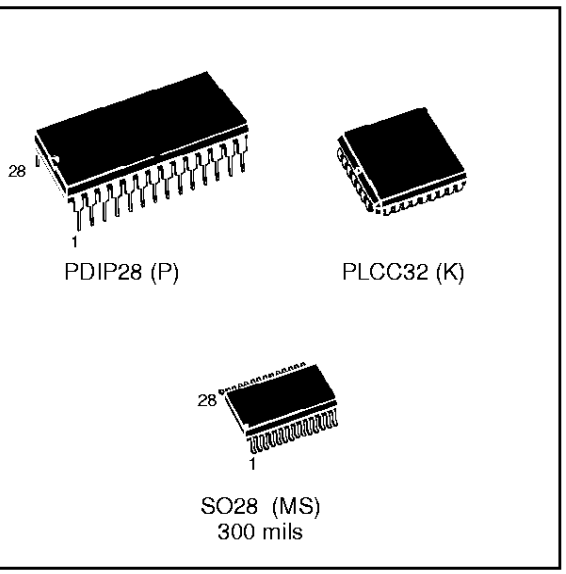
SGS-THOMSON MICROELECTRONICS

M28LV17

LOW VOLTAGE 16K (2K x 8) PARALLEL EEPROM with SOFTWARE DATA PROTECTION

- FAST ACCESS TIME: 200ns
- SINGLE LOW VOLTAGE OPERATION
- LOW POWER CONSUMPTION
- FAST WRITE CYCLE:
  - 64 Bytes Page Write Operation
  - Byte or Page Write Cycle: 3ms Max
- ENHANCED END OF WRITE DETECTION:
  - Ready/Busy Open Drain Output
  - Data Polling
  - Toggle Bit
- PAGE LOAD TIMER STATUS BIT
- HIGH RELIABILITY SINGLE POLYSILICON, CMOS TECHNOLOGY:
  - Endurance >100,000 Erase/Write Cycles
  - Data Retention >40 Years
- JEDEC APPROVED BYTEWIDE PIN OUT
- SOFTWARE DATA PROTECTION



DESCRIPTION

The M28LV17 is a 2K x 8 low power Parallel EEPROM fabricated with SGS-THOMSON proprietary single polysilicon CMOS technology. The device offers fast access time with low power dissipation and requires a 2.7V to 3.6V power supply.

The M28LV17 offers the same features than the M28LV16, in addition to the Ready/Busy pin.

The circuit has been designed to offer a flexible microcontroller interface featuring both hardware

Table 1. Signal Names

A0 - A10	Address Input
DQ0 - DQ7	Data Input / Output
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$R\overline{B}$	Ready / Busy
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

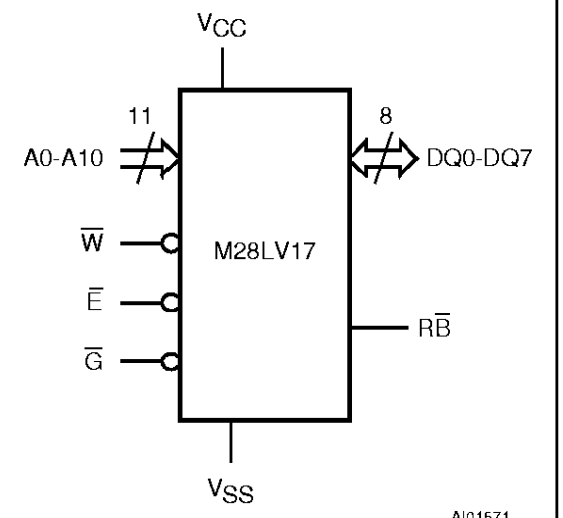
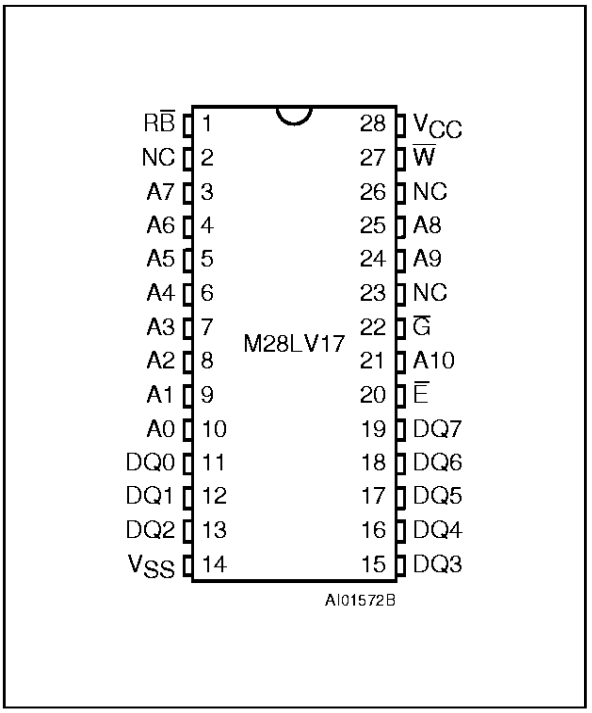
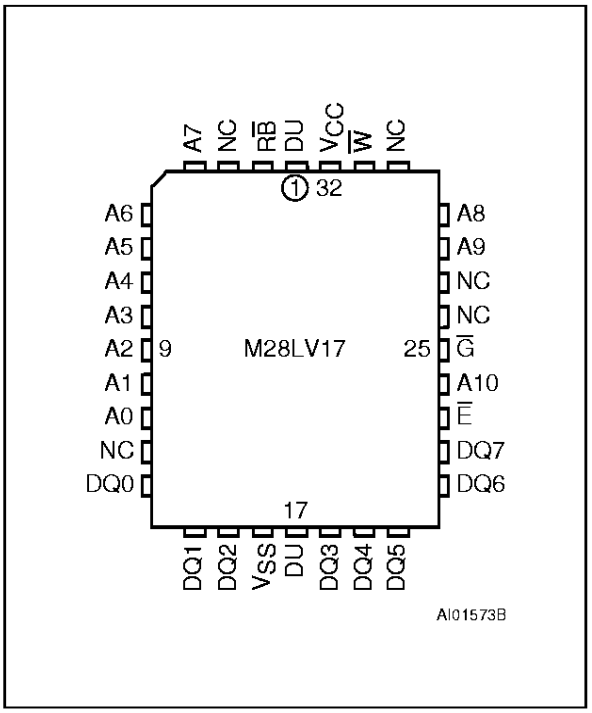


Figure 2A. DIP Pin Connections



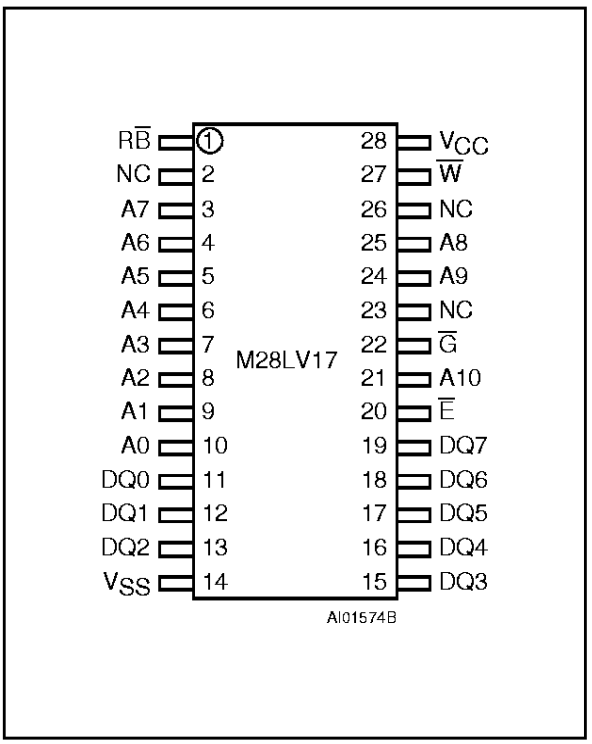
Warning: NC = No Connection.

Figure 2B. LCC Pin Connections



Warning: NC = No Connection, DU = Don't Use

Figure 2C. SO Pin Connections



Warning: NC = No Connection.

DESCRIPTION (cont'd)

and software handshaking with Ready/Busy, Data Polling and Toggle Bit. The M28LV17 supports 64 byte page write operation. A Software Data Protection (SDP) is also possible using the standard JEDEC algorithm.

PIN DESCRIPTION

Addresses (A0-A10). The address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{E}$). The chip enable input must be low to enable all read/write operations. When Chip Enable is high, power consumption is reduced.

Output Enable ($\overline{G}$). The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Out (DQ0 - DQ7). Data is written to or read from the M28LV17 through the I/O pins.

Write Enable ($\overline{W}$). The Write Enable input controls the writing of data to the M28LV17.

Ready/Busy ($R\overline{B}$). Ready/Busy is an open drain output that can be used to detect the end of the internal write cycle.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	– 40 to 85	°C
T_{STG}	Storage Temperature Range	– 65 to 150	°C
V_{CC}	Supply Voltage	–0.3 to 6.5	V
V_{IO}	Input/Output Voltage	– 0.3 to V_{CC} +0.6	V
V_I	Input Voltage	–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)	4000	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

2. 100pF through 1500Ω; MIL-STD-883C, 3015.7

Table 3. Operating Modes (1)

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Standby	1	X	X	Hi-Z
Output Disable	X	1	X	Hi-Z
Write Disable	X	X	1	Hi-Z
Read	0	0	1	Data Out
Write	0	1	0	Data In

Note: 1. 0 = V_{IL}; 1 = V_{IH}; X = V_{IL} or V_{IH}.

OPERATION

In order to prevent data corruption and inadvertent write operations during power-up, a Power On Reset (POR) circuit resets all internal programming cicuitry. Access to the memory in write mode is allowed after a power-up as specified in Table 7.

Read

The M28LV17 is accessed like a static RAM. When $\overline{E}$ and $\overline{G}$ are low with $\overline{W}$ high, the data addressed is presented on the I/O pins. The I/O pins are high impedance when either $\overline{G}$ or $\overline{E}$ is high.

Write

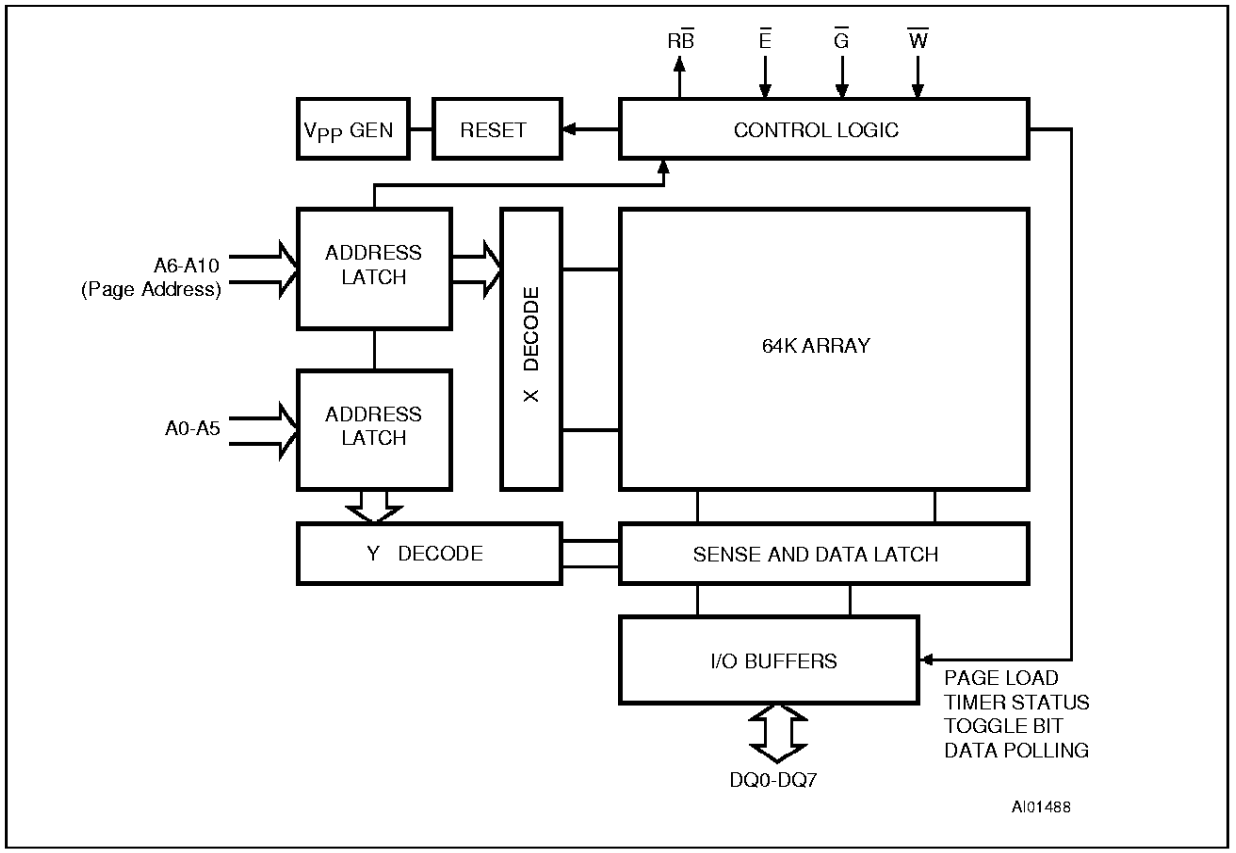
Write operations are initiated when both $\overline{W}$ and $\overline{E}$ are low and $\overline{G}$ is high. The M28LV17 supports both $\overline{E}$ and $\overline{W}$ controlled write cycles. The Address is latched by the falling edge of $\overline{E}$ or $\overline{W}$ which ever occurs last and the Data on the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first. Once initiated the write operation is internally timed until completion.

Page Write

Page write allows up to 64 bytes to be consecutively latched into the memory prior to initiating a programming cycle. All bytes must be located in a single page address, that is A6-A10 must be the same for all bytes. The page write can be initiated during any byte write operation.

Following the first byte write instruction the host may send another address and data with a minimum data transfer rate of $1/t_{WHWH}$ (see Figure 13). If a transition of $\overline{E}$ or $\overline{W}$ is not detected within t_{WHWH}, the internal programming cycle will start.

Figure 3. Block Diagram



Microcontroller Control Interface

The M28LV17 provides two write operation status bits and one status pin that can be used to minimize the system write cycle. These signals are available on the I/O port bits DQ7 or DQ6 of the memory during programming cycle only, or as the RB signal on a separate pin.

Figure 4. Status Bit Assignment

DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
DP	TB	PLTS	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

DP = Data Polling
TB = Toggle Bit
PLTS = Page Load Timer Status

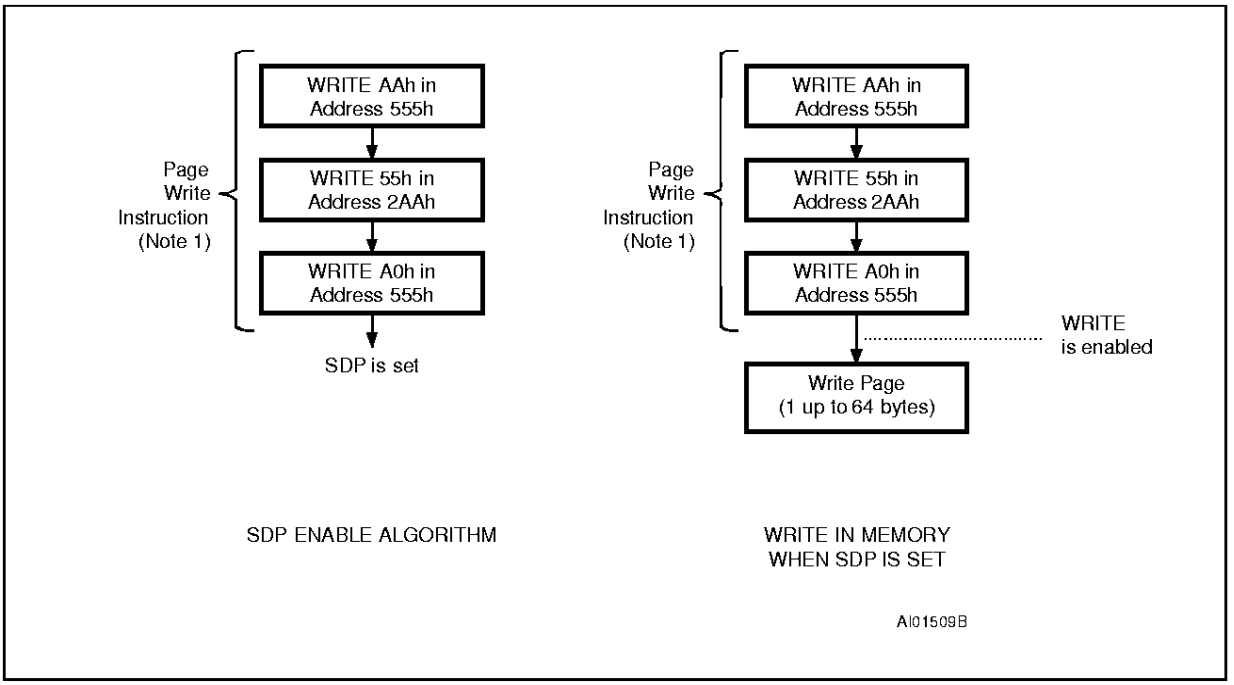
Data Polling bit (DQ7). During the internal write cycle, any attempt to read the last byte written will produce on DQ7 the complementary value of the previously latched bit. Once the write cycle is finished the true logic value appears on DQ7 in the read cycle.

Toggle bit (DQ6). The M28LV17 offers another way for determining when the internal write cycle is completed. During the internal Erase/Write cycle, DQ6 will toggle from "0" to "1" and "1" to "0" (the first read value is "0") on subsequent attempts to read the memory. When the internal cycle is completed the toggling will stop and the device will be accessible for a new Read or Write operation.

Page Load Timer Status bit (DQ5). In the Page Write mode data may be latched by E or W. Up to 32 bytes may be input. The Data output (DQ5) indicates the status of the internal Page Load Timer. DQ5 may be read by asserting Output Enable Low (t_{PLTS}). DQ5 Low indicates the timer is running, High indicates time-out after which the write cycle will start and no new data may be input.

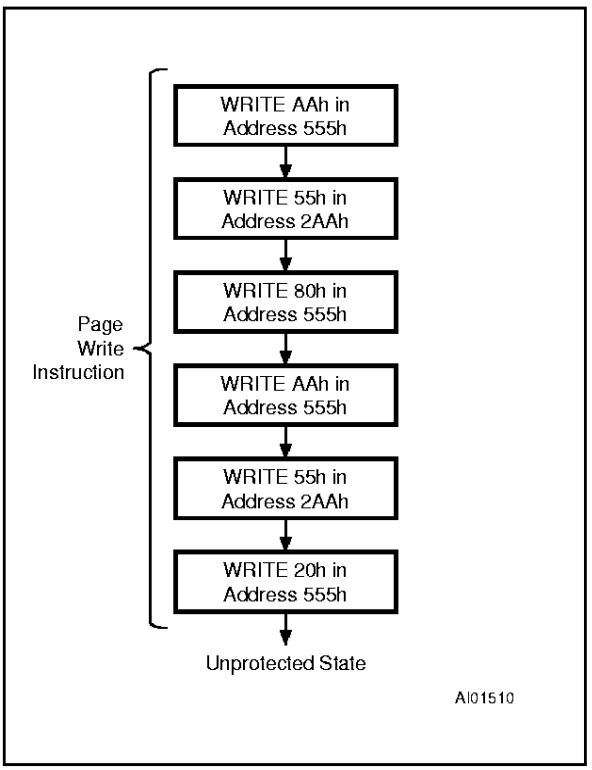
Ready/Busy pin. The RB pin provides a signal at its open drain output which is low during the erase/write cycle, but which is released at the completion of the programming cycle.

Figure 5. Software Data Protection Enable Algorithm and Memory Write



Note: 1. MSB Address bits (A6 to A10) differ during these specific Page Write operations.

Figure 6. Software Data Protection Disable Algorithm



Software Data Protection

The M28LV17 offers a software controlled write protection facility that allows the user to inhibit all write modes to the device including the Chip Erase instruction. This can be useful in protecting the memory from inadvertent write cycles that may occur due to uncontrolled bus conditions.

The M28LV17 is shipped as standard in the "unprotected" state meaning that the memory contents can be changed as required by the user. After the Software Data Protection enable algorithm is issued, the device enters the "Protect Mode" of operation where no further write commands have any effect on the memory contents. The device remains in this mode until a valid Software Data Protection (SDP) disable sequence is received whereby the device reverts to its "unprotected" state. The Software Data Protection is fully non-volatile and is not changed by power on/off sequences.

To enable the Software Data Protection (SDP) the device requires the user to write (with a Page Write) three specific data bytes to three specific memory locations as per Figure 5. Similarly to disable the Software Data Protection the user has to write specific data bytes into six different locations as per Figure 6 (with a Page Write). This complex series ensures that the user will never enable or disable the Software Data Protection accidentally.

Table 4. AC Measurement Conditions

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0V to V_{CC} -0.3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 7. AC Testing Input Output Waveforms

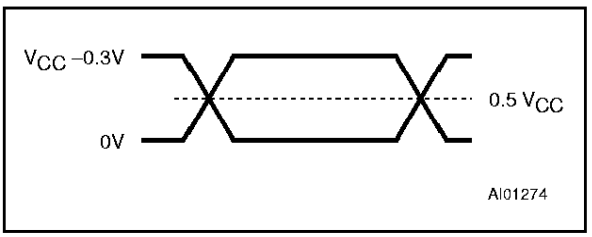


Figure 8. AC Testing Equivalent Load Circuit

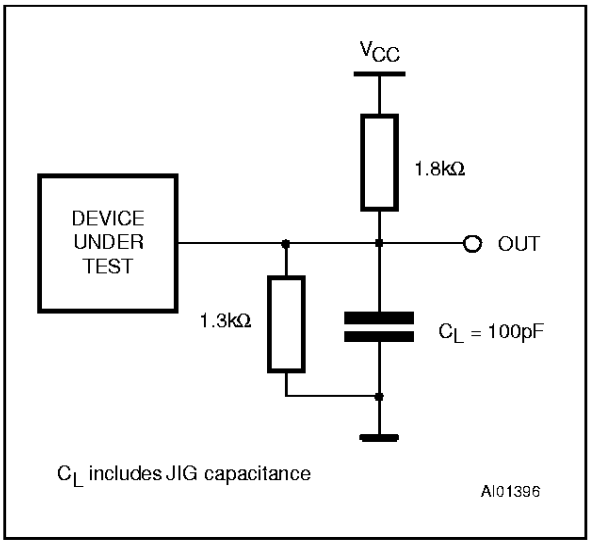


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		10	µA
I_{CC} (1)	Supply Current (CMOS inputs)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, f = 5 MHz, V_{CC} = 3.3V		8	mA
		$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, f = 5 MHz, V_{CC} = 3.6V		10	mA
I_{CC2} (1)	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} –0.3V		50	µA
V_{IL}	Input Low Voltage		– 0.3	0.6	V
V_{IH}	Input High Voltage		2	V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA		0.2 V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = 1 mA	0.8 V_{CC}		V

Note: 1. All I/O's open circuit.

Table 7. Power Up Timing (1) (T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Min	Max	Unit
t_{PUR}	Time Delay to Read Operation	1		µs
t_{PUW}	Time Delay to Write Operation	10		ms
V_{WI}	Write Inhibit Threshold	1.5	2.5	V

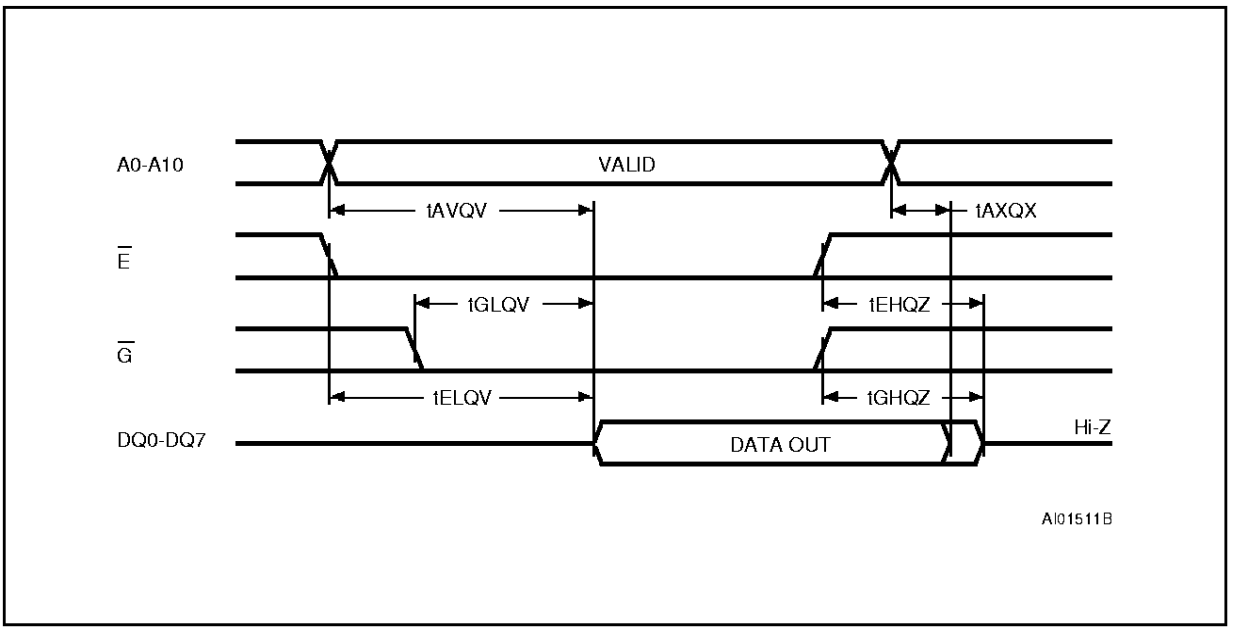
Note: 1. Sampled only, not 100% tested.

Table 8. Read Mode AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.7V to 3.6V)

Symbol	Alt	Parameter	Test Condition	M28LV17						Unit
				-200		-250		-300		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		200		250		300	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	G = V_{IL}		200		250		300	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		100		150		150	ns
t_{EHQZ} (1)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	55	0	60	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	55	0	60	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Note: 1. Output Hi-Z is defined as the point at which data is no longer driven.

Figure 9. Read Mode AC Waveforms



Note: Write Enable ($\overline{W}$) = High.

Table 9. Write Mode AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.7V to 3.6V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G}$ = V_{IH}, $\overline{W}$ = V_{IL}	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E}$ = V_{IL}	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W}$ = V_{IL}	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		100		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		100		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G}$ = V_{IH}, $\overline{W}$ = V_{IL}		1	µs
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		100	1000	ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		0		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		0		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		100		ns
t_{WHWH}	t_{BLC}	Byte Load Repeat Cycle Time		0.2	100	µs
t_{WHRH}	t_{WC}	Write Cycle Time			3	ms
t_{WHRL}	t_{DB}	Write Enable High to Ready/Busy Low	Note 1		150	ns
t_{EHRL}	t_{DB}	Chip Enable High to Ready/Busy Low	Note 1		150	ns
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		50		ns

Note: 1. With a 3.3 kΩ external pull-up resistor.

Figure 10. Write Mode AC Waveforms - Write Enable Controlled

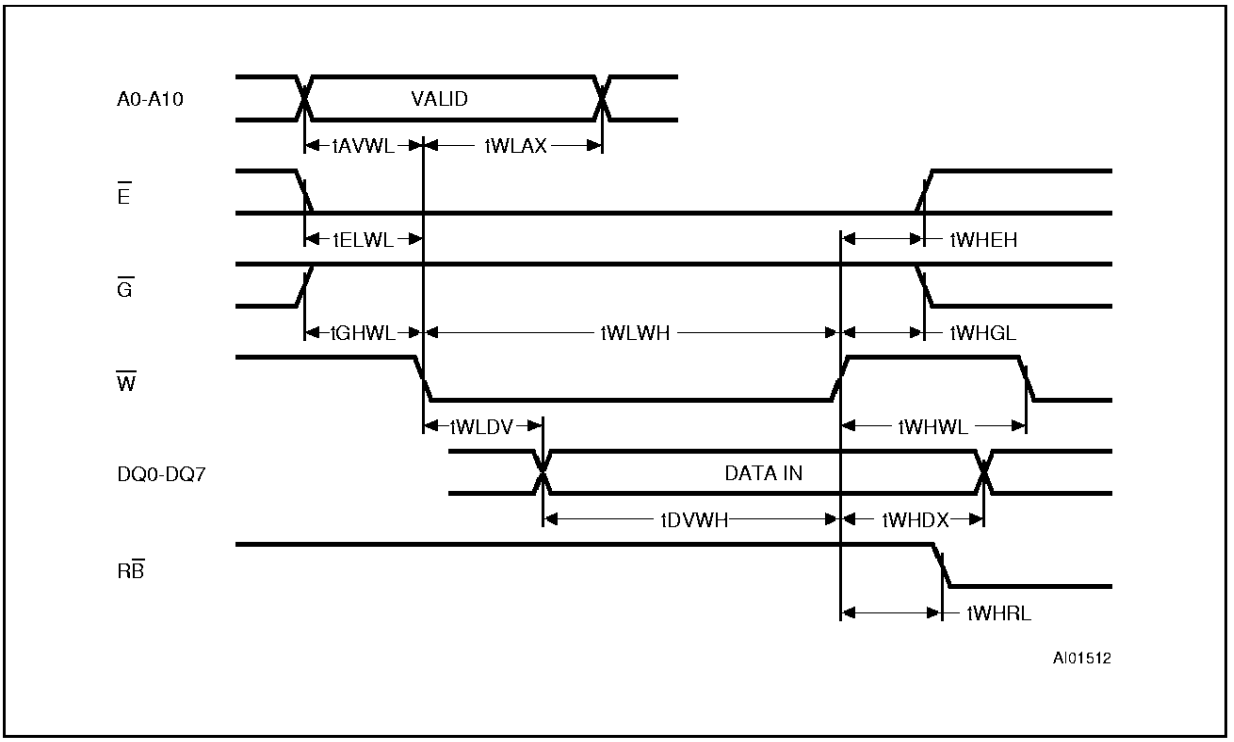


Figure 11. Write Mode AC Waveforms - Chip Enable Controlled

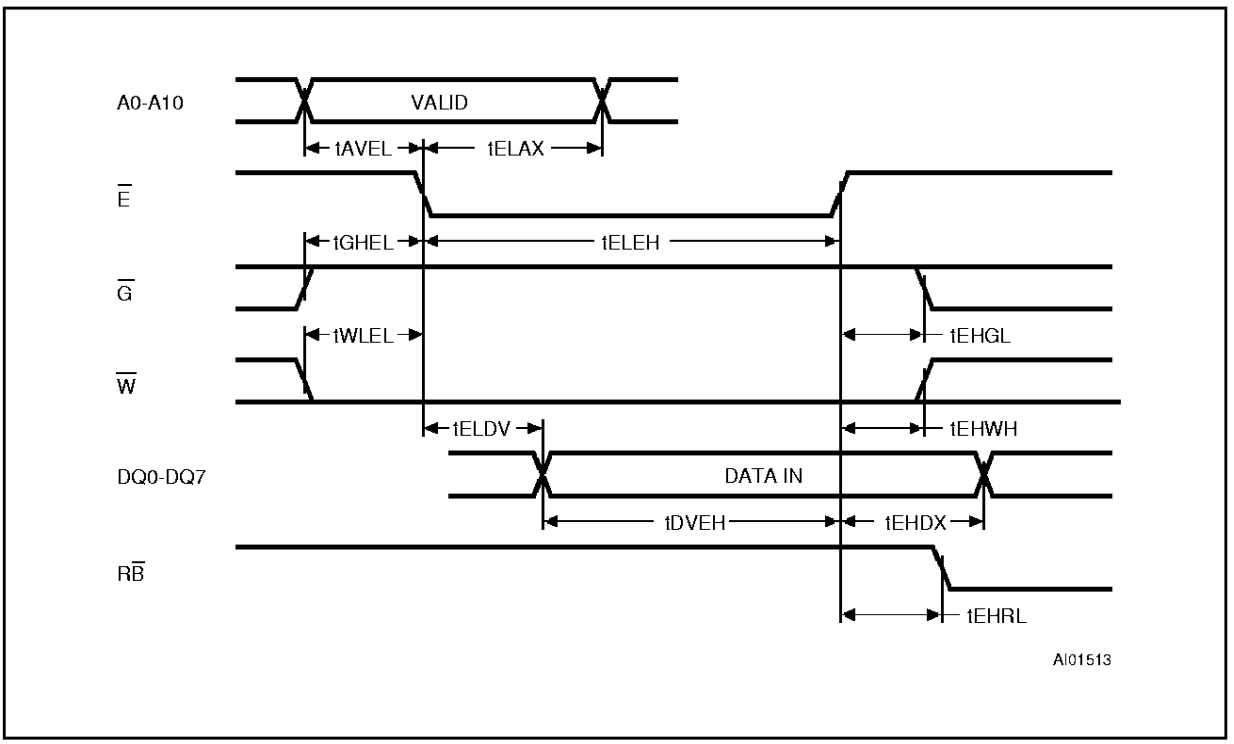


Figure 12. Page Write Mode AC Waveforms - Write Enable Controlled

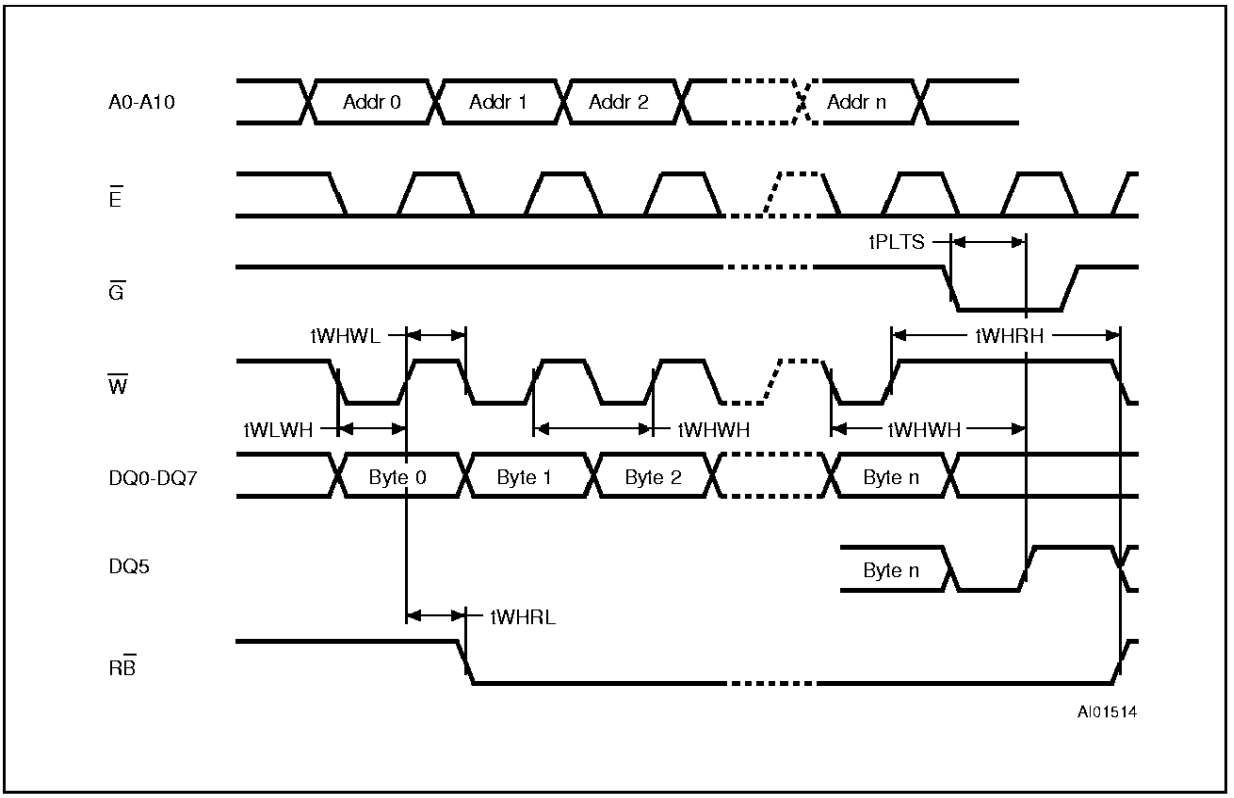
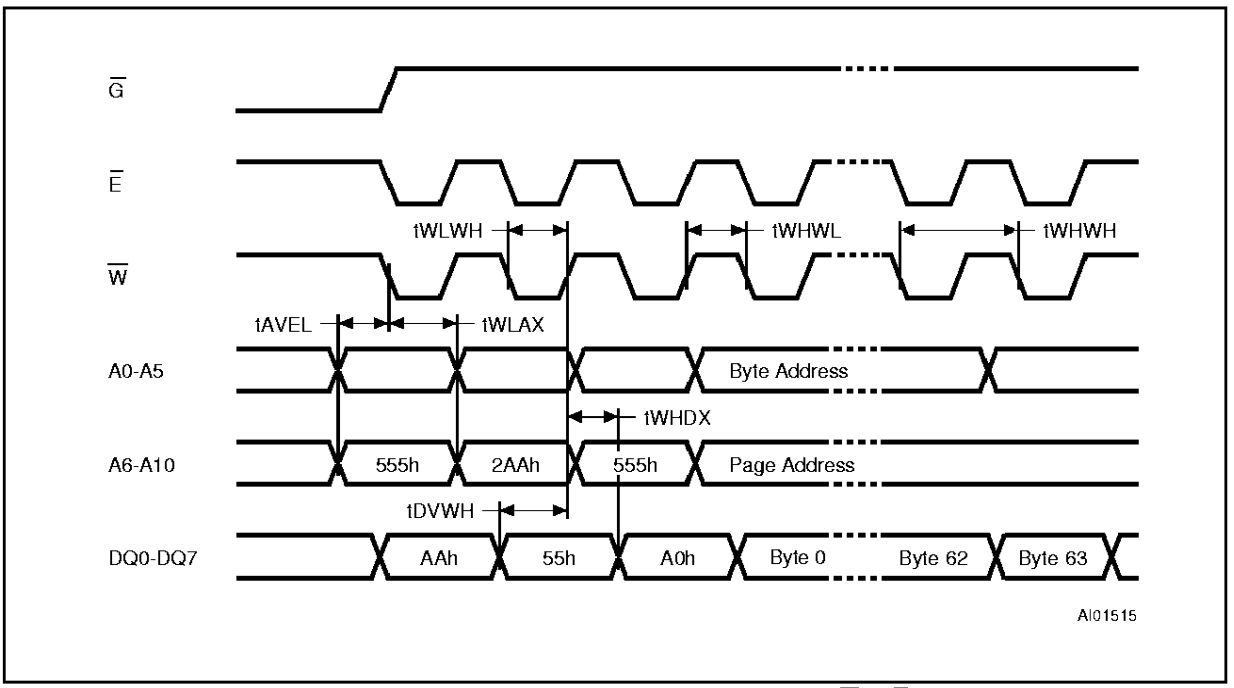


Figure 13. Software Protected Write Cycle Waveforms



Note: A6 through A10 must specify the same page address during each high to low transition of $\overline{W}$ (or $\overline{E}$) after the software code has been entered. G must be high only when W and E are both low.

Figure 14. Data Polling Waveform Sequence

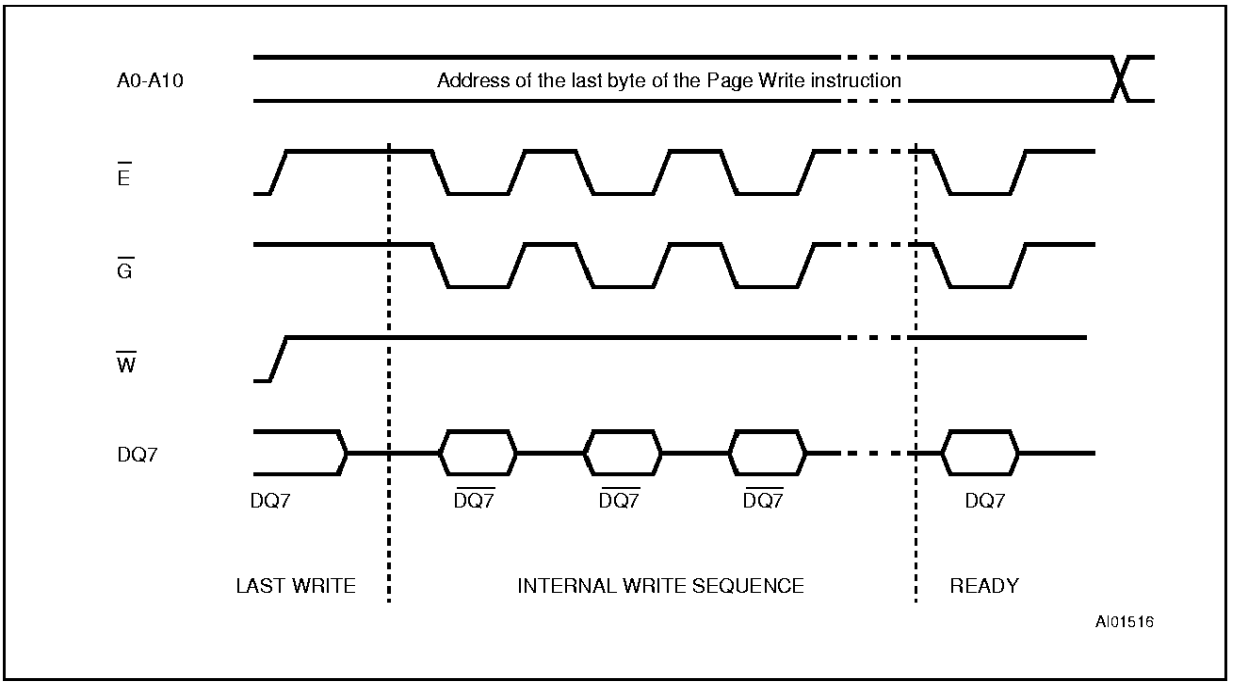
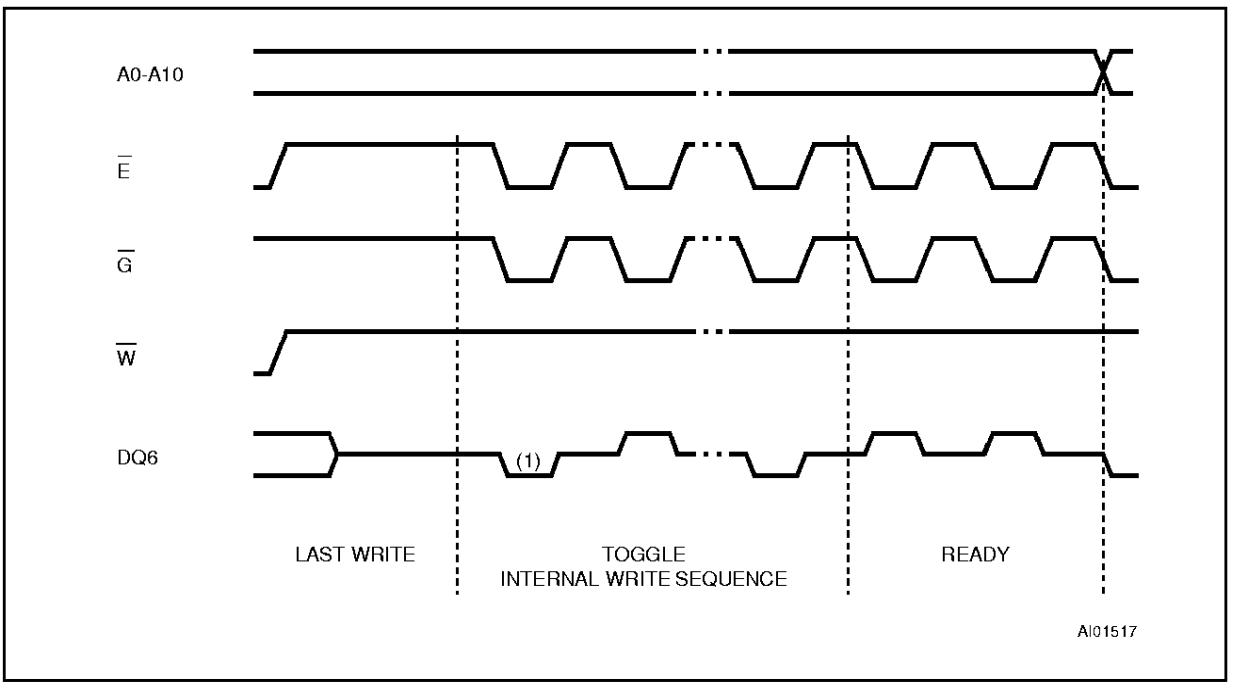


Figure 15. Toggle Bit Waveform Sequence



Note: 1. First Toggle bit is forced to '0'

ORDERING INFORMATION SCHEME

Example: M28LV17 -200 K 1 T

Speed		Package		Temperature Range		Option	
-200	200ns	P	PDIP28	1	0 to 70 °C	T	Tape & Reel Packing
-250	250ns	K	PLCC32	6	–40 to 85 °C		
-300	300ns	MS	SO28 300mils				

Parts are shipped with the memory content set at all "1's" (FFh).

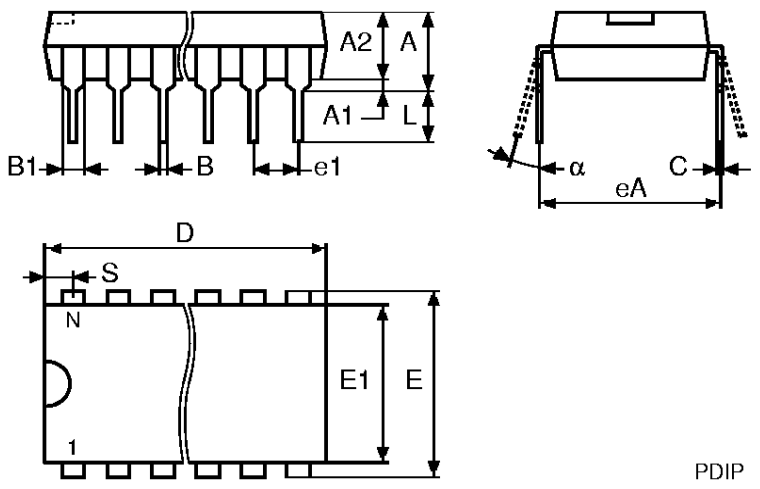
For a list of available options (Speed, Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PDIP28 - 28 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.94	5.08		0.155	0.200
A1		0.38	1.78		0.015	0.070
A2		3.56	4.06		0.140	0.160
B		0.38	0.56		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.30		0.008	0.012
D		34.70	37.34		1.366	1.470
E		14.80	16.26		0.583	0.640
E1		12.50	13.97		0.492	0.550
e1	2.54	–	–	0.100	–	–
eA		15.20	17.78		0.598	0.700
L		3.05	3.82		0.120	0.150
S		1.02	2.29		0.040	0.090
α		0°	15°		0°	15°
N	28			28		

PDIP28



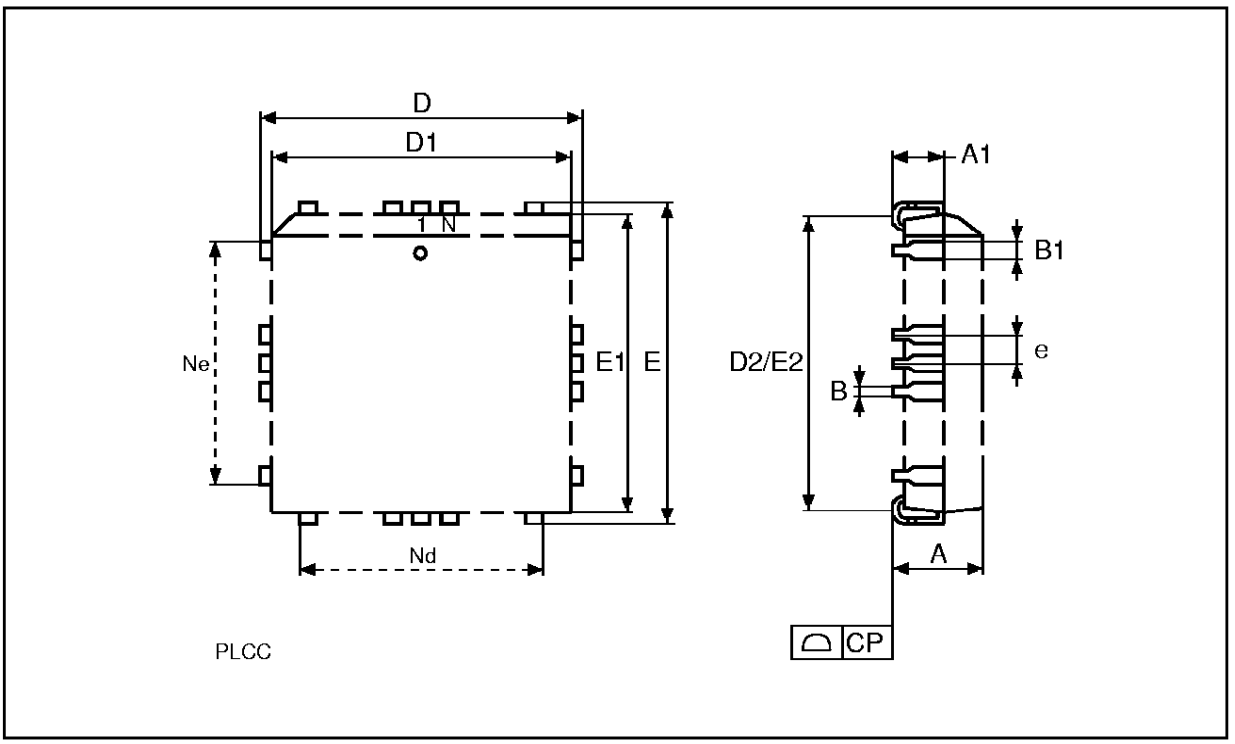
PDIP

Drawing is not to scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32

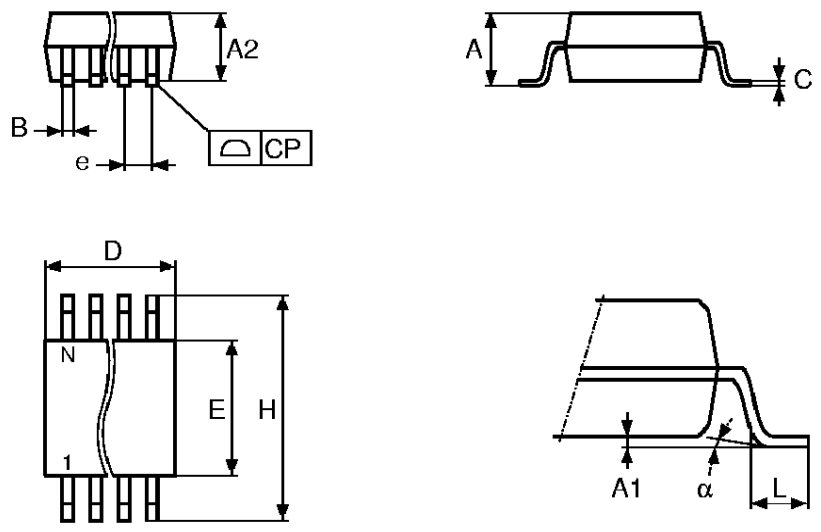


Drawing is not to scale

SO28 - 28 lead Plastic Small Outline, 300 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.46	2.64		0.097	0.104
A1		0.13	0.29		0.005	0.011
A2		2.29	2.39		0.090	0.094
B		0.35	0.48		0.014	0.019
C		0.23	0.32		0.009	0.013
D		17.81	18.06		0.701	0.711
E		7.42	7.59		0.292	0.299
e	1.27	–	–	0.050	–	–
H		10.16	10.41		0.400	0.410
L		0.61	1.02		0.024	0.040
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

SO28



SO-b

Drawing is not to scale