CYPRESS

PRELIMINARY **CY7C4425V/4205V/4215V**
CY7C4225V/4235V/4245V

64/256/512/1K/2K/4K x18 Low Voltage Synchronous FIFOs

Features

- **3.3V operation for low power consumption and easy integration into low voltage systems**
- **High-speed, low-power, first-in first-out (FIFO) memories**
- **64 x 18 (CY7C4425V)**
- **256 x 18 (CY7C4205V)**
- **512 x 18 (CY7C4215V)**
- **1K x 18 (CY7C4225V)**
- **2K x 18 (CY7C4235V)**
- **4K x 18 (CY7C4245V)**
- **0.65µ CMOS**
- **High-speed 67-MHz operation (15 ns read/write cycle times)**
- **Low power — I_{CC} = 30 mA**
- **5V tolerant inputs ($V_{IH\ MAX}$ = 5V)**
- **Fully asynchronous and simultaneous read and write operation**
- **Empty, Full, Half Full, and programmable Almost Empty and Almost Full status flags**
- **TTL compatible**
- **Retransmit function**
- **Output Enable ($\overline{OE}$) pin**
- **Independent read and write enable pins**
- **Supports free-running 50% duty cycle clock inputs**
- **Width Expansion Capability**
- **Depth Expansion Capability**
- **68-pin PLCC and 64-pin 10x10 STQFP**

Functional Description

The CY7C42X5V are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. All are 18 bits wide. The CY7C42X5V can be cascaded to increase FIFO depth. Programmable features include Almost Full/Almost Empty flags. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

These FIFOs have 18-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (WCLK) and a write enable pin ($\overline{WEN}$).

When $\overline{WEN}$ is asserted, data is written into the FIFO on the rising edge of the WCLK signal. While $\overline{WEN}$ is held active, data is continually written into the FIFO on each cycle. The output port is controlled in a similar manner by a free-running read clock (RCLK) and a read enable pin ($\overline{REN}$). In addition, the CY7C42X5V have an output enable pin ($\overline{OE}$). The read and write clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 66-MHz are achievable.

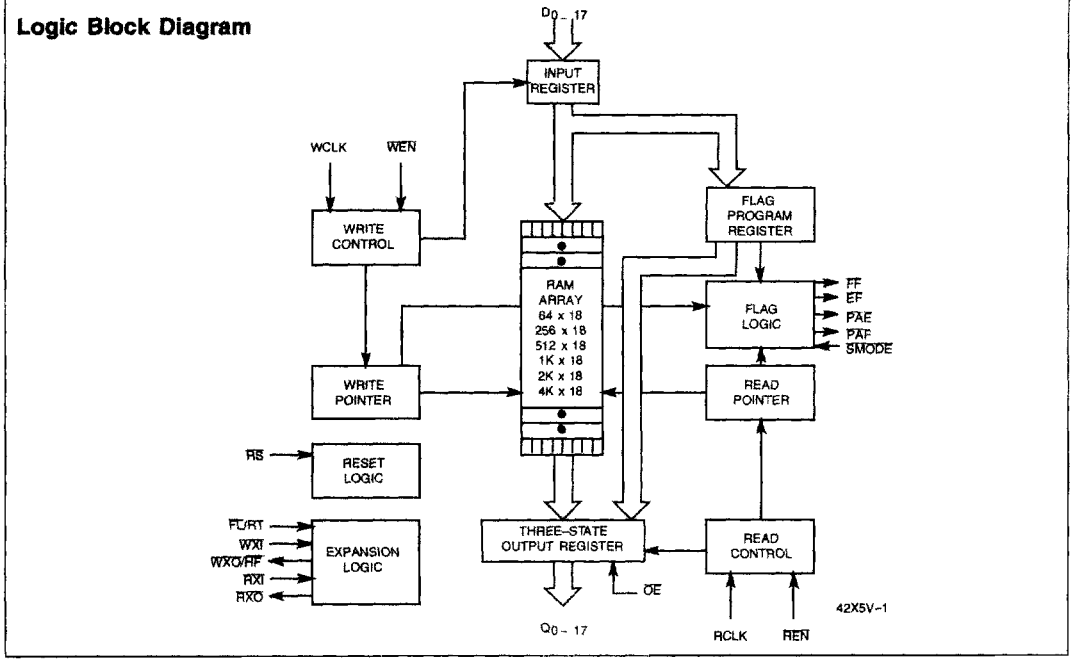
Retransmit and Synchronous Almost Full/Almost Empty flag features are available on these devices.

Depth expansion is possible using the cascade input ($\overline{WXI}$, $\overline{RXI}$), cascade output ($\overline{WXO}$, $\overline{RXO}$), and First Load ($\overline{FL}$) pins. The $\overline{WXO}$ and $\overline{RXO}$ pins are connected to the $\overline{WXI}$ and $\overline{RXI}$ pins of the next device, and the $\overline{WXO}$ and $\overline{RXO}$ pins of the last device should be connected to the $\overline{WXI}$ and $\overline{RXI}$ pins of the first device. The $\overline{FL}$ pin of the first device is tied to V_{SS} and the $\overline{FL}$ pin of all the remaining devices should be tied to V_{CC}.

The CY7C42X5V provides five status pins. These pins are decoded to determine one of five states: Empty, Almost Empty, Half Full, Almost Full, and Full (see *Table 2*). The Half Full flag shares the $\overline{WXO}$ pin. This flag is valid in the stand-alone and width-expansion configurations. In the depth expansion, this pin provides the expansion out ($\overline{WXO}$) information that is used to signal the next FIFO when it will be activated.

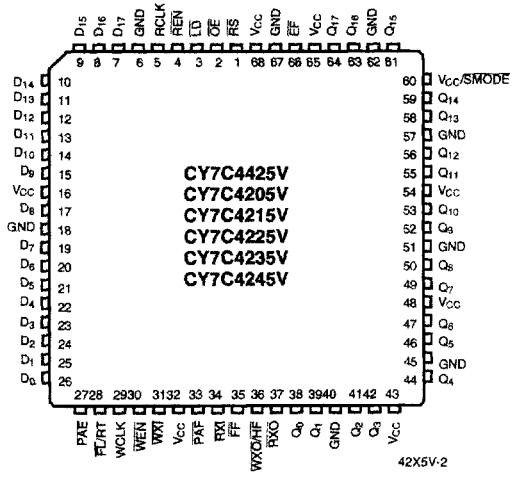
The Empty and Full flags are synchronous, i.e., they change state relative to either the read clock (RCLK) or the write clock (WCLK). When entering or exiting the Empty states, the flag is updated exclusively by the RCLK. The flag denoting Full states is updated exclusively by WCLK. The synchronous flag architecture guarantees that the flags will remain valid from one clock cycle to the next. As mentioned previously, the Almost Empty/Almost Full flags become synchronous if the V_{CC}/$\overline{SMODE}$ is tied to V_{SS}. All configurations are fabricated using an advanced 0.65µ P-Well CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of guard rings.

Logic Block Diagram

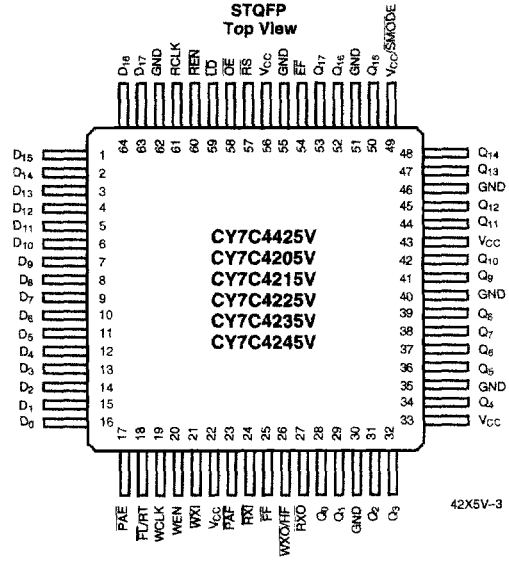


Pin Configurations

PLCC
Top View



STQFP
Top View



Selection Guide

		CY7C42X5V-15	CY7C42X5V-25	CY7C42X5V-35
Maximum Frequency (MHz)		66.7	40	28.6
Maximum Access Time (ns)		11	15	20
Minimum Cycle Time (ns)		15	25	35
Minimum Data or Enable Set-Up (ns)		4	6	7
Minimum Data or Enable Hold (ns)		1	1	2
Maximum Flag Delay (ns)		11	15	20
Operating Current (mA)	Commercial	30	30	30

	CY7C4425V	CY7C4205V	CY7C4215V	CY7C4225V	CY7C4235V	CY7C4245V
Density	64 x 18	256 x 18	512 x 18	1K x 18	2K x 18	4K x 18
Packages	68-pin PLCC, 64-pin 10x10 STQFP	68-pin PLCC, 64-pin 10x10 STQFP	68-pin PLCC, 64-pin 10x10 STQFP	68-pin PLCC, 64-pin 10x10 STQFP	68-pin PLCC, 64-pin 10x10 STQFP	68-pin PLCC, 64-pin 10x10 STQFP

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Pin Definitions

Signal Name	Description	I/O	Function
D_{0-17}	Data Inputs	I	Data inputs for an 18-bit bus
Q_{0-17}	Data Outputs	O	Data outputs for an 18-bit bus
$\overline{WEN}$	Write Enable	I	Enables the WCLK input
$\overline{REN}$	Read Enable	I	Enables the RCLK input
WCLK	Write Clock	I	The rising edge clocks data into the FIFO when $\overline{WEN}$ is LOW and the FIFO is not Full. When $\overline{LD}$ is asserted, WCLK writes data into the programmable flag-offset register.
RCLK	Read Clock	I	The rising edge clocks data out of the FIFO when $\overline{REN}$ is LOW and the FIFO is not Empty. When $\overline{LD}$ is asserted, RCLK reads data out of the programmable flag-offset register.
$\overline{WXO}/\overline{HF}$	Write Expansion Out/Half Full Flag	O	Dual-Mode Pin: Single device or width expansion - Half Full status flag. Cascaded - Write Expansion Out signal, connected to $\overline{WXI}$ of next device.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full. $\overline{FF}$ is synchronized to WCLK.
$\overline{PAE}$	Programmable Almost Empty	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the almost-empty offset value programmed into the FIFO. $\overline{PAE}$ is asynchronous when $V_{CC}/\overline{SMODE}$ is tied to V_{CC}; it is synchronized to RCLK when $V_{CC}/\overline{SMODE}$ is tied to V_{SS}.
$\overline{PAF}$	Programmable Almost Full	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO. $\overline{PAF}$ is asynchronous when $V_{CC}/\overline{SMODE}$ is tied to V_{CC}; it is synchronized to WCLK when $V_{CC}/\overline{SMODE}$ is tied to V_{SS}.
$\overline{LD}$	Load	I	When $\overline{LD}$ is LOW, D_{0-17} (O_{0-17}) are written (read) into (from) the programmable-flag-offset register.
$\overline{FL}/\overline{RT}$	First Load/ Retransmit	I	Dual-Mode Pin: Cascaded - The first device in the daisy chain will have $\overline{FL}$ tied to V_{SS}; all other devices will have $\overline{FL}$ tied to V_{CC}. In standard mode of width expansion, $\overline{FL}$ is tied to V_{SS} on all devices. Not Cascaded - Tied to V_{SS}. Retransmit function is also available in stand-alone mode by strobing $\overline{RT}$.
$\overline{WXI}$	Write Expansion Input	I	Cascaded - Connected to $\overline{WXO}$ of previous device. Not Cascaded - Tied to V_{SS}.
$\overline{RXI}$	Read Expansion Input	I	Cascaded - Connected to $\overline{RXO}$ of previous device. Not Cascaded - Tied to V_{SS}.

Pin Definitions (continued)

Signal Name	Description	I/O	Function
$\overline{RXO}$	Read Expansion Output	O	Cascaded - Connected to $\overline{RXI}$ of next device.
$\overline{RS}$	Reset	I	Resets device to empty condition. A reset is required before an initial read or write operation after power-up.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the FIFO's data outputs drive the bus to which they are connected. If $\overline{OE}$ is HIGH, the FIFO's outputs are in High Z (high-impedance) state.
$V_{CC}/\overline{SMODE}$	Synchronous Almost Empty/ Almost Full Flags	I	Dual-Mode Pin Asynchronous Almost Empty/Almost Full flags - tied to V_{CC}. Synchronous Almost Empty/Almost Full flags - tied to V_{SS}. (Almost Empty synchronized to RCLK, Almost Full synchronized to WCLK.)

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +5.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to V_{CC}+0.5V

DC Input Voltage ..... –0.5V to +5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 300mV

Electrical Characteristics Over the Operating Range[1]

Parameter	Description	Test Conditions		7C42X5V-15 Min.	7C42X5V-15 Max.	7C42X5V-25 Min.	7C42X5V-25 Max.	7C42X5V-35 Min.	7C42X5V-35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage	Low = 2.0V High = V_{CC} +0.5V		2.0	5.0	2.0	5.0	2.0	5.0	V
V_{IL}[2]	Input LOW Voltage	Low = –3.0V High = 0.8 V		–0.5	0.8	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		–10	10	–10	10	–10	10	µA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		–10	+10	–10	+10	–10	+10	µA
I_{CC}[3]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		30		30		30	mA
I_{SB}[4]	Standby Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		6		6		6	mA

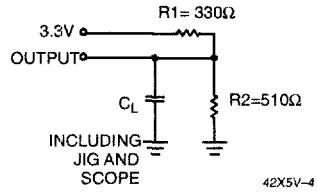
Capacitance[5]

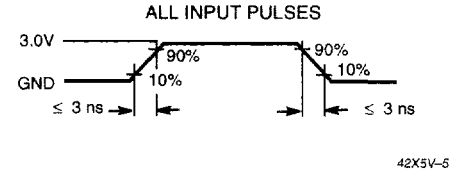
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

Notes:

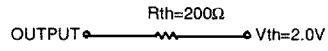
1. See the last page of this specification for Group A subgroup testing information.
2. The V_{IH} and V_{IL} specifications apply for all inputs except $\overline{WXI}$, $\overline{RXI}$. The $\overline{WXI}$, $\overline{RXI}$ pin is not a TTL input. It is connected to either $\overline{RXO}$, $\overline{WXO}$ of the previous device or V_{SS}.
3. Input signals switch from 0V to 3V with a rise/fall time less than 3 ns, clocks and clock enables switch at 20 MHz, while the data inputs switch at 10 MHz. Outputs are unloaded.
4. All inputs = V_{CC} – 0.2V, except WCLK and RCLK, which are switching at 20MHz.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[6, 7]





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range

Parameter	Description	7C42X5V-15		7C42X5V-25		7C42X5V-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_S	Clock Cycle Frequency		66.7		40		28.6	MHz
t_A	Data Access Time	2	11	2	15	2	20	ns
t_{CLK}	Clock Cycle Time	15		25		35		ns
t_{CLKH}	Clock HIGH Time	6		10		14		ns
t_{CLKL}	Clock LOW Time	6		10		14		ns
t_{DS}	Data Set-Up Time	4		6		7		ns
t_{DH}	Data Hold Time	1		2		2		ns
t_{ENS}	Enable Set-Up Time	4		6		7		ns
t_{ENH}	Enable Hold Time	1		2		2		ns
t_{RS}	Reset Pulse Width[8]	15		25		35		ns
t_{RSR}	Reset Recovery Time	10		15		20		ns
t_{RSF}	Reset to Flag and Output Time		15		25		35	ns
t_{PRT}	Retransmit Pulse Width	15		25		35		ns
t_{RTR}	Retransmit Recovery Time	15		25		35		ns
t_{OLZ}	Output Enable to Output in Low Z[9]	0		0		0		ns
t_{OE}	Output Enable to Output Valid	3	8	3	12	3	15	ns
t_{OHZ}	Output Enable to Output in High Z[9]	3	8	3	12	3	15	ns
t_{WFF}	Write Clock to Full Flag		11		15		20	ns
t_{REF}	Read Clock to Empty Flag		11		15		20	ns
$t_{PAFasynch}$	Clock to Programmable Almost-Full Flag[10] (Asynchronous mode, V_{CC}/SMODE tied to V_{CC})		18		22		25	ns
$t_{PAFsynch}$	Clock to Programmable Almost-Full Flag (Synchronous mode, V_{CC}/SMODE tied to V_{SS})		11		15		20	ns
$t_{PAEasynch}$	Clock to Programmable Almost-Empty Flag[10] (Asynchronous mode, V_{CC}/SMODE tied to V_{CC})		18		22		25	ns
$t_{PAEsynch}$	Clock to Programmable Almost-Full Flag (Synchronous mode, V_{CC}/SMODE tied to V_{SS})		11		15		20	ns

Notes:

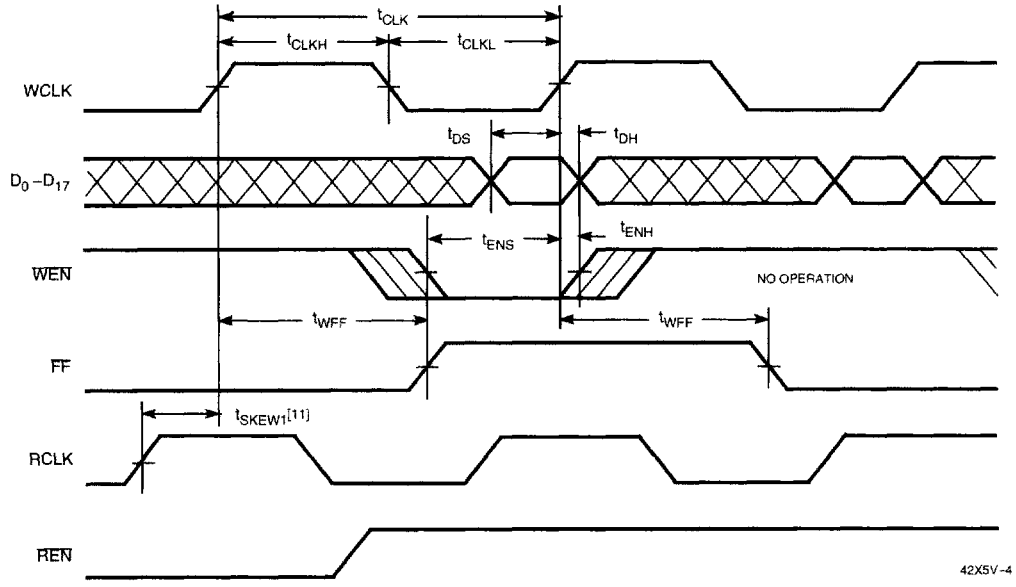
6. C_L = 30 pF for all AC parameters except for t_{OHZ}.
7. C_L = 5 pF for t_{OHZ}.
8. Pulse widths less than minimum values are not allowed.
9. Values guaranteed by design, not currently tested.
10. $t_{PAFasynch}$, $t_{PAEasynch}$, after program register write will not be valid until 5 ns + $t_{PAF(E)}$.

Switching Characteristics Over the Operating Range (continued)

Parameter	Description	7C42X5V-15		7C42X5V-25		7C42X5V-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{HF}	Clock to Half-Full Flag		16		20		25	ns
t_{XO}	Clock to Expansion Out		10		15		20	ns
t_{XI}	Expansion in Pulse Width	6.5		10		14		ns
t_{XIS}	Expansion in Set-Up Time	5		10		15		ns
t_{SKEW1}	Skew Time between Read Clock and Write Clock for Full Flag	6		10		12		ns
t_{SKEW2}	Skew Time between Read Clock and Write Clock for Empty Flag	6		10		12		ns
t_{SKEW3}	Skew Time between Read Clock and Write Clock for Programmable Almost Empty and Programmable Almost Full Flags.	15		18		20		ns

Switching Waveforms

Write Cycle Timing

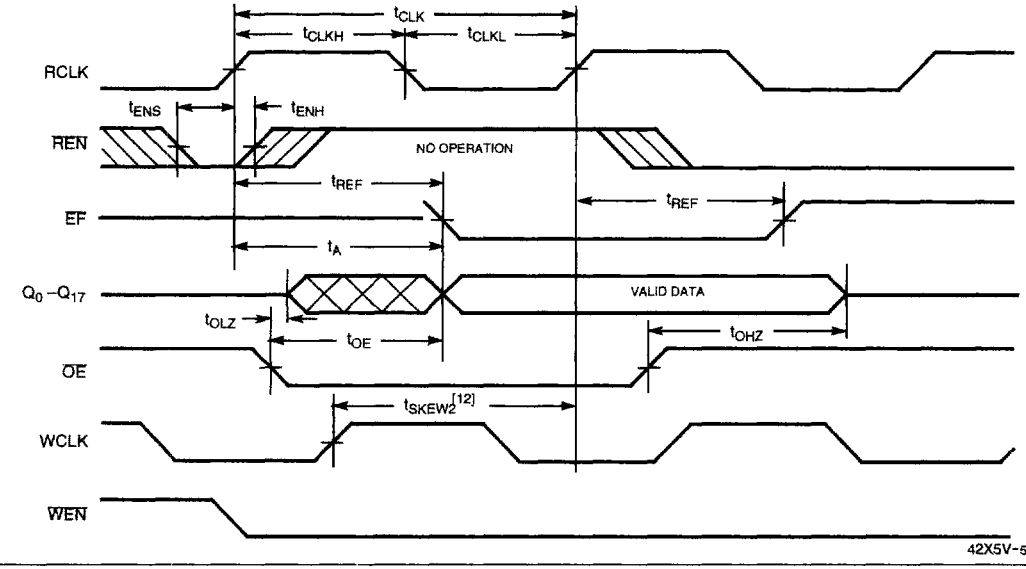


Note:

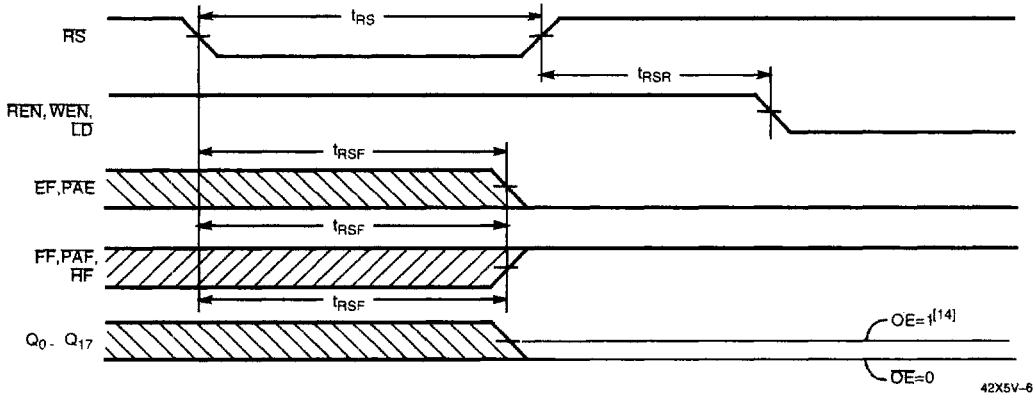
11. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that FF will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then FF may not change state until the next WCLK edge.

Switching Waveforms (continued)

Read Cycle Timing



Reset Timing[13]

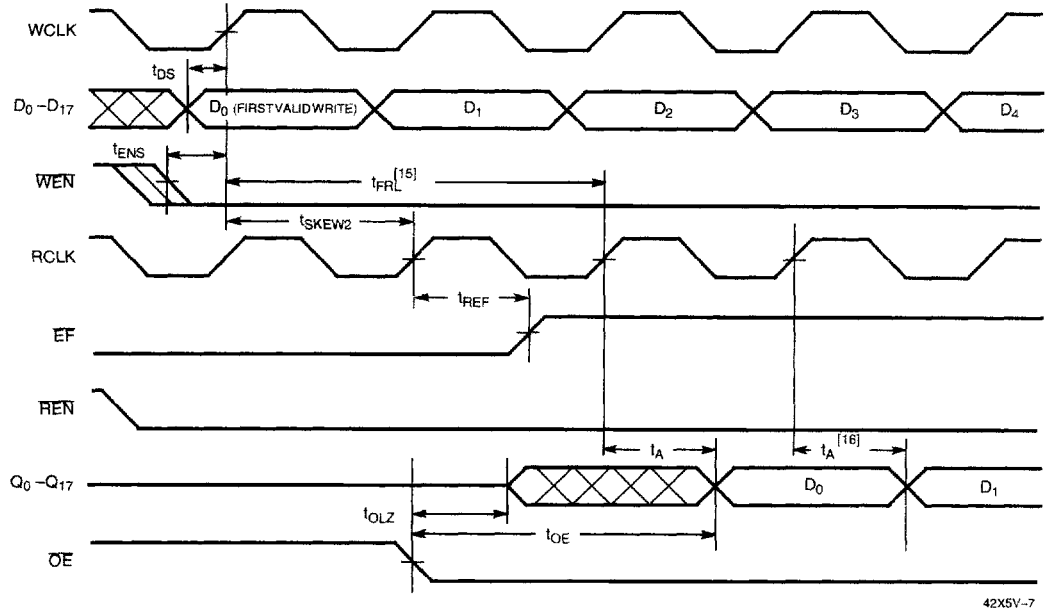


Notes:

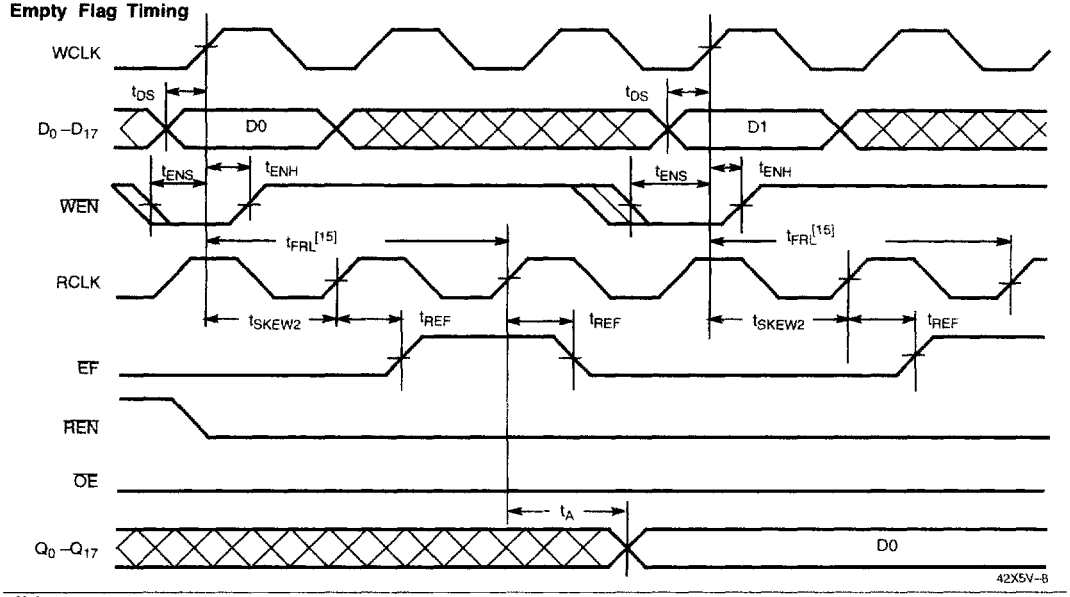
12. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ may not change state until the next RCLK edge.
13. The clocks (RCLK, WCLK) can be free-running during reset.
14. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and three-state if $\overline{OE}$ = 1.

Switching Waveforms (continued)

First Data Word Latency after Reset with Simultaneous Read and Write



Empty Flag Timing

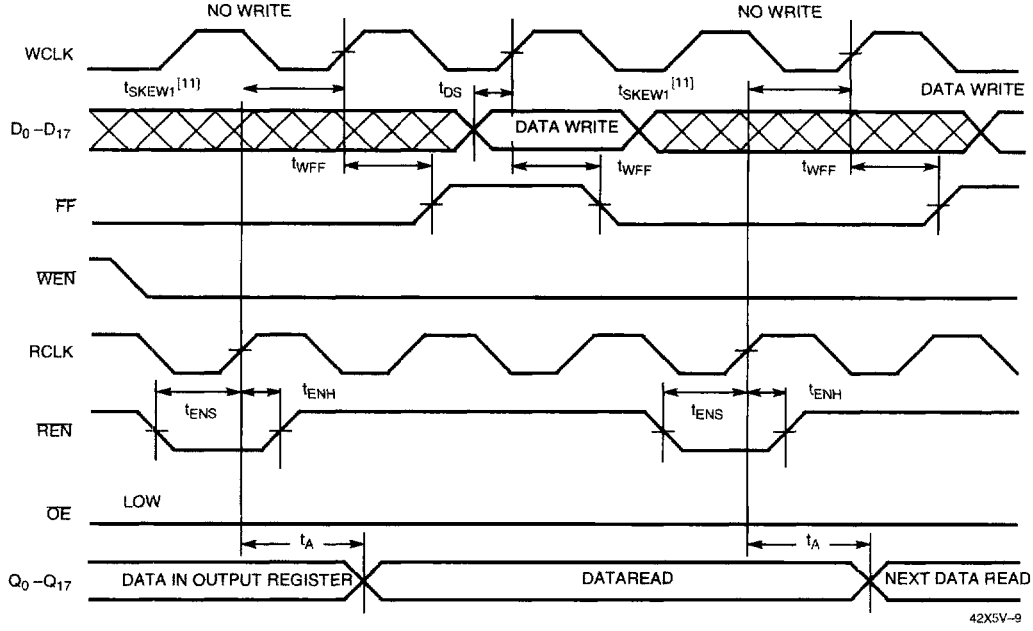


Notes:

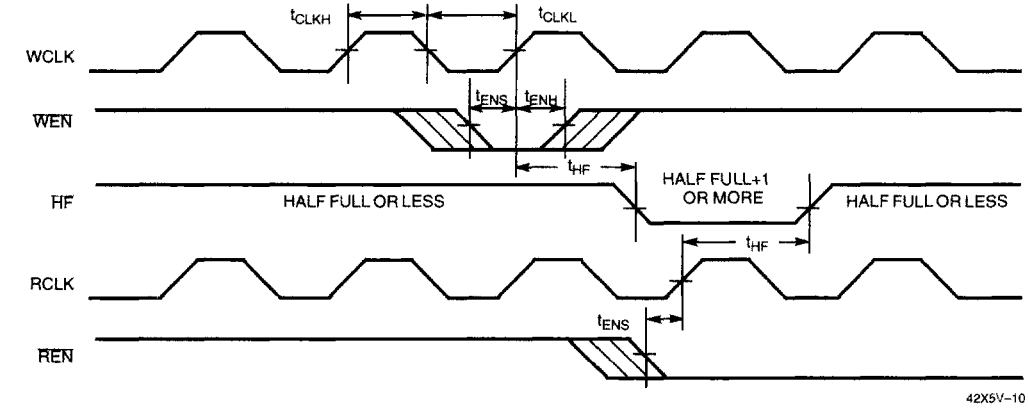
15. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = $t_{CLK} + t_{SKEW2}$. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either $2*t_{CLK} + t_{SKEW2}$ or $t_{CLK} + t_{SKEW2}$. The Latency Timing applies only at the Empty Boundary (EF = LOW).
16. The first word is available the cycle after EF goes HIGH, always.

Switching Waveforms (continued)

Full Flag Timing

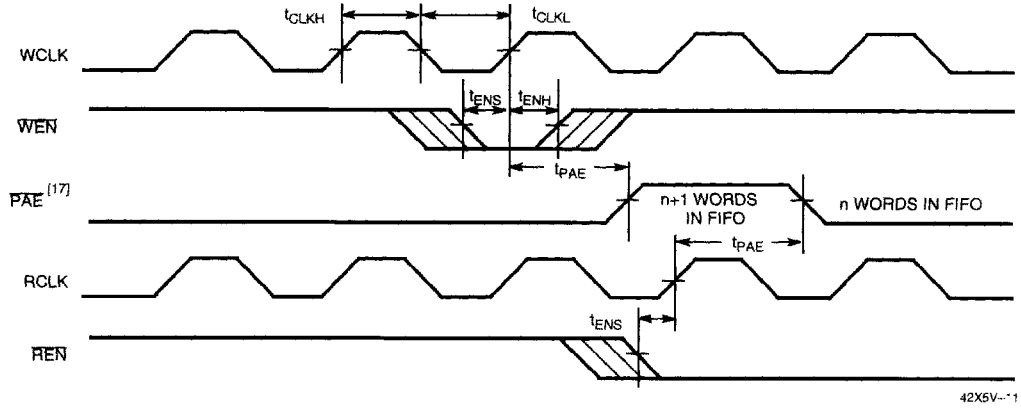


Half-Full Flag Timing

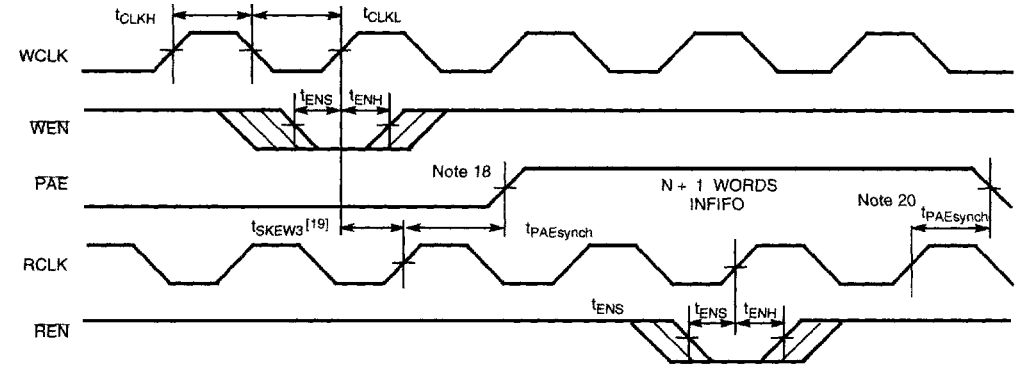


Switching Waveforms (continued)

Programmable Almost Empty Flag Timing



Programmable Almost Empty Flag Timing (applies only in SMODE (SMODE is LOW)

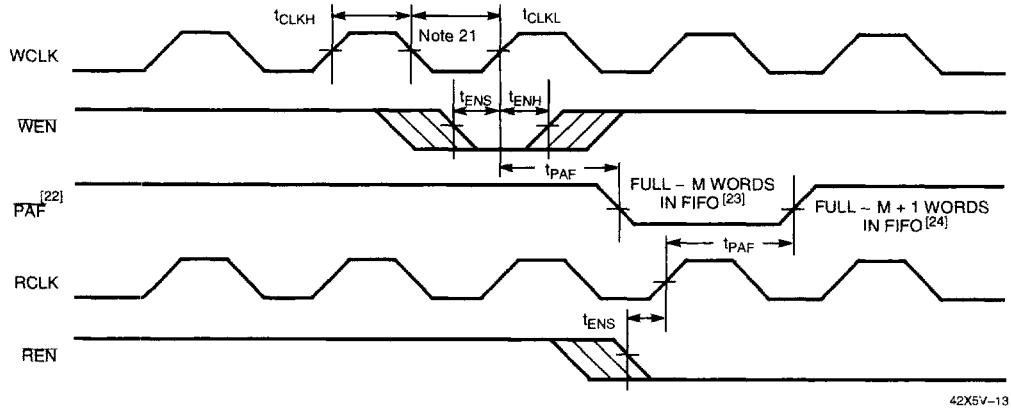


Notes:

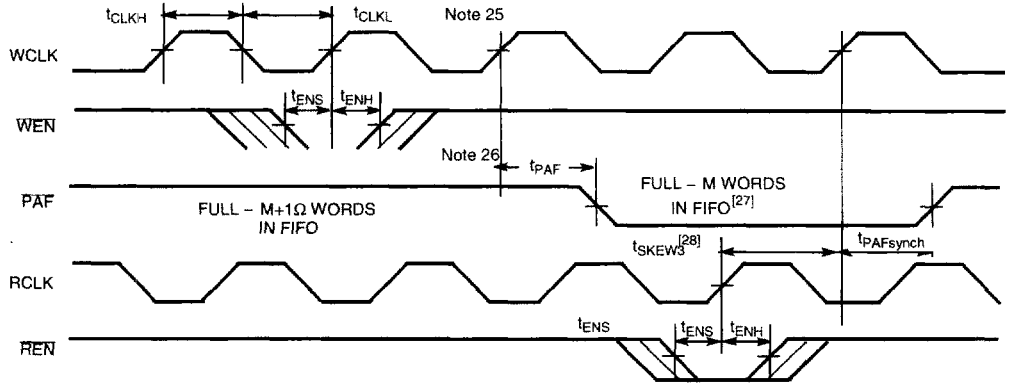
17. PAE offset –n. Number of data words into FIFO already = n.
18. PAE offset –n.
19. t_{SKEW3} is the minimum time between a rising WCLK and a rising RCLK edge for PAE to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than t_{SKEW3}, then PAE may not change state until the next RCLK.
20. If a read is performed on this rising edge of the read clock, there will be Empty + (n–1) words in the FIFO when PAE goes LOW.

Switching Waveforms (continued)

Programmable Almost Full Flag Timing



Programmable Almost Full Flag Timing (applies only in SMODE (SMODE in LOW))

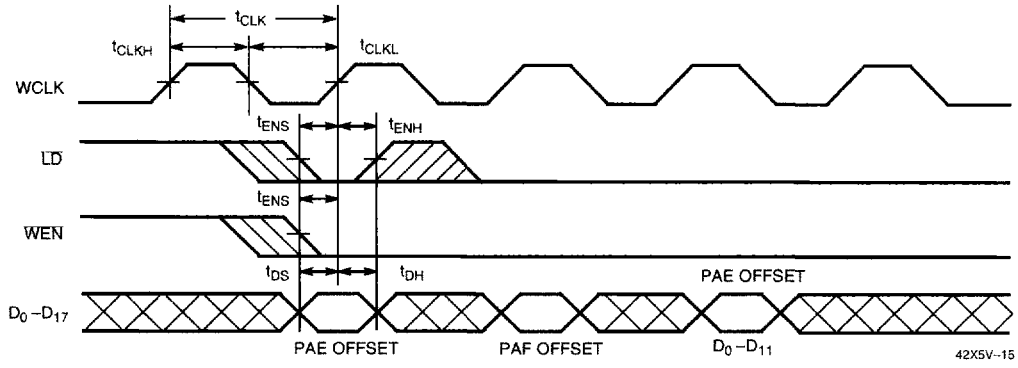


Notes:

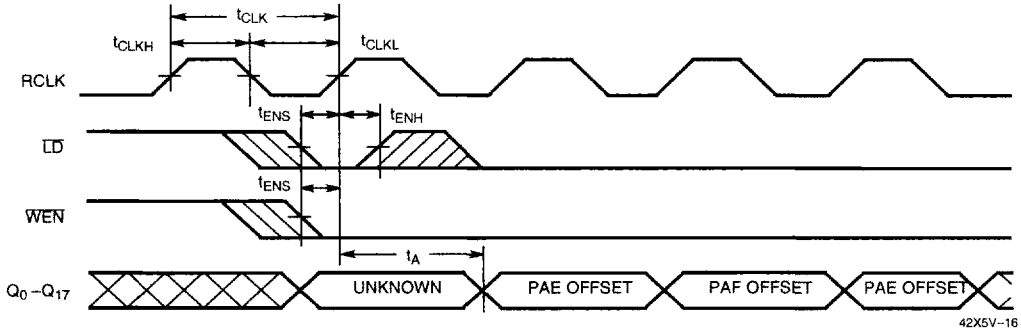
21. PAF offset = m. Number of data words written into FIFO already = 64 – m + 1 for the CY7C4425V, 256 – m + 1 for the CY7C4205V, 512 – m + 1 for the CY7C4215V. *1024 – m + 1 for the CY7C4225V, 2048 – m + 1 for the CY7C4235V, and 4096 – m + 1 for the CY7C4245V.*
22. PAF is offset = m.
23. 64 – m words in CY7C4425V, 256 - m words inCY7C4205V, 512 – m word in CY7C4215V. 1024 - m words in CY7C4225V, 2048 – m words in CY7C4235V, and 4096 – m words in CY7C4245V.
24. *64 – m + 1 words in CY7C4425V, 256 – m + 1 words in CY7C4205V, 512 – m +1 words in CY7C4215V, 1024 – m + 1 CY7C4225V, 2048 – m + 1 in CY74235V,* and 4096 – m + 1 words in CY7C4245V.
25. If a write is performed on this rising edge of the write clock, there will be Full - (m-1) words of the FIFO when PAF goes LOW.
26. PAF offset = m.
27. *64 – m words in CY7C4425V, 256 – m words in FIFO for CY7C4205V, 512 – m word in CY7C4215V, 1024 – m words in CY7C4225V, 2048 – m worcs in* CY7C4235V, and 4096 – m words in CY7C4245V.
28. t_{SKEW3} is the minimum time between a rising RCLK and a rising WCLK edge for PAF to change state during that clock cycle. If the time between the edge of RCLK and the rising edge of WCLK is less than t_{SKEW3}, then PAF may not change state until the next WCLK rising edge.

Switching Waveforms (continued)

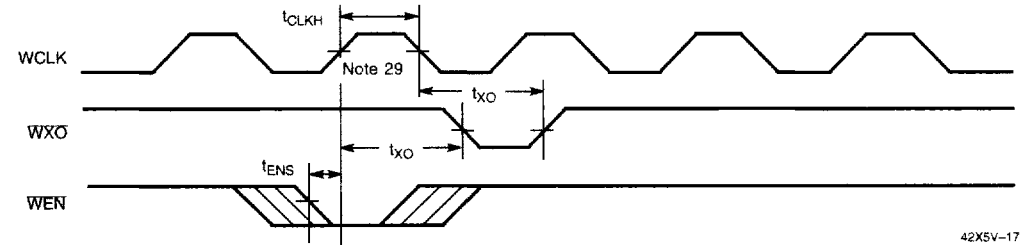
Write Programmable Registers



Read Programmable Registers



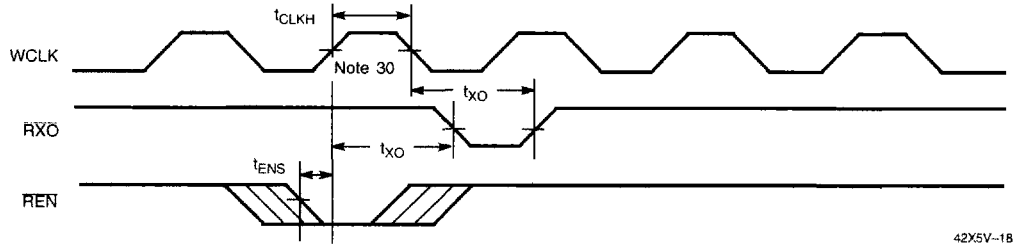
Write Expansion Out Timing



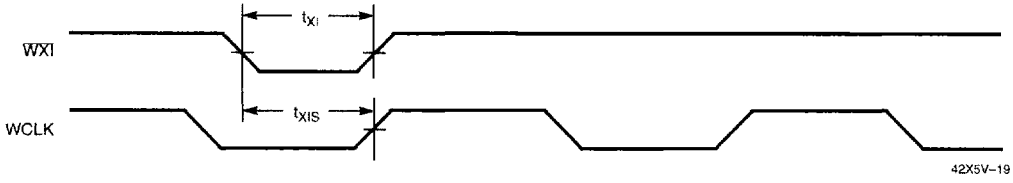
Note:
29. Write to Last Physical Location.

Switching Waveforms (continued)

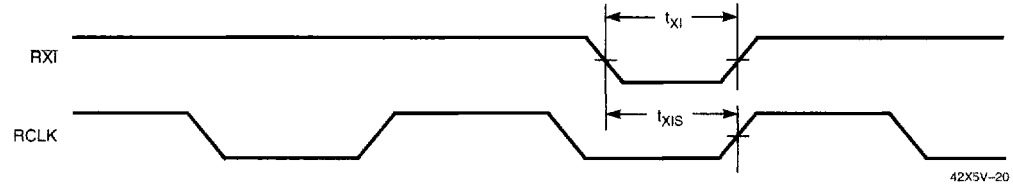
Read Expansion Out Timing



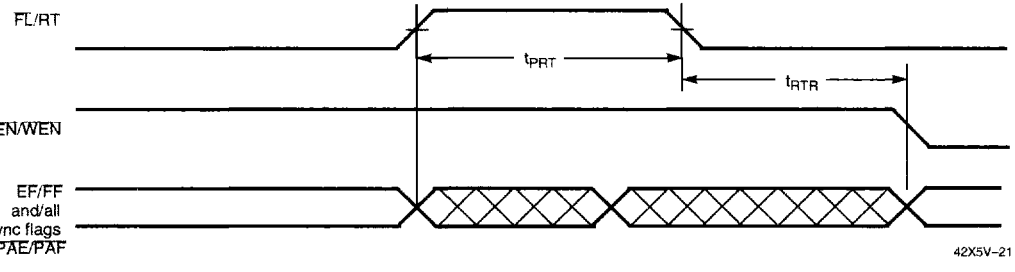
Write Expansion In Timing



Read Expansion In Timing



Retransmit Timing[31, 32, 33]



Notes:

30. Read from Last Physical Location
31. Clocks are free running in this case.
32. The flags may change state during Retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTR}.
33. For the synchronous $\overline{PAE}$ and $\overline{PAF}$ flags (SMODE), an appropriate clock cycle is necessary after t_{RTR} to update these flags.

Architecture

The CY7C42X5V consists of an array of 64 to 4K words of 18 bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (RCLK, WCLK, $\overline{REN}$, $\overline{WEN}$, $\overline{RS}$), and flags ($\overline{EF}$, $\overline{PAE}$, $\overline{HF}$, $\overline{PAF}$, $\overline{FF}$). The CY7C42X5V also includes the control signals $\overline{WXI}$, $\overline{RXI}$, $\overline{WXO}$, $\overline{RXO}$ for depth expansion.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Reset ($\overline{RS}$) cycle. This causes the FIFO to enter the Empty condition signified by $\overline{EF}$ being LOW. All data outputs go LOW after the falling edge of $\overline{RS}$ only if $\overline{OE}$ is asserted. In order for the FIFO to reset to its default state, a falling edge must occur on $\overline{RS}$ and the user must not read or write while $\overline{RS}$ is LOW.

FIFO Operation

When the $\overline{WEN}$ signal is active (LOW), data present on the D_{0-17} pins is written into the FIFO on each rising edge of the WCLK signal. Similarly, when the $\overline{REN}$ signal is active LOW, data in the FIFO memory will be presented on the Q_{0-17} outputs. New data will be presented on each rising edge of RCLK while $\overline{REN}$ is active LOW and $\overline{OE}$ is LOW. $\overline{REN}$ must set up tENS before RCLK for it to be a valid read function. $\overline{WEN}$ must occur tENS before WCLK for it to be a valid write function.

An output enable ($\overline{OE}$) pin is provided to three-state the Q_{0-17} outputs when $\overline{OE}$ is de-asserted. When $\overline{OE}$ is enabled (LOW), data in the output register will be available to the Q_{0-17} outputs after t_{OE}. If devices are cascaded, the $\overline{OE}$ function will only output data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-17} outputs even after additional reads occur.

Programming

The CY7C42X5V devices contain two 12-bit offset registers. Data present on D0-11 during a program write will determine the distance from Empty (Full) that the Almost Empty (Almost Full) flags become active. If the user elects not to program the FIFO's flags, the default offset values are used (see *Table 2*). When the Load $\overline{LD}$ pin is set LOW and $\overline{WEN}$ is set LOW, data on the inputs D0 - 11 is written into the Empty offset register on the first LOW-to-HIGH transition of the write clock (WCLK). When the $\overline{LD}$ pin and $\overline{WEN}$ are held LOW then data is written into the Full offset register on the second LOW-to-HIGH transition of the write clock (WCLK). The third transition of the write clock (WCLK) again writes to the Empty offset register (see *Table 1*). Writing all offset registers does not have to occur at one time. One or two offset registers can be written and then, by bringing the $\overline{LD}$ pin HIGH, the FIFO is returned to normal read/write operation. When the $\overline{LD}$ pin is set LOW, and $\overline{WEN}$ is LOW, the next offset register in sequence is written.

The contents of the offset registers can be read on the output lines when the $\overline{LD}$ pin is set LOW and $\overline{REN}$ is set LOW; then, data can be read on the LOW-to-HIGH transition of the read clock (RCLK).

Table 1. Write Offset Register

$\overline{LD}$	$\overline{WEN}$	WCLK[34]	Selection
0	0		Writing to offset registers: Empty Offset Full Offset 
0	1		No Operation
1	0		Write Into FIFO
1	1		No Operation

Note:
34. The same selection sequence applies to reading from the registers. $\overline{REN}$ is enabled and read is performed on the LOW-to-HIGH transition of RCLK.

Flag Operation

The CY7C42X5V devices provide five flag pins to indicate the condition of the FIFO contents. Empty and Full are synchronous. $\overline{PAE}$ and $\overline{PAF}$ are synchronous if V_{CC}/$\overline{SMODE}$ is tied to V_{SS}.

Full Flag

The Full Flag ($\overline{FF}$) will go LOW when device is Full. Write operations are inhibited whenever $\overline{FF}$ is LOW regardless of the state of $\overline{WEN}$. $\overline{FF}$ is synchronized to WCLK, i.e., it is exclusively updated by each rising edge of WCLK.

Empty Flag

The Empty Flag ($\overline{EF}$) will go LOW when the device is empty. Read operations are inhibited whenever $\overline{EF}$ is LOW, regardless of the state of $\overline{REN}$. $\overline{EF}$ is synchronized to RCLK, i.e., it is exclusively updated by each rising edge of RCLK.

Programmable Almost Empty/Almost Full Flag

The CY7C42X5V features programmable Almost Empty and Almost Full Flags. Each flag can be programmed (described in the Programming section) a specific distance from the corresponding boundary flags (Empty or Full). When the FIFO contains the number of words or fewer for which the flags have been programmed, the $\overline{PAF}$ or $\overline{PAE}$ will be asserted, signifying that the FIFO is either Almost Full or Almost Empty. See *Table 2* for a description of programmable flags.

When the $\overline{SMODE}$ pin is tied LOW, the $\overline{PAF}$ flag signal transition is caused by the rising edge of the write clock and the $\overline{PAE}$ flag transition is caused by the rising edge of the read clock.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

The Retransmit (RT) input is active in the stand-alone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred since the last $\overline{RS}$ cycle. A HIGH pulse on RT resets the internal read pointer to the first physical location of the FIFO. WCLK and RCLK may be free running but must be disabled during and tRTR after the retransmit pulse. With every valid read cycle after retransmit, previously accessed data is read and the

read pointer is incremented until it is equal to the write pointer. Flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of RT are transmitted also.

The full depth of the FIFO can be repeatedly retransmitted.

Table 2. Flag Truth Table

Number of Words in FIFO							
7C4425V - 64 x 18	7C4205V - 256 x 18	7C4215V - 512 x 18	FF	PAF	HF	PAE	EF
0	0	0	H	H	H	L	L
1 to n[35]	1 to n[35]	1 to n[35]	H	H	H	L	H
(n+1) to 32	(n+1) to 128	(n+1) to 256	H	H	H	H	H
33 to (64–(m+1))	129 to (256–(m+1))	257 to (512–(m+1))	H	H	L	H	H
(64–m)[36] to 63	(256–m)[36] to 255	(512–m)[36] to 511	H	L	L	H	H
64	256	512	L	L	L	H	H

Number of Words in FIFO							
7C4225V - 1K x 18	7C4235V - 2K x 18	7C4245V - 4K x 18	FF	PAF	HF	PAE	EF
0	0	0	H	H	H	L	L
1 to n[35]	1 to n[35]	1 to n[35]	H	H	H	L	H
(n+1) to 512	(n+1) to 1024	(n+1) to 2048	H	H	H	H	H
513 to (1024 –(m+1))	1025 to (2048 –(m+1))	2049 to (4096 –(m+1))	H	H	L	H	H
(1024–m)[36] to 1023	(2048–m)[36] to 2047	(4096–m)[36] to 4095	H	L	L	H	H
1024	2048	4096	L	L	L	H	H

Notes:
35. n = Empty Offset (Default Values: CY7C4425V n = 7, CY7C4205V n = 31, CY7C4215V n = 63, CY7C4225V/7C4235V/7C4245V n = 127).
36. m = Full Offset (Default Values: CY7C4425V n = 7, CY7C4205V n = 31, CY7C4215V n = 63, CY7C4225V/7C4235V/7C4245V n = 127).

Width Expansion Configuration

The CY7C42X5V can be expanded in width to provide word widths greater than 18 in increments of 18. During width expansion mode all control line inputs are common and all flags are available. Empty (Full) flags should be created by ANDing the Empty (Full) flags of every FIFO. This technique will avoid ready data from the FIFO that is "staggered" by one clock cycle due to the variations in skew between RCLK and WCLK. *Figure 2* demonstrates a 36-word width by using two CY7C42X5.V

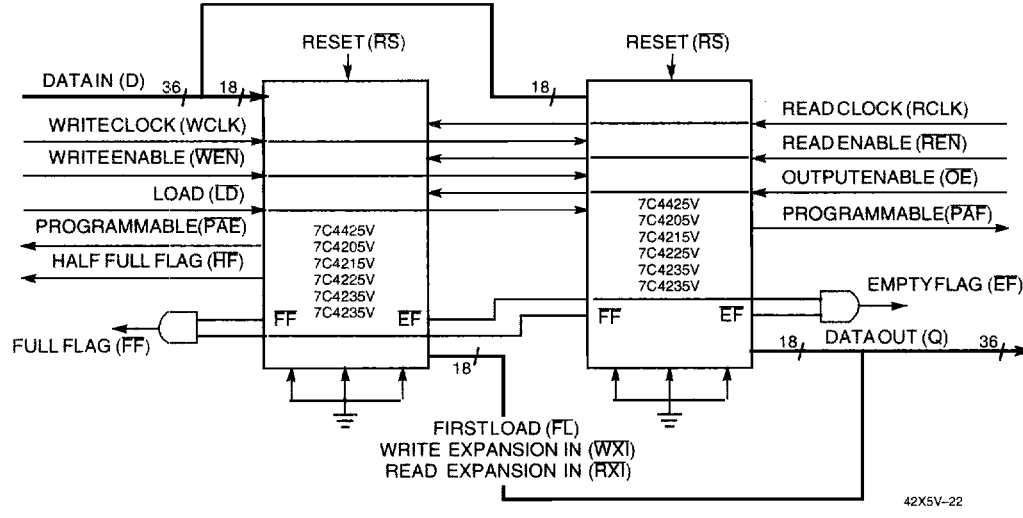


Figure 1. Block Diagram of Low Voltage Synchronous FIFO Memories Used in a Width Expansion Configuration

Depth Expansion Configuration (with Programmable Flags)

The CY7C42X5V can easily be adapted to applications requiring more than 64/256/512/1024/2048/4096 words of buffering. *Figure 2* shows Depth Expansion using three CY7C42X5Vs. Maximum depth is limited only by signal loading. Follow these steps:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the HIGH state.
3. The Write Expansion Out ($\overline{WXO}$) pin of each device must be tied to the Write Expansion In ($\overline{WXI}$) pin of the next device.
4. The Read Expansion Out ($\overline{RXO}$) pin of each device must be tied to the Read Expansion In ($\overline{RXI}$) pin of the next device.
5. All Load ($\overline{LD}$) pins are tied together.
6. The Half-Full Flag ($\overline{HF}$) is not available in the Depth Expansion Configuration.
7. $\overline{EF}$, $\overline{FF}$, $\overline{PAE}$, and $\overline{PAF}$ are created with composite flags by ORing together these respective flags for monitoring. The composite $\overline{PAE}$ and $\overline{PAF}$ flags are not precise.

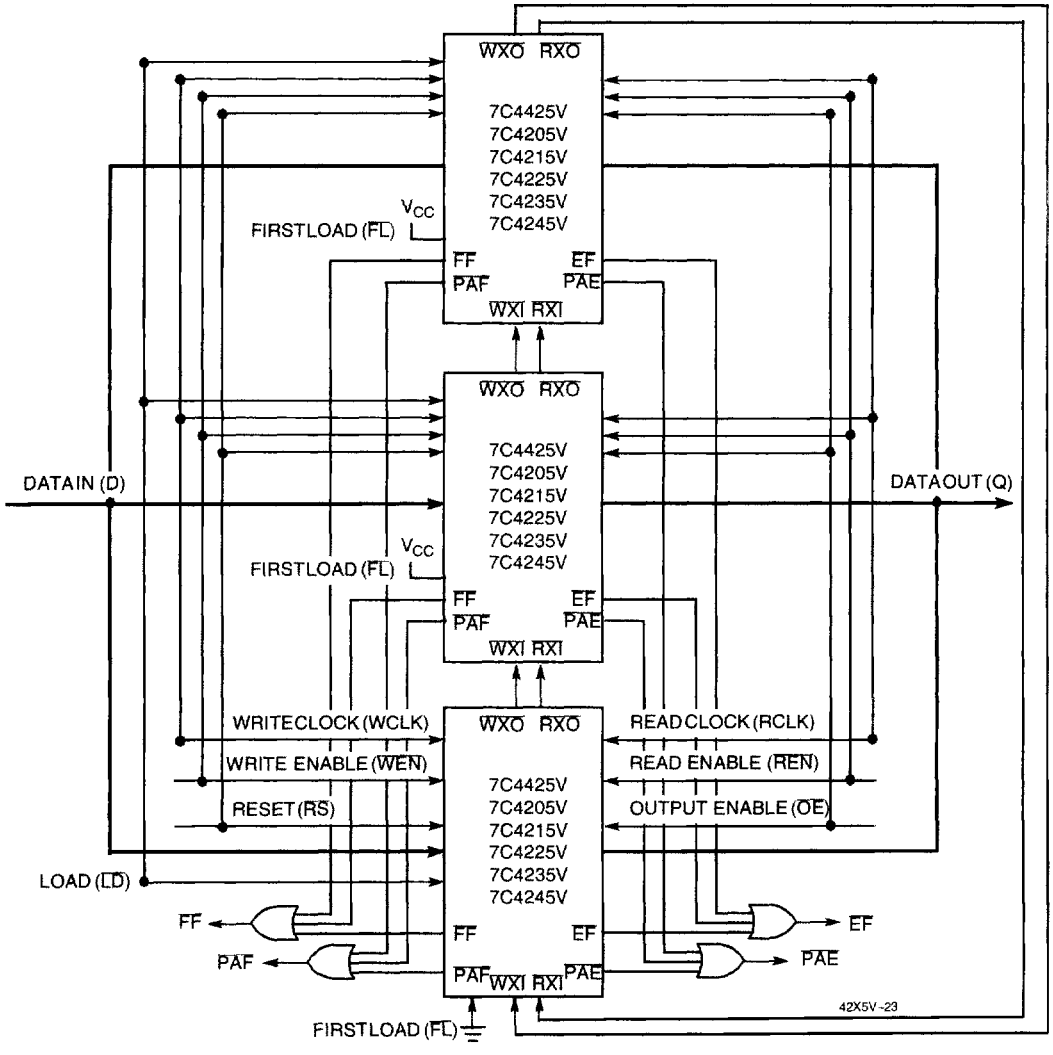


Figure 2. Block Diagram of Low Voltage Synchronous FIFO Memory with Programmable Flags used in Depth Expansion Configuration

Ordering Information

64 x 18 Low Voltage Synchronous FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C4425V-15ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial
	CY7C4425V-15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4425V-25ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial
	CY7C4425V-25JC	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4425V-35ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial
	CY7C4425V-35JC	J81	68-Lead Plastic Leaded Chip Carrier	

256 x 18 Low Voltage Synchronous FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C4205V-15ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial
	CY7C4205V-15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4205V-25ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial
	CY7C4205V-25JC	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4205V-35ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial
	CY7C4205V-35JC	J81	68-Lead Plastic Leaded Chip Carrier	

512 x 18 Low Voltage Synchronous FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C4215V-15ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial
	CY7C4215V-15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4215V-25ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial
	CY7C4215V-25JC	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4215V-35ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial
	CY7C4215V-35JC	J81	68-Lead Plastic Leaded Chip Carrier	

1K x 18 Low Voltage Synchronous FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C4225V-15ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial
	CY7C4225V-15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4225V-25ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial
	CY7C4225V-25JC	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4225V-35ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial
	CY7C4225V-35JC	J81	68-Lead Plastic Leaded Chip Carrier	

Ordering Information (continued)

2K x 18 Low Voltage Synchronous FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C4235V-15ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial
	CY7C4235V-15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4235V-25ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial
	CY7C4235V-25JC	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4235V-35ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial
	CY7C4235V-35JC	J81	68-Lead Plastic Leaded Chip Carrier	

4K x 18 Low Voltage Synchronous FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C4245V-15ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial
	CY7C4245V-15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4245V-25ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial
	CY7C4245V-25JC	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4245V-35ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial
	CY7C4245V-35JC	J81	68-Lead Plastic Leaded Chip Carrier	

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