

CERAMIC SMD CRYSTAL CLOCK OSCILLATOR WITH VOLTAGE CONTROL



7.0 x 5.0 x 1.8 mm

ALVD



FEATURES:

- Based on a proprietary digital multiplier
- Tri-State Output
- Low Phase Jitter
- 3.3V +/- 5% operation
- Ceramic SMD, low profile package

APPLICATIONS:

- SONET, xDSL
- SDH, CPE
- STB

STANDARD SPECIFICATIONS:

PARAMETERS	
ABRACON P/N:	ALVD Series
Frequency range:	750 KHz to 800 MHz
Operating temperature:	0°C to +70°C (see options)
Storage temperature:	-55°C to +125°C
Overall frequency stability:	±50 ppm max. (see options)
Supply voltage (V_{dd}):	3.3V ± 10%
Voltage control (V_c):	0.3VDC min, 1.65VDC typ, 3.0 VDC max.
Symmetry at 1/2 Vdd:	40/60% max.
Output Level:	See options (PECL, CMOS, or LVDS)
Pullability:	± 50ppm (see option)
Tristate Function:	"1" ($V_{IH} \geq 0.7 * V_{dd}$) or open: Oscillation "0" ($V_{IL} < 0.3 * V_{dd}$) : Hi Z
Aging per year:	±5 ppm max.
RMS Phase Jitter:	3ps typical, 5ps max. (12KHz~20MHz)
Period Jitter (peak to peak):	35 ps typical
Phase Noise:	-112 dBc/Hz @ 1kHz Offset from 155.52MHz -125 dBc/Hz @ 10kHz Offset from 155.52MHz -123 dBc/Hz @ 100KHz Offset from 155.52MHz -109 dBc/Hz @ 1kHz Offset from 622.08MHz -110 dBc/Hz @ 10kHz Offset from 622.08MHz -109 dBc/Hz @ 100KHz Offset from 622.08MHz
<p>PECL: Supply current (I_{DD}): 25mA max (for $F_o < 24\text{MHz}$), 65mA max (for $24\text{MHz} < F_o < 96\text{MHz}$), 100mA max ($96\text{MHz} < F_o < 800\text{MHz}$) Output Logic High: $V_{dd} - 1.025\text{V}$ min, $V_{dd} - 0.880\text{V}$ max. Output Logic Low: $V_{dd} - 1.810\text{V}$ min, $V_{dd} - 1.620\text{V}$ max. Symmetry (Duty Cycle): 45% min, 50% typ, 55% max, Rise time: 0.6nSec typ, 1.5nS max Fall time: 0.6nSec typ, 1.5nS max</p>	
<p>CMOS: Supply current (I_{DD}): 15 mA max (for $F_o < 24\text{MHz}$), 30mA max (for $24\text{MHz} < F_o < 96\text{MHz}$), 40mA max ($96\text{MHz} < F_o < 800\text{MHz}$) Output Clock Rise/ Fall Time [10%~90% VDD with 10pF load]: 1.2ns typ, 1.6ns max. Output Clock Duty Cycle [Measured @ 50% VDD]: 45% min, 50% typical, 55% max</p>	
<p>LVDS: Supply current (I_{DD}): 25mA max (for $F_o < 24\text{MHz}$), 45mA max (for $24\text{MHz} < F_o < 96\text{MHz}$), 80mA max ($96\text{MHz} < F_o < 800\text{MHz}$) Output Clock Duty Cycle @ 1.25V: 45% min, 50% typical, 55% max Output Differential Voltage (V_{OD}): 247mV min, 355mV typical, 454mV max VDD Magnitude Change (ΔV_{OD}): -50mV min, 50mV max Output High Voltage : $V_{OH} = 1.4\text{V}$ typical, 1.6V max. Output Low Voltage: $V_{OL} = 0.9\text{V}$ min, 1.1V typical Offset Voltage [$R_L = 100 \Omega$]: $V_{OS} = 1.125\text{V}$ min, 1.2V typical, 1.375V max Offset Magnitude Change [$R_L = 100 \Omega$]: $\Delta V_{OS} = 0\text{mV}$ min, 3mV typical, 25mV max Power-off Leakage (I_{OxD}) [$V_{out} = V_{DD}$ or GND, $V_{DD} = 0\text{V}$] = ±1 μA typical, ±10 μA max. Differential Clock Rise Time (t_r) [$R_L = 100 \Omega$, $CL = 10\text{pF}$]: 0.2nS min, 0.7nS typical, 1.0nS,max Differential Clock Fall Time (t_f) [$R_L = 100 \Omega$, $CL = 10\text{pF}$]: 0.2nS min, 0.7nS typical, 1.0nS max</p>	

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PIN ASSIGNMENTS

PIN #	Name	DESCRIPTION
1	Vc	Voltage Control
2	Tristate	Tristate
3	GND	Ground
4	Q	PECL, LVDS, or CMOS Output.
5	Q	Complimentary PECL, LVDS, or NC.
6	V _{DD}	VDD Connection.

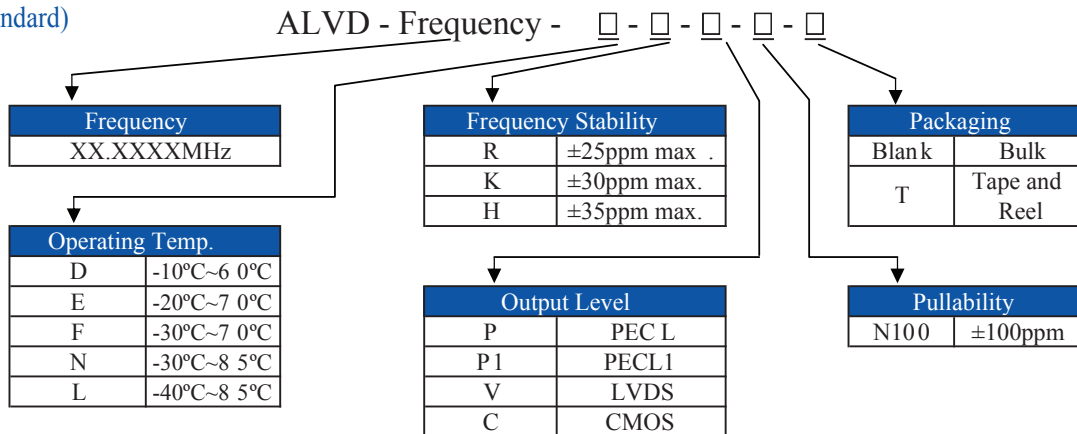
TRI-STATE PIN OPERATION:

OUTPUT TYPE OPTION	PIN 2 logic level*	Output State (Tri-state)
P PECL	0 (Default)	Enabled
	1	Disabled
P1 PECL1	0	Disabled
	1	Enabled
V LVDS	0	Disabled
	1(Default)	Enabled
C CMOS	0	Disabled
	1(Default)	Enabled

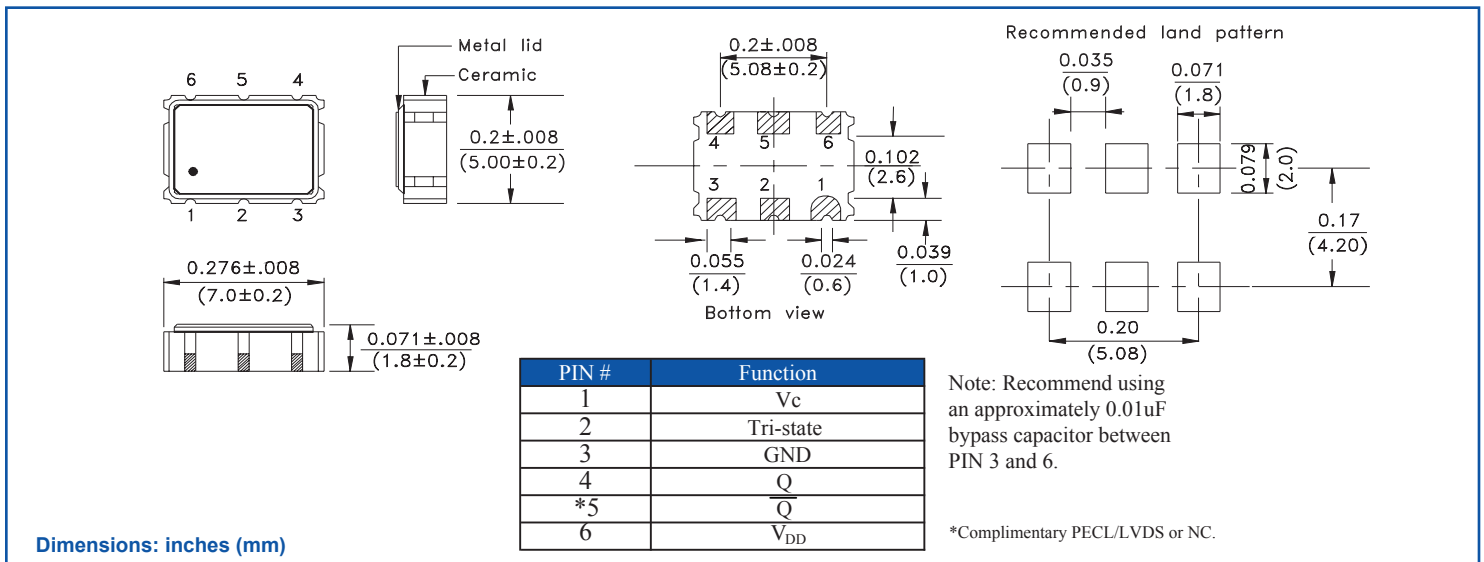
*Connect to VDD for logic level "1", connect to ground for logic level "0".

OPTIONS & PART IDENTIFICATION:

(Left blank if standard)



OUTLINE DRAWING:



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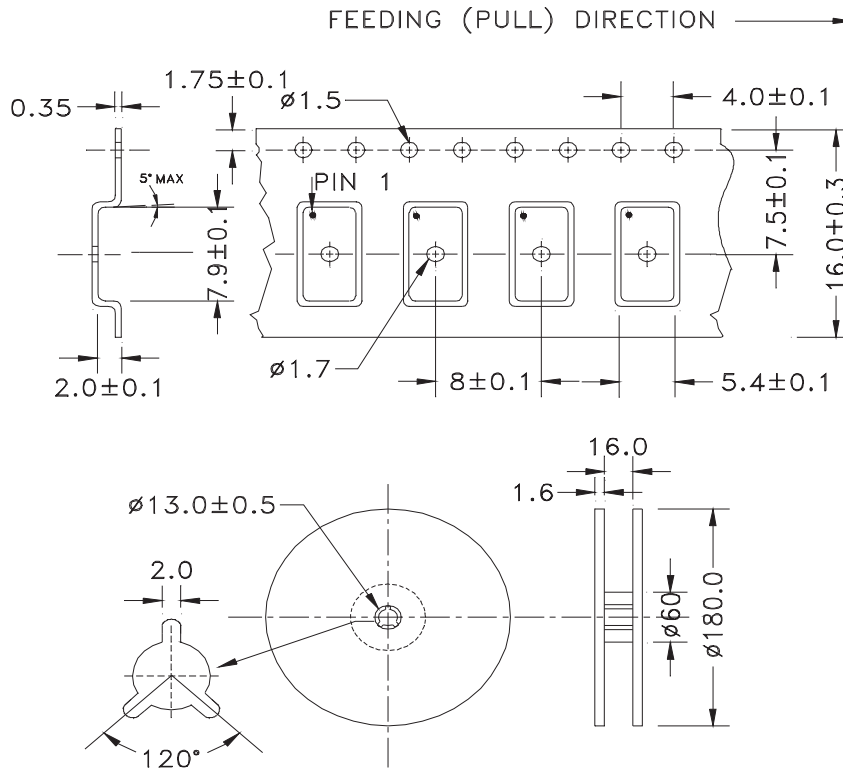


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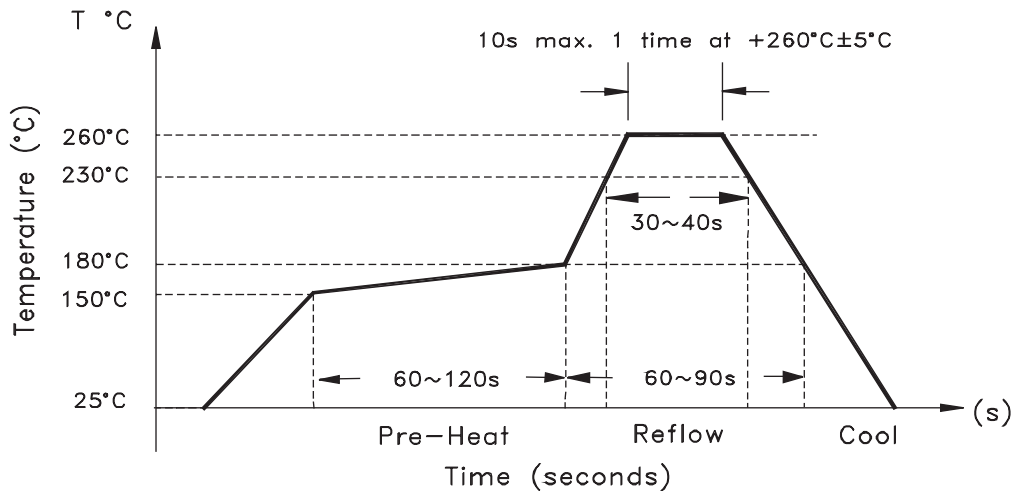


TAPE & REEL: Tape and reel (1,000pcs/reel)



Dimensions: mm

REFLOW PROFILE:



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