

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT7046A** Phase-locked-loop with lock detector

Product specification  
File under Integrated Circuits, IC06

December 1990

## Phase-locked-loop with lock detector

## 74HC/HCT7046A

### FEATURES

- Low power consumption
- Centre frequency up to 17 MHz (typ.) at  $V_{CC} = 4.5\text{ V}$
- Choice of two phase comparators: EXCLUSIVE-OR; edge-triggered JK flip-flop;
- Excellent VCO frequency linearity
- VCO-inhibit control for ON/OFF keying and for low standby power consumption
- Minimal frequency drift
- Operation power supply voltage range:  
VCO section 3.0 to 6.0 V  
digital section 2.0 to 6.0 V
- Zero voltage offset due to op-amp buffering
- Output capability: standard
- $I_{CC}$  category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT7046 are high-speed Si-gate CMOS devices and are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT7046 are phase-locked-loop circuits that comprise a linear voltage-controlled oscillator (VCO) and two different phase comparators (PC1 and PC2) with a common signal input amplifier and a common comparator input.

A lock detector is provided and this gives a HIGH level at pin 1 (LD) when the PLL is locked. The lock detector capacitor must be connected between pin 15 ( $C_{LD}$ ) and pin 8 (GND). The value of the  $C_{LD}$  capacitor can be determined, using information supplied in Fig.32. The input signal can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input

amplifiers. With a passive low-pass filter, the "7046" forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

### VCO

The VCO requires one external capacitor C1 (between  $C1_A$  and  $C1_B$ ) and one external resistor R1 (between  $R_1$  and GND) or two external resistors R1 and R2 (between  $R_1$  and GND, and  $R_2$  and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required.

The high input impedance of the VCO simplifies the design of low-pass filters by giving the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin 10 ( $DEM_{OUT}$ ). In contrast to conventional techniques where the  $DEM_{OUT}$  voltage is one threshold voltage lower than the VCO input voltage, here the  $DEM_{OUT}$  voltage equals that of the VCO input. If  $DEM_{OUT}$  is used, a load resistor ( $R_S$ ) should be connected from  $DEM_{OUT}$  to GND; if unused,  $DEM_{OUT}$  should be left open. The VCO output ( $VCO_{OUT}$ ) can be connected directly to the comparator input ( $COMP_{IN}$ ), or connected via a frequency-divider. The VCO output signal has a duty factor of 50% (maximum expected deviation 1%), if the VCO input is held at a constant DC level. A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

The only difference between the HC and HCT versions is the input level specification of the INH input. This input disables the VCO section. The comparators' sections are identical, so that there is no difference in the

$SIG_{IN}$  (pin 14) or  $COMP_{IN}$  (pin 3) inputs between the HC and HCT versions.

### Phase comparators

The signal input ( $SIG_{IN}$ ) can be directly coupled to the self-biasing amplifier at pin 14, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

#### Phase comparator 1 (PC1)

This is an EXCLUSIVE-OR network. The signal and comparator input frequencies ( $f_i$ ) must have a 50% duty factor to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple ( $f_r = 2f_i$ ) is suppressed, is:

$$V_{DEMOUT} = \frac{V_{CC}}{\pi} (\phi_{SIGIN} - \phi_{COMPIN})$$

where  $V_{DEMOUT}$  is the demodulator output at pin 10;

$V_{DEMOUT} = V_{PC1OUT}$  (via low-pass filter).

The phase comparator gain is:

$$K_p = \frac{V_{CC}}{\pi} (V/r).$$

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 ( $V_{DEMOUT}$ ), is the resultant of the phase differences of signals ( $SIG_{IN}$ ) and the comparator input ( $COMP_{IN}$ ) as shown in Fig.6. The average of  $V_{DEMOUT}$  is equal to  $1/2 V_{CC}$  when there is no signal or noise at  $SIG_{IN}$  and with this input the VCO oscillates at the centre frequency ( $f_0$ ). Typical

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waveforms for the PC1 loop locked at  $f_o$  are shown in Fig.7.

The frequency capture range ( $2f_c$ ) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ( $2f_L$ ) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range. This configuration retains lock even with very noisy input signals. Typical behaviour of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO centre frequency.

### Phase comparator 2 (PC2)

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of  $SIG_{IN}$  and  $COMP_{IN}$  are not important. PC2 comprises two D-type flip-flops, control-gating and a 3-state output stage. The circuit functions as an up-down counter (Fig.5) where  $SIG_{IN}$  causes an up-count and  $COMP_{IN}$  a down-count. The transfer function of PC2, assuming ripple ( $f_r = f_i$ ) is suppressed, is:

$$V_{DEMODOUT} = \frac{V_{CC}}{4\pi} (\phi_{SIGIN} - \phi_{COMPIN})$$

where  $V_{DEMODOUT}$  is the demodulator output at pin 10;

$V_{DEMODOUT} = V_{PC2OUT}$  (via low-pass filter).

The phase comparator gain is:

$$K_p = \frac{V_{CC}}{4\pi} (V/r).$$

$V_{DEMODOUT}$  is the resultant of the initial phase differences of  $SIG_{IN}$  and  $COMP_{IN}$  as shown in Fig.8. Typical waveforms for the PC2 loop locked at  $f_o$  are shown in Fig.9.

When the frequencies of  $SIG_{IN}$  and  $COMP_{IN}$  are equal but the phase of  $SIG_{IN}$  leads that of  $COMP_{IN}$ , the p-type output driver at  $PC2_{OUT}$  is held "ON" for a time corresponding to the phase difference ( $\phi_{DEMODOUT}$ ). When the phase of  $SIG_{IN}$  lags that of  $COMP_{IN}$ , the n-type driver is held "ON".

When the frequency of  $SIG_{IN}$  is higher than that of  $COMP_{IN}$ , the p-type output driver is held "ON" for most of the input signal cycle time, and for the remainder of the cycle both n and p-type drivers are "OFF" (3-state). If the  $SIG_{IN}$  frequency is lower than the  $COMP_{IN}$  frequency, then it is the n-type driver that is held "ON" for most of the cycle. Subsequently, the voltage at the capacitor (C2) of the low-pass filter connected to  $PC2_{OUT}$  varies until the signal and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance.

Thus, for PC2, no phase difference exists between  $SIG_{IN}$  and  $COMP_{IN}$  over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both p and n-type drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of

the low-pass filter. With no signal present at  $SIG_{IN}$  the VCO adjusts, via PC2, to its lowest frequency.

### APPLICATIONS

- FM modulation and demodulation
- Frequency synthesis and multiplication
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control

## Phase-locked-loop with lock detector

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**QUICK REFERENCE DATA**GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$f_o$	VCO centre frequency	$C_1 = 40\text{ pF}$ ; $R_1 = 3\text{ k}\Omega$ ; $V_{CC} = 5\text{ V}$	19	19	MHz
$C_I$	input capacitance (pin 5)		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per package	notes 1 and 2	24	24	pF

**Notes**

1. Applies to the phase comparator section only (VCO disabled).  
For power dissipation of VCO and demodulator sections see Figs 20, 21 and 22.

2.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

**ORDERING INFORMATION**

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	LD	lock detector output (active HIGH)
2	PC1 <sub>OUT</sub>	phase comparator 1 output
3	COMP <sub>IN</sub>	comparator input
4	VCO <sub>OUT</sub>	VCO output
5	INH	inhibit input
6	C1 <sub>A</sub>	capacitor C1 connection A
7	C1 <sub>B</sub>	capacitor C1 connection B
8	GND	ground (0 V)
9	VCO <sub>IN</sub>	VCO input
10	DEM <sub>OUT</sub>	demodulator output
11	R <sub>1</sub>	resistor R1 connection
12	R <sub>2</sub>	resistor R2 connection
13	PC2 <sub>OUT</sub>	phase comparator 2 output
14	SIG <sub>IN</sub>	signal input
15	C <sub>LD</sub>	lock detector capacitor input
16	V <sub>CC</sub>	positive supply voltage

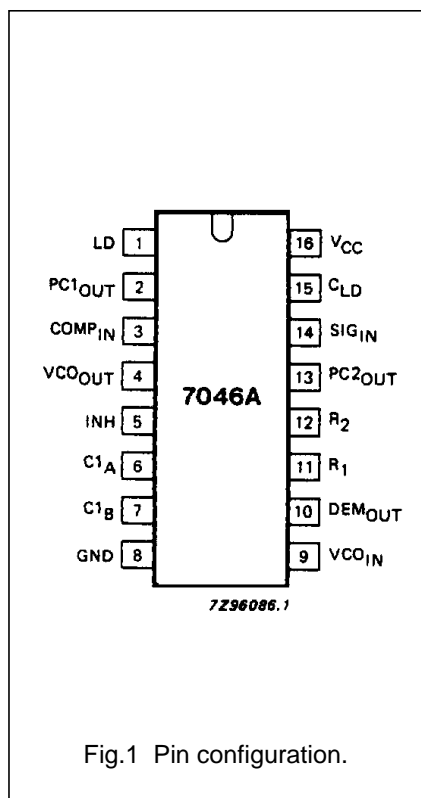


Fig.1 Pin configuration.

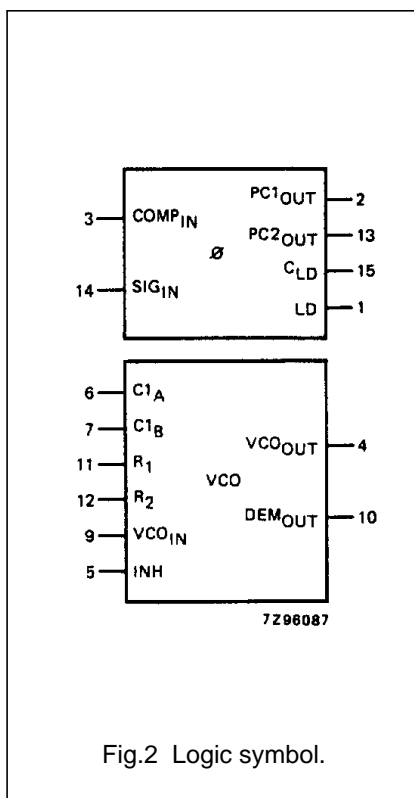


Fig.2 Logic symbol.

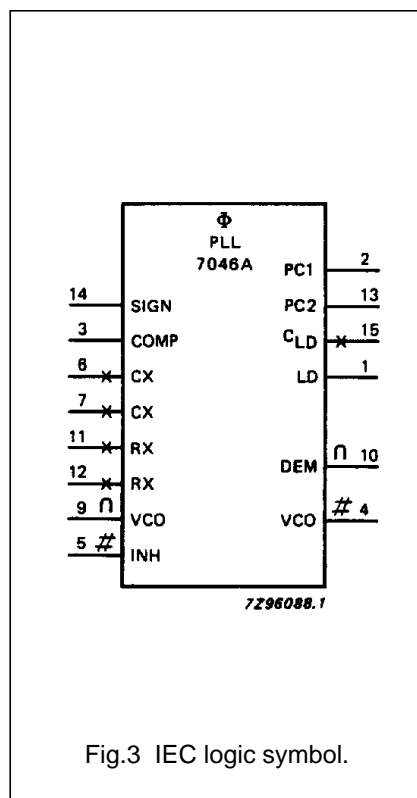


Fig.3 IEC logic symbol.

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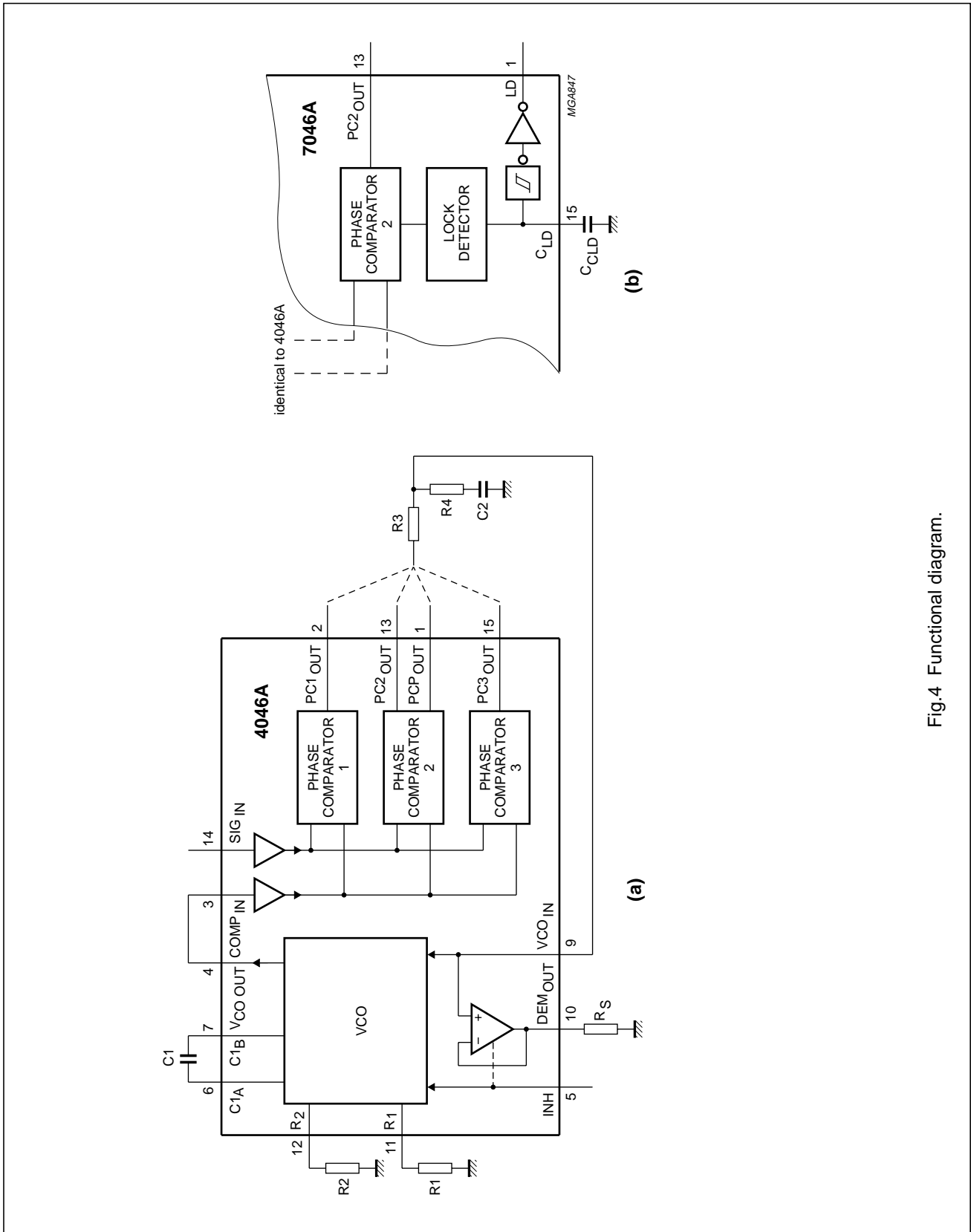


Fig.4 Functional diagram.

Phase-locked-loop with lock detector

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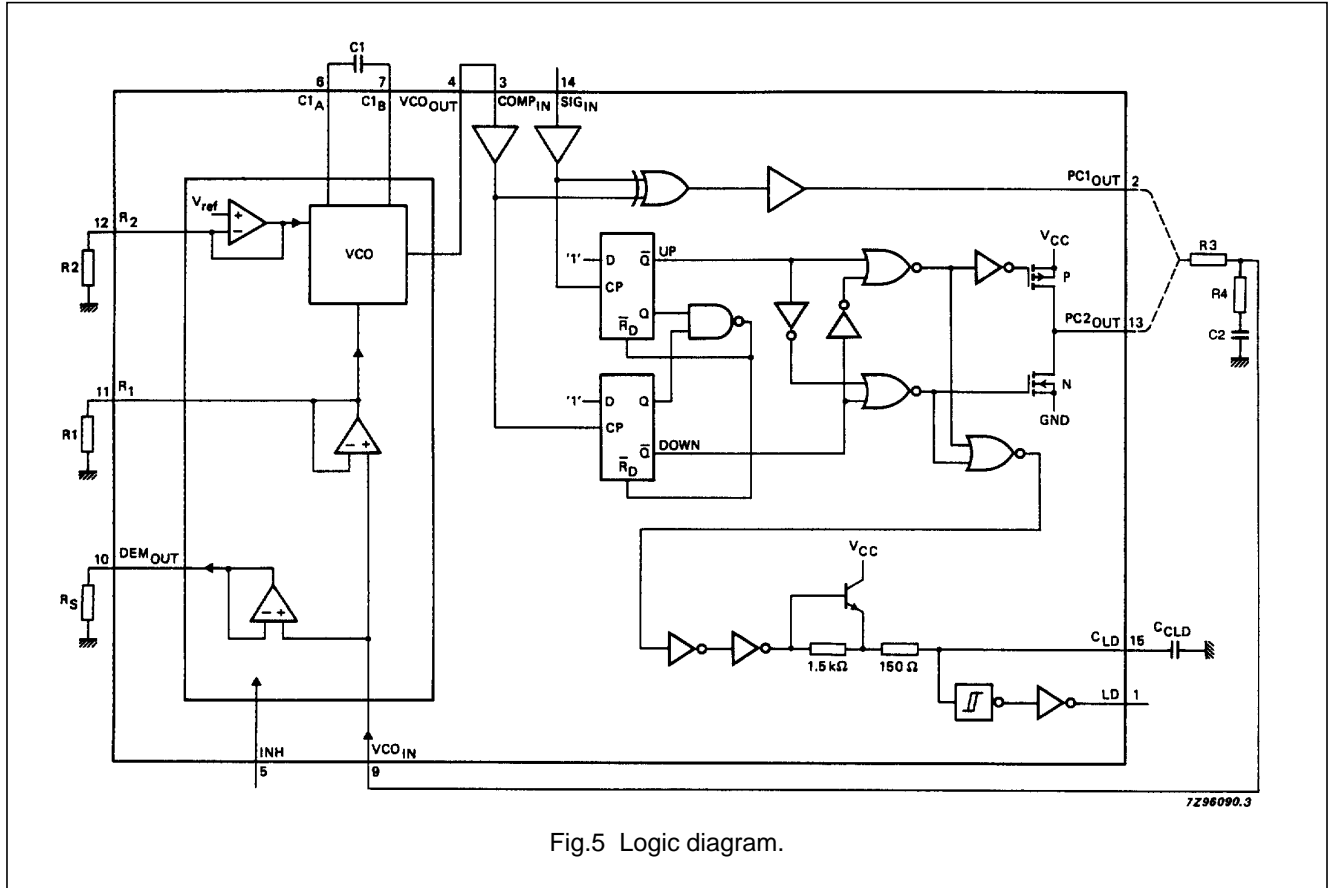
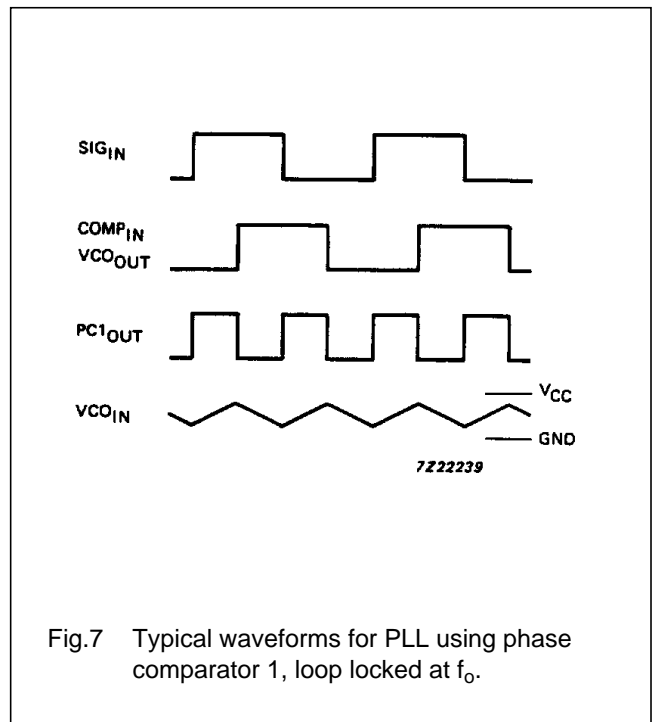
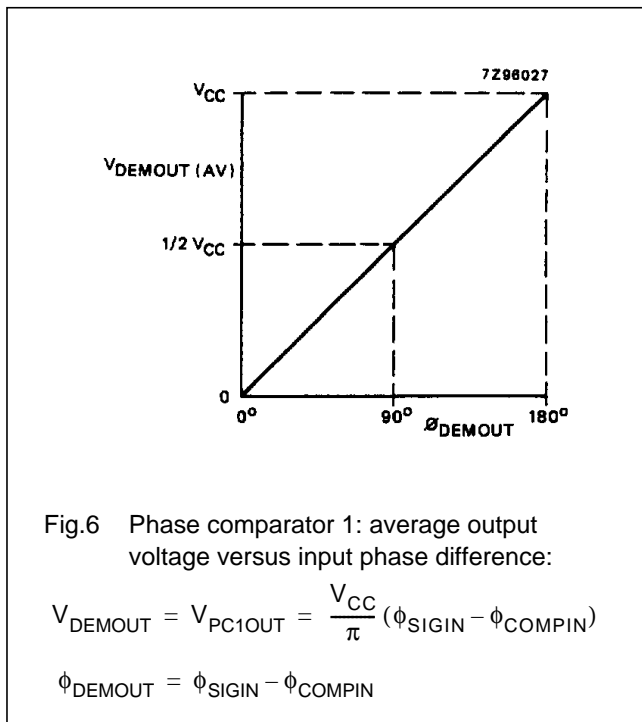


Fig.5 Logic diagram.



Phase-locked-loop with lock detector

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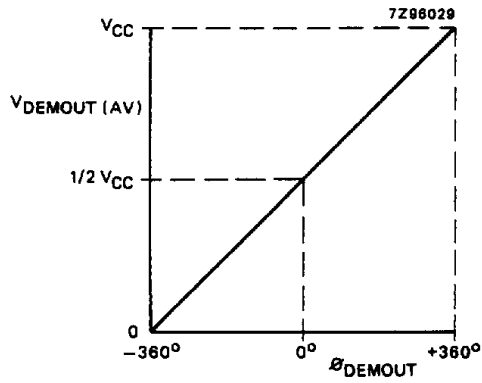


Fig.8 Phase comparator 2: average output voltage versus input phase difference:

$$V_{\text{DEMOUT}} = V_{\text{PC2OUT}} = \frac{V_{\text{CC}}}{4\pi} (\phi_{\text{SIGIN}} - \phi_{\text{COMPIN}})$$

$$\phi_{\text{DEMOUT}} = (\phi_{\text{SIGIN}} - \phi_{\text{COMPIN}}) \cdot$$

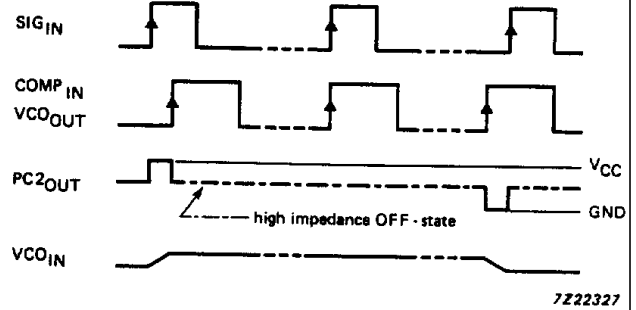


Fig.9 Typical waveforms for PLL using phase comparator 2, loop locked at  $f_0$ .



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## RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
$V_{CC}$	DC supply voltage	3.0	5.0	6.0	4.5	5.0	5.5	V	
$V_{CC}$	DC supply voltage if VCO section is not used	2.0	5.0	6.0	4.5	5.0	5.5	V	
$V_I$	DC input voltage range	0		$V_{CC}$	0		$V_{CC}$	V	
$V_O$	DC output voltage range	0		$V_{CC}$	0		$V_{CC}$	V	
$T_{amb}$	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC CHARACTERISTICS
$T_{amb}$	operating ambient temperature range	-40		+125	-40		+125	°C	
$t_r, t_f$	input rise and fall times (pin 5)		6.0	1000 500 400		6.0	500	ns	$V_{CC} = 2.0\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 6.0\text{ V}$

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
$V_{CC}$	DC supply voltage	-0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$
$\pm I_{CC};$ $\pm I_{GND}$	DC $V_{CC}$ or GND current		50	mA	
$T_{stg}$	storage temperature range	-65	+150	°C	
$P_{tot}$	power dissipation per package				for temperature range: -40 to +125 °C
	plastic DIL		750	mW	74HC/HCT above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K

## Phase-locked-loop with lock detector

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## DC CHARACTERISTICS FOR 74HC

## Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS		
		74HC								V <sub>CC</sub> (V)	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
I <sub>CC</sub>	quiescent supply current (VCO disabled)			8.0		80.0		160.0	μA	6.0	pins 3, 5, and 14 at V <sub>CC</sub> ; pin 9 at GND; I <sub>I</sub> at pins 3 and 14 to be excluded	

## Phase-locked-loop with lock detector

## 74HC/HCT7046A

**Phase comparator section**

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HC							V <sub>CC</sub> (V)	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.		max.			
V <sub>IH</sub>	DC coupled HIGH level input voltage SIG <sub>IN</sub> , COMP <sub>IN</sub>	1.5 3.15 4.2	1.2 2.4 3.2		1.5 3.15 4.2		1.5 3.15 4.2	V	2.0 4.5 6.0			
V <sub>IL</sub>	DC coupled LOW level input voltage SIG <sub>IN</sub> , COMP <sub>IN</sub>		0.8 2.1 2.8	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V <sub>OH</sub>	HIGH level output voltage LD, PC <sub>nOUT</sub>	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9	V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 µA -I <sub>O</sub> = 20 µA -I <sub>O</sub> = 20 µA	
V <sub>OH</sub>	HIGH level output voltage LD, PC <sub>nOUT</sub>	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 4.0 mA -I <sub>O</sub> = 5.2 mA	
V <sub>OL</sub>	LOW level output voltage LD, PC <sub>nOUT</sub>		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 µA I <sub>O</sub> = 20 µA I <sub>O</sub> = 20 µA
V <sub>OL</sub>	LOW level output voltage LD, PC <sub>nOUT</sub>		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA I <sub>O</sub> = 5.2 mA
±I <sub>I</sub>	input leakage current SIG <sub>IN</sub> , COMP <sub>IN</sub>			3.0 7.0 18.0 30.0		4.0 9.0 23.0 38.0		5.0 11.0 27.0 45.0	µA	2.0 3.0 4.5 6.0	V <sub>CC</sub> or GND	
±I <sub>OZ</sub>	3-state OFF-state current PC2 <sub>OUT</sub>			0.5		5.0		10.0	µA	6.0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND
R <sub>I</sub>	input resistance SIG <sub>IN</sub> , COMP <sub>IN</sub>		800 250 150						kΩ	3.0 4.5 6.0	V <sub>I</sub> at self-bias operating point; ΔV <sub>I</sub> = 0.5 V; see Figs 10, 11 and 12	

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**VCO section**

Voltages are referenced to GND (ground = 0 V)

SYM-BOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS		
		74HC								V <sub>CC</sub> (V)	V <sub>I</sub>	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V <sub>IH</sub>	HIGH level input voltage INH	2.1 3.15 4.2	1.7 2.4 3.2		2.1 3.15 4.2		2.1 3.15 4.2		V	3.0 4.5 6.0		
V <sub>IL</sub>	LOW level input voltage INH		1.3 2.1 2.8	0.9 1.35 1.8		0.9 1.35 1.8		0.9 1.35 1.8	V	3.0 4.5 6.0		
V <sub>OH</sub>	HIGH level output voltage VCO <sub>OUT</sub>	2.9 4.4 5.9	3.0 4.5 6.0		2.9 4.4 5.9		2.9 4.4 5.9		V	3.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA
V <sub>OH</sub>	HIGH level output voltage VCO <sub>OUT</sub>	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 4.0 mA -I <sub>O</sub> = 5.2 mA
V <sub>OL</sub>	LOW level output voltage VCO <sub>OUT</sub>		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	3.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA
V <sub>OL</sub>	LOW level output voltage VCO <sub>OUT</sub>		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA I <sub>O</sub> = 5.2 mA
V <sub>OL</sub>	LOW level output voltage C1 <sub>A</sub> , C1 <sub>B</sub> (test purposes only)			0.40 0.40		0.47 0.47		0.54 0.54	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA I <sub>O</sub> = 5.2 mA
±I <sub>I</sub>	input leakage current INH, VCO <sub>IN</sub>			0.1		1.0		1.0	μA	6.0	V <sub>CC</sub> or GND	
R1	resistor range	3.0 3.0 3.0		300 300 300					kΩ	3.0 4.5 6.0		note 1
R2	resistor range	3.0 3.0 3.0		300 300 300					kΩ	3.0 4.5 6.0		note 1
C1	capacitor range	40 40 40		no limit					pF	3.0 4.5 6.0		
V <sub>VCOIN</sub>	operating voltage range at VCO <sub>IN</sub>	1.1 1.1 1.1		1.9 3.4 4.9					V	3.0 4.5 6.0		over the range specified for R1; for linearity see Figs 18 and 19.

**Note**

- The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/or R2 are/is > 10 kΩ.

## Phase-locked-loop with lock detector

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**Demodulator section**

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> (V)	OTHER
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
R <sub>S</sub>	resistor range	50 50 50		300 300 300					kΩ	3.0 4.5 6.0	at R <sub>S</sub> > 300 kΩ the leakage current can influence V <sub>DEMOUT</sub>
V <sub>OFF</sub>	offset voltage V <sub>COIN</sub> to V <sub>DEMOUT</sub>		±30 ±20 ±10						mV	3.0 4.5 6.0	V <sub>I</sub> = V <sub>VCOIN</sub> = 1/2 V <sub>CC</sub> ; values taken over R <sub>S</sub> range; see Fig.13
R <sub>D</sub>	dynamic output resistance at DEM <sub>OUT</sub>		25 25 25						Ω	3.0 4.5 6.0	V <sub>DEMOUT</sub> = 1/2 V <sub>CC</sub>

## Phase-locked-loop with lock detector

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## AC CHARACTERISTICS FOR 74HC

## Phase comparator section

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ (V)	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC1 <sub>OUT</sub>		58 21 17	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig.14
$t_{PZH}/t_{PZL}$	3-state output enable time SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC2 <sub>OUT</sub>		74 27 22	280 56 48		350 70 60		420 84 71	ns	2.0 4.5 6.0	Fig.15
$t_{PHZ}/t_{PLZ}$	3-state output disable time SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC2 <sub>OUT</sub>		96 35 28	325 65 55		405 81 69		490 98 83	ns	2.0 4.5 6.0	Fig.15
$t_{THL}/t_{TLH}$	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.14
$V_{I(p-p)}$	AC coupled input sensitivity (peak-to-peak value) at SIG <sub>IN</sub> or COMP <sub>IN</sub>		9 11 15 33						mV	2.0 3.0 4.5 6.0	$f_i = 1$ MHz

## VCO section

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYM- BOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ (V)	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	typ.	max.	min.				max.
$\Delta f/T$	frequency stability with temperature change				0.20 0.15 0.14				%/K	3.0 4.5 6.0	$V_I = V_{VCOIN} = 1/2 V_{CC}$ ; R1 = 100 k $\Omega$ ; R2 = $\infty$ ; C1 = 100 pF; see Fig.16
$f_o$	VCO centre frequency (duty factor = 50%)	7.0 11.0 13.0	10.0 17.0 21.0						MHz	3.0 4.5 6.0	$V_{VCOIN} = 1/2 V_{CC}$ ; R1 = 3 k $\Omega$ ; R2 = $\infty$ ; C1 = 40 pF; see Fig.17
$\Delta f_{VCO}$	VCO frequency linearity		1.0 0.4 0.3						%	3.0 4.5 6.0	R1 = 100 k $\Omega$ ; R2 = $\infty$ ; C1 = 100 pF; see Figs 18 and 19
$\delta_{VCO}$	duty factor at VCO <sub>OUT</sub>		50 50 50						%	3.0 4.5 6.0	

## Phase-locked-loop with lock detector

## 74HC/HCT7046A

## DC CHARACTERISTICS FOR 74HCT

## Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> (V)	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
I <sub>CC</sub>	quiescent supply current (VCO disabled)			8.0		80.0		160.0	μA	6.0	pins 3, 5 and 14 at V <sub>CC</sub> ; pin 9 at GND; I <sub>I</sub> at pins 3 and 14 to be excluded
ΔI <sub>CC</sub>	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1) V <sub>I</sub> = V <sub>CC</sub> - 2.1 V		100	360		450		490	μA	4.5 to 5.5	pins 3 and 14 at V <sub>CC</sub> ; pin 9 at GND; I <sub>I</sub> at pins 3 and 14 to be excluded

## Note

- The value of additional quiescent supply current (ΔI<sub>CC</sub>) for a unit load of 1 is given above. To determine ΔI<sub>CC</sub> per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
INH	1.00

## Phase-locked-loop with lock detector

## 74HC/HCT7046A

**Phase comparator section**

Voltages are referenced to GND (ground = 0 V)

SYM BOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS		
		74HCT								V <sub>CC</sub> (V)	V <sub>I</sub>	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V <sub>IH</sub>	DC coupled HIGH level input voltage SIG <sub>IN</sub> , COMP <sub>IN</sub>	3.15	2.4						V	4.5		
V <sub>IL</sub>	DC coupled LOW level input voltage SIG <sub>IN</sub> , COMP <sub>IN</sub>		2.1	1.35					V	4.5		
V <sub>OH</sub>	HIGH level output voltage LD, PC <sub>nOUT</sub>	4.4	4.5		4.4		4.4		V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA
V <sub>OH</sub>	HIGH level output voltage LD, PC <sub>nOUT</sub>	3.98	4.32		3.84		3.7		V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 4.0 mA
V <sub>OL</sub>	LOW level output voltage LD, PC <sub>nOUT</sub>		0	0.1		0.1		0.1	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA
V <sub>OL</sub>	LOW level output voltage LD, PC <sub>nOUT</sub>		0.15	0.26		0.33		0.4	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA
±I <sub>I</sub>	input leakage current SIG <sub>IN</sub> , COMP <sub>IN</sub>			30		38		45	μA	5.5	V <sub>CC</sub> or GND	
±I <sub>OZ</sub>	3-state OFF-state current PC <sub>2OUT</sub>			0.5		5.0		10.0	μA	5.5	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND
R <sub>I</sub>	input resistance SIG <sub>IN</sub> , COMP <sub>IN</sub>		250						kΩ	4.5	V <sub>I</sub> at self-bias operating point; ΔV <sub>I</sub> = 0.5 V; see Figs 10, 11 and 12	



## Phase-locked-loop with lock detector

## 74HC/HCT7046A

## DC CHARACTERISTICS FOR 74HCT

## VCO section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS		
		74HCT								V <sub>CC</sub> (V)	V <sub>I</sub>	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V <sub>IH</sub>	HIGH level input voltage INH	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V <sub>IL</sub>	LOW level input voltage INH		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
V <sub>OH</sub>	HIGH level output voltage VCO <sub>OUT</sub>	4.4	4.5		4.4		4.4		V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 µA
V <sub>OH</sub>	HIGH level output voltage VCO <sub>OUT</sub>	3.98	4.32		3.84		3.7		V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 4.0 mA
V <sub>OL</sub>	LOW level output voltage VCO <sub>OUT</sub>		0	0.1		0.1		0.1	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 µA
V <sub>OL</sub>	LOW level output voltage VCO <sub>OUT</sub>		0.15	0.26		0.33		0.4	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA
V <sub>OL</sub>	LOW level output voltage C1 <sub>A</sub> , C1 <sub>B</sub> (test purposes only)			0.40		0.47		0.54	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA
±I <sub>I</sub>	input leakage current INH, VCO <sub>IN</sub>			0.1		1.0		1.0	µA	5.5	V <sub>CC</sub> or GND	
R1	resistor range	3.0		300					kΩ	4.5		note 1
R2	resistor range	3.0		300					kΩ	4.5		note 1
C1	capacitor range	40		no limit					pF	4.5		
V <sub>VCOIN</sub>	operating voltage range at VCO <sub>IN</sub>	1.1		3.4					V	4.5		over the range specified for R1; for linearity see Figs 18 and 19.

## Note

1. The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/or R2 are/is > 10 kΩ.

## Phase-locked-loop with lock detector

## 74HC/HCT7046A

**Demodulator section**

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HCT									V <sub>CC</sub> (V)	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
R <sub>S</sub>	resistor range	50		300					kΩ	4.5	at R <sub>S</sub> > 300 kΩ the leakage current can influence V <sub>DEMOUT</sub>	
V <sub>OFF</sub>	offset voltage VCO <sub>IN</sub> to V <sub>DEMOUT</sub>		±20						mV	4.5	V <sub>I</sub> = V <sub>VCOIN</sub> = 1/2 V <sub>CC</sub> ; values taken over R <sub>S</sub> range; see Fig.13	
R <sub>D</sub>	dynamic output resistance at DEM <sub>OUT</sub>		25						Ω	4.5	V <sub>DEMOUT</sub> = 1/2 V <sub>CC</sub>	

**AC CHARACTERISTICS FOR 74HCT****Phase comparator section**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HCT									V <sub>CC</sub> (V)	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC1 <sub>OUT</sub>		21	40		50		60	ns	4.5	Fig.14	
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC2 <sub>OUT</sub>		27	56		70		84	ns	4.5	Fig.15	
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC2 <sub>OUT</sub>		35	65		81		98	ns	4.5	Fig.15	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig.14	
V <sub>I(p-p)</sub>	AC coupled input sensitivity (peak-to-peak value) at SIG <sub>IN</sub> or COMP <sub>IN</sub>		15						mV	4.5	f <sub>i</sub> = 1 MHz	

## Phase-locked-loop with lock detector

## 74HC/HCT7046A

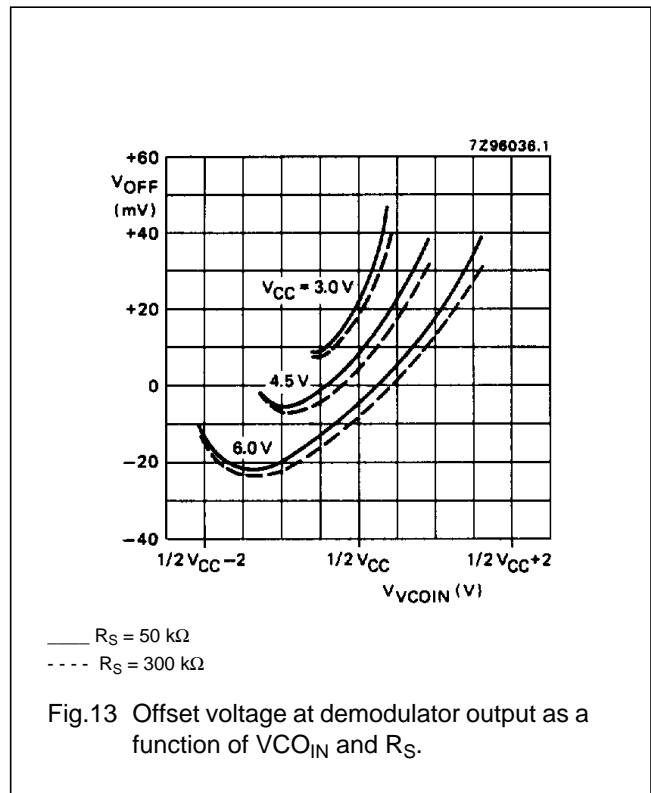
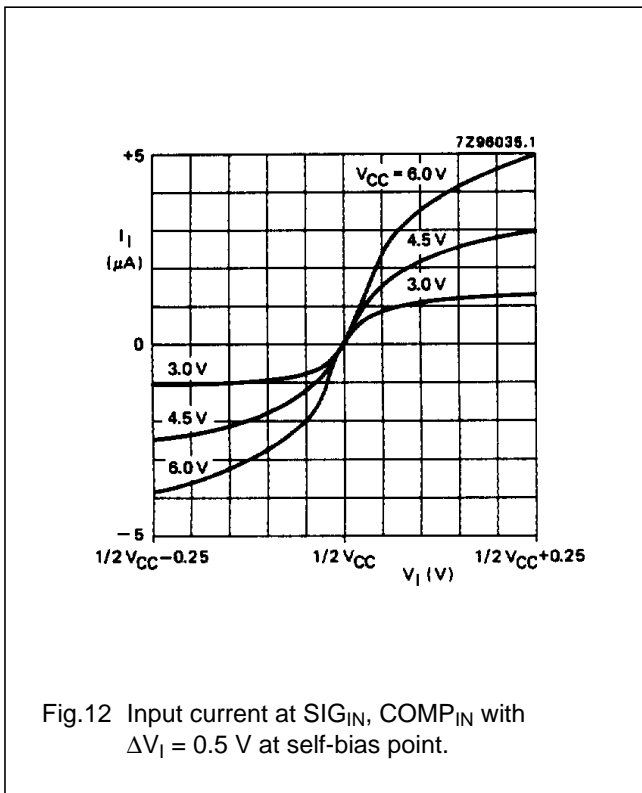
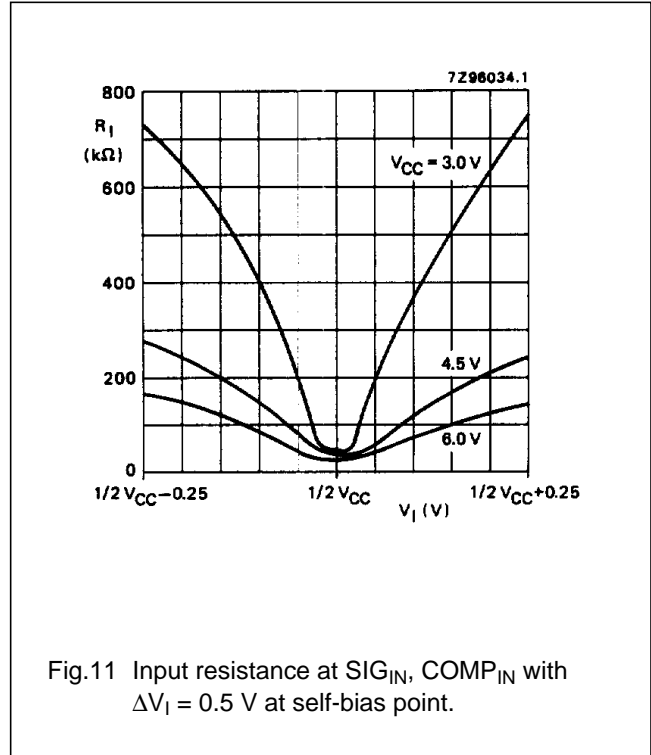
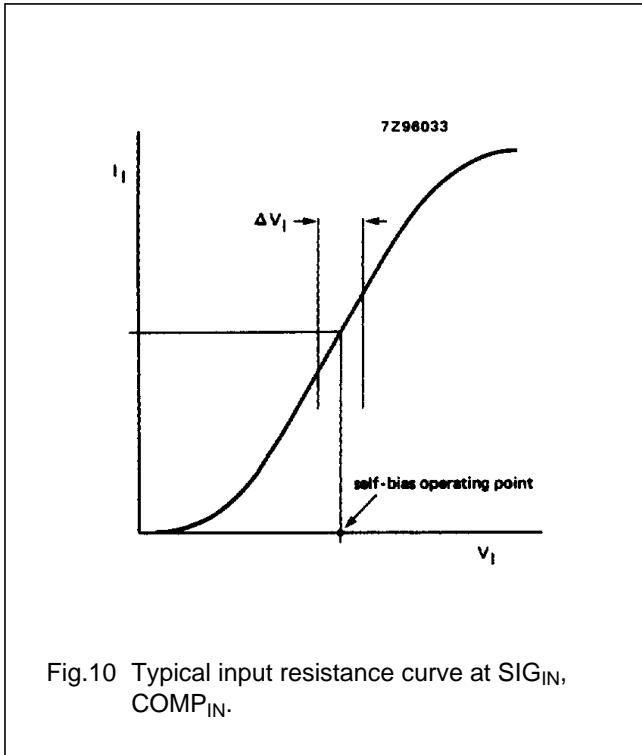
**VCO section**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)								UNIT	TEST CONDITIONS	
		74HCT									$V_{CC}$ (V)	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	typ.	max.	min.	max.				
$\Delta f/T$	frequency stability with temperature change				0.15					%/K	4.5	$V_I = V_{COIN}$ within recommended range; R1 = 100 k $\Omega$ ; R2 = $\infty$ ; C1 = 100 pF; see Fig.16b
$f_o$	VCO centre frequency (duty factor = 50%)	11.0	17.0							MHz	4.5	$V_{VCOIN} = 1/2 V_{CC}$ ; R1 = 3 k $\Omega$ ; R2 = $\infty$ ; C1 = 40 pF; see Fig.17
$\Delta f_{VCO}$	VCO frequency linearity		0.4							%	4.5	R1 = 100 k $\Omega$ ; R2 = $\infty$ ; C1 = 100 pF; see Figs 18 and 19
$\delta_{VCO}$	duty factor at VCO <sub>OUT</sub>		50							%	4.5	

Phase-locked-loop with lock detector

74HC/HCT7046A

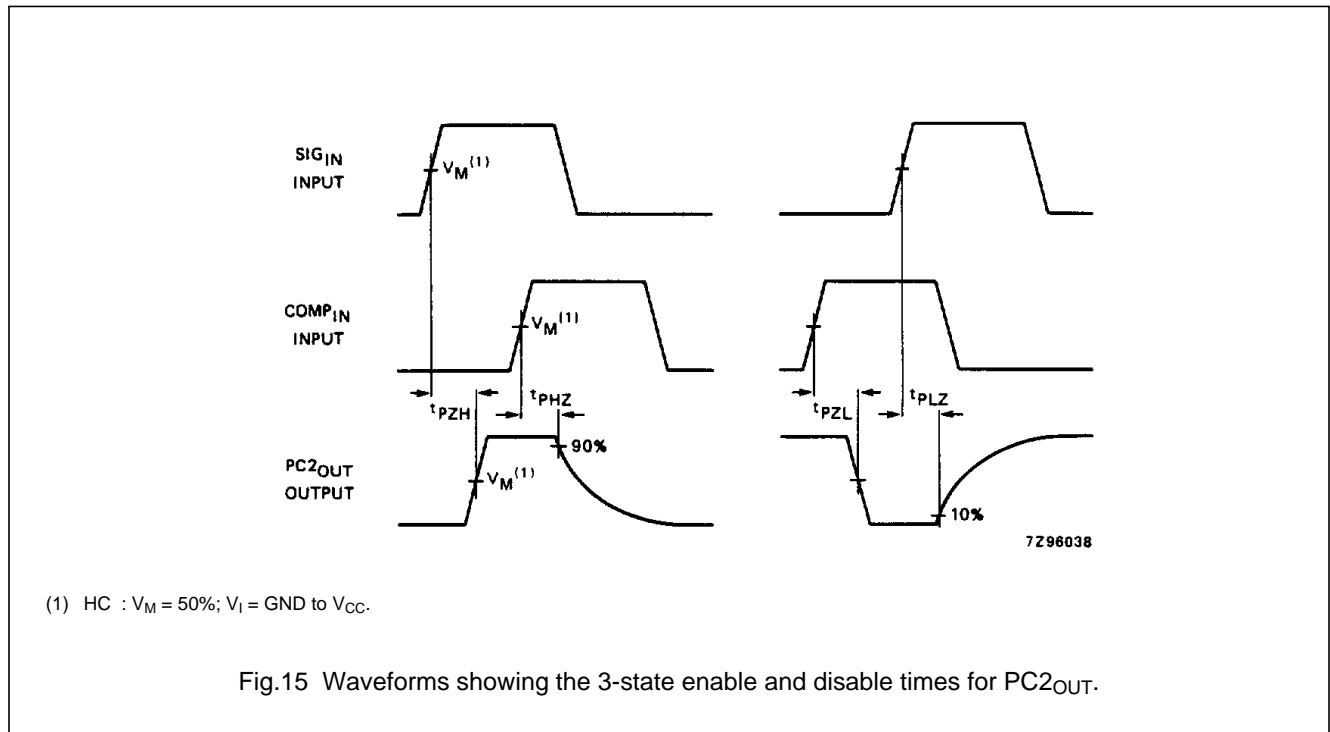
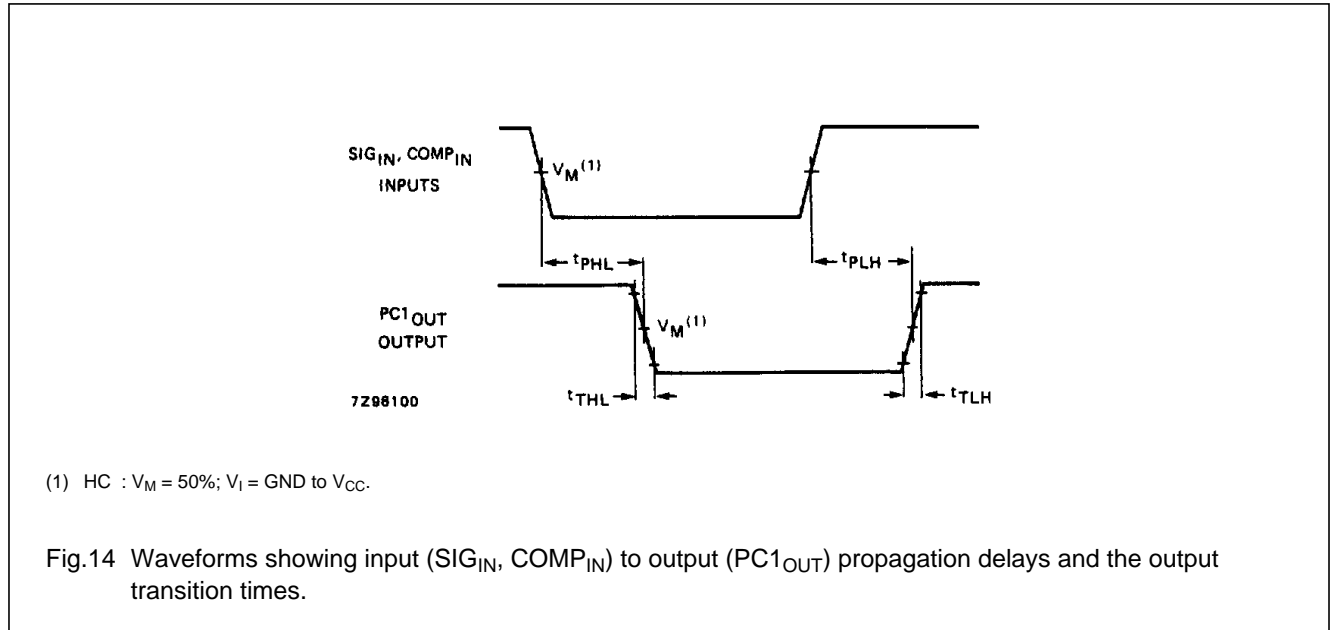
FIGURE REFERENCES FOR DC CHARACTERISTICS



Phase-locked-loop with lock detector

74HC/HCT7046A

AC WAVEFORMS



Phase-locked-loop with lock detector

74HC/HCT7046A

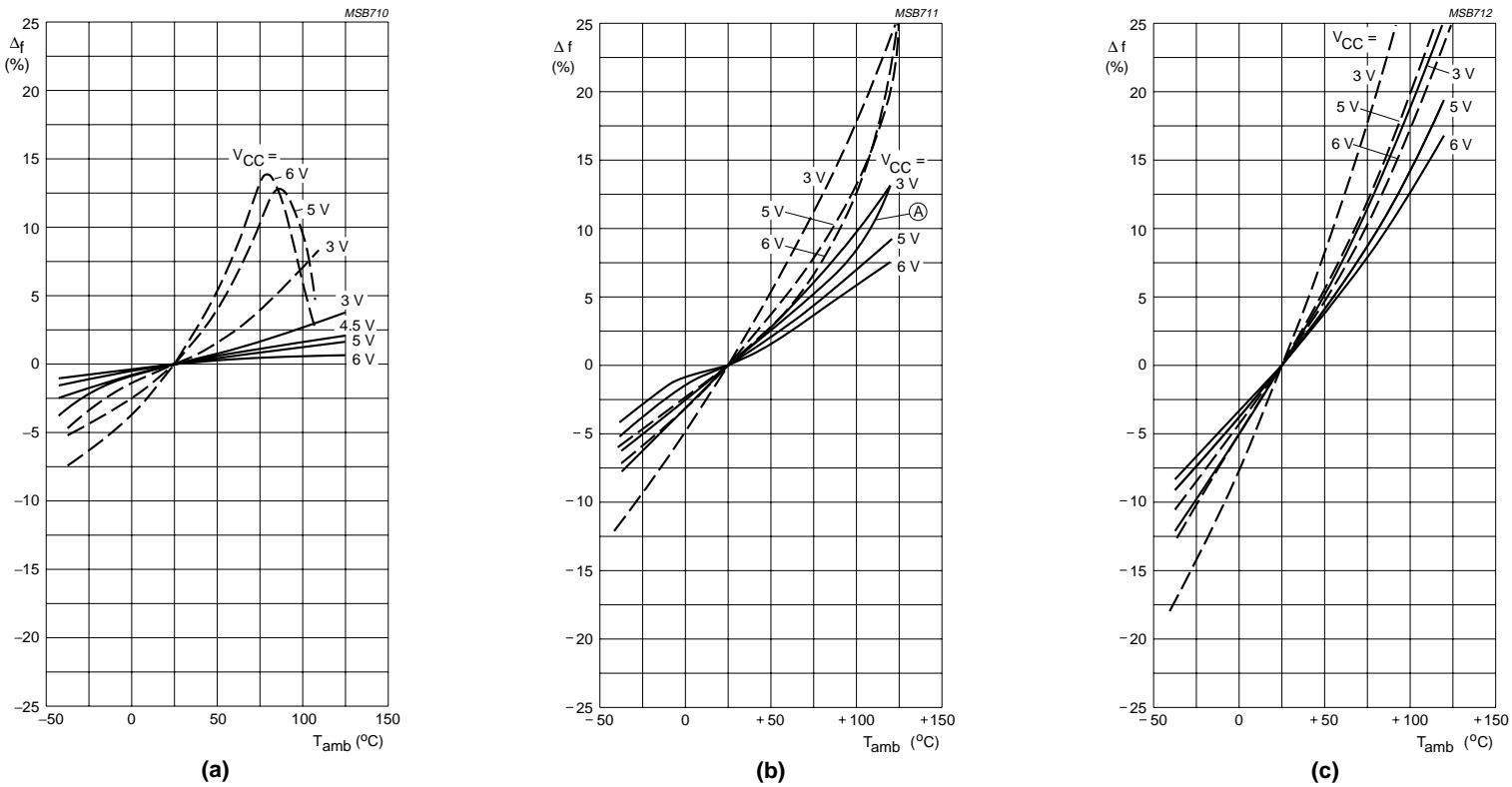


Fig.16 Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter.

— without offset ( $R_2 = \infty$ ): (a)  $R_1 = 3 \text{ k}\Omega$ ; (b)  $R_1 = 10 \text{ k}\Omega$ ; (c)  $R_1 = 300 \text{ k}\Omega$ .

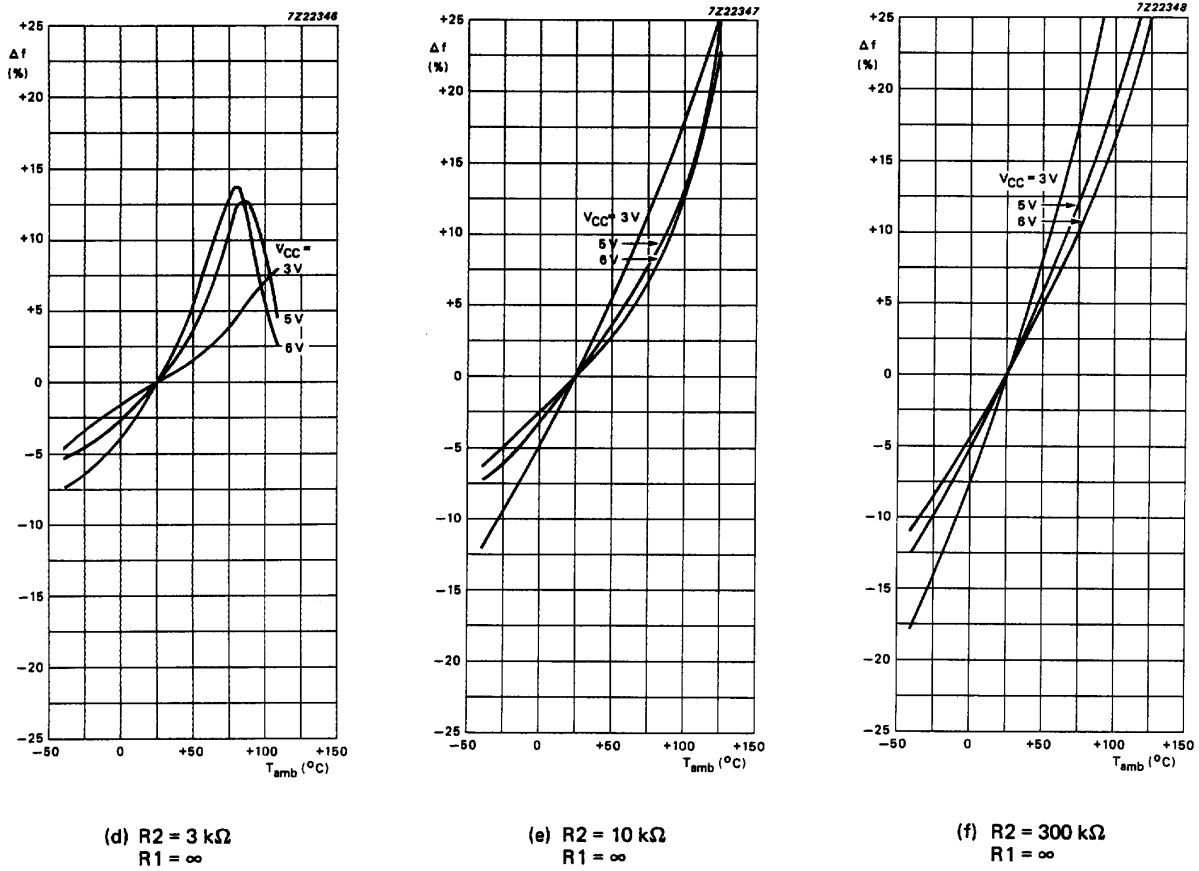
- - - with offset ( $R_1 = \infty$ ): (a)  $R_2 = 3 \text{ k}\Omega$ ; (b)  $R_2 = 10 \text{ k}\Omega$ ; (c)  $R_2 = 300 \text{ k}\Omega$ .

In (b), the frequency stability for  $R_1 = R_2 = 10 \text{ k}\Omega$  at 5 V is also given (curve A). This curve is set by the total VCO bias current, and is not simply the addition of the two  $10 \text{ k}\Omega$  stability curves.  $C_1 = 100 \text{ pF}$ ;  $V_{\text{VCO IN}} = 0.5 V_{\text{CC}}$ .

Phase-locked-loop with lock detector

74HC/HCT7046A

AC WAVEFORMS

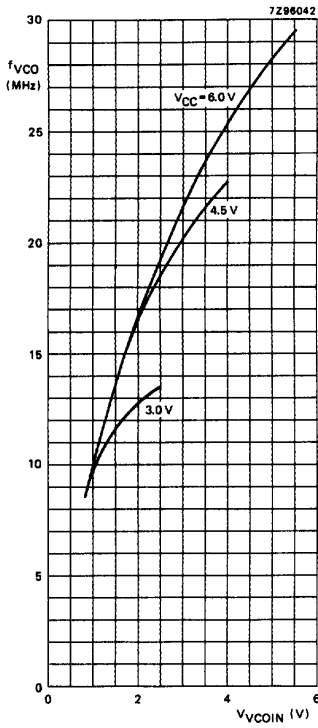


To obtain optimum temperature stability,  $C_1$  must be as small as possible, but larger than 100 pF.

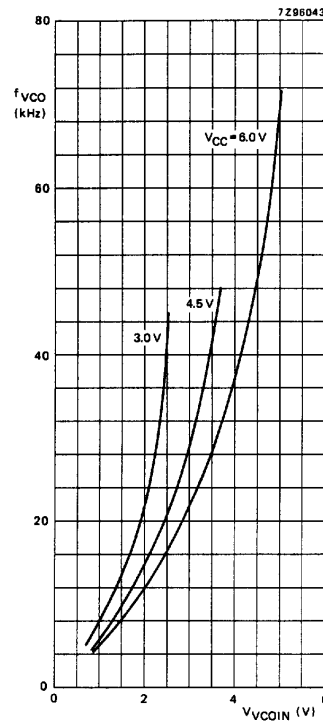
Fig.16 Continued.

Phase-locked-loop with lock detector

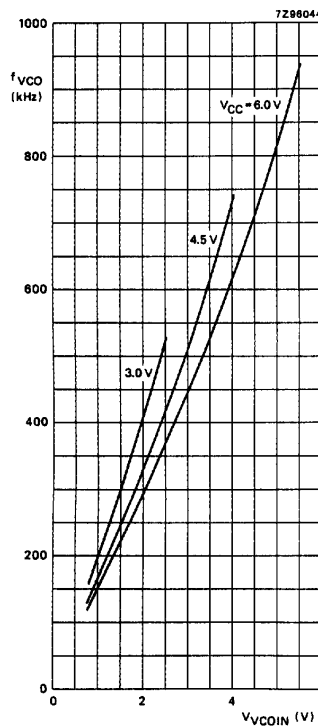
74HC/HCT7046A



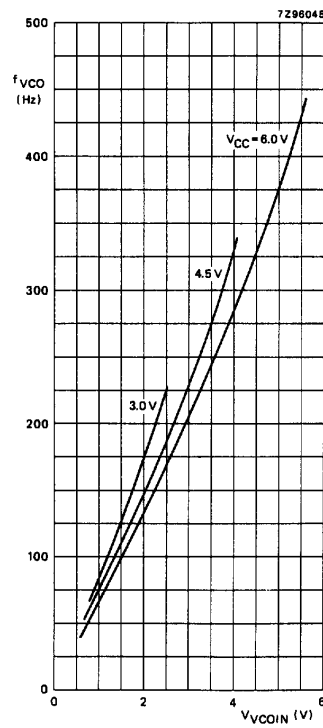
(a)  $R1 = 3\text{ k}\Omega$ ;  
 $C1 = 40\text{ pF}$



(b)  $R1 = 3\text{ k}\Omega$ ;  
 $C1 = 100\text{ nF}$



(c)  $R1 = 300\text{ k}\Omega$ ;  
 $C1 = 40\text{ pF}$



(d)  $R1 = 300\text{ k}\Omega$ ;  
 $C1 = 100\text{ nF}$

Fig.17 Graphs showing VCO frequency ( $f_{VCO}$ ) as a function of the VCO input voltage ( $V_{VCOIN}$ ).



Phase-locked-loop with lock detector

74HC/HCT7046A

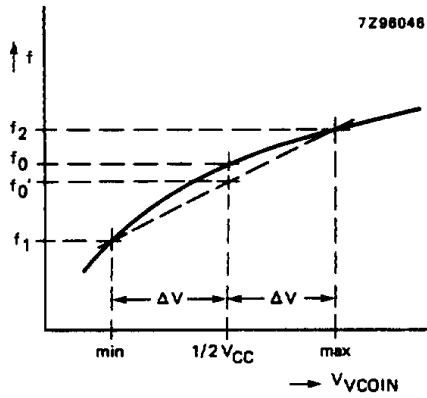


Fig.18 Definition of VCO frequency linearity:  
 $\Delta V = 0.5 \text{ V}$  over the  $V_{CC}$  range:  
 for VCO linearity

$$f'_0 = \frac{f_1 + f_2}{2}$$

$$\text{linearity} = \frac{f'_0 - f_0}{f'_0} \times 100\%$$

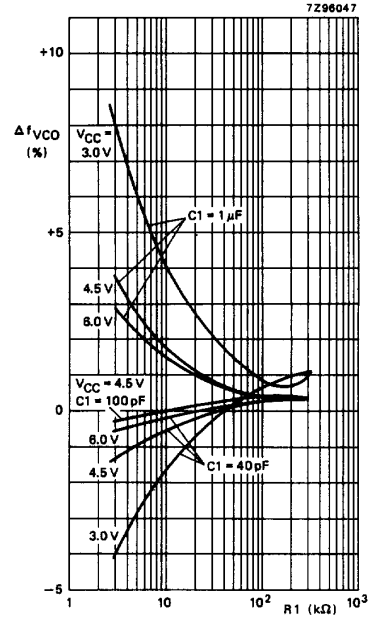
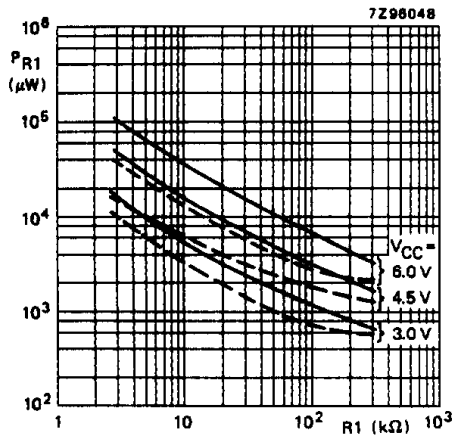


Fig.19 Frequency linearity as a function of  $R_1$ ,  $C_1$  and  $V_{CC}$ :  $R_2 = \infty$  and  $\Delta V = 0.5 \text{ V}$ .

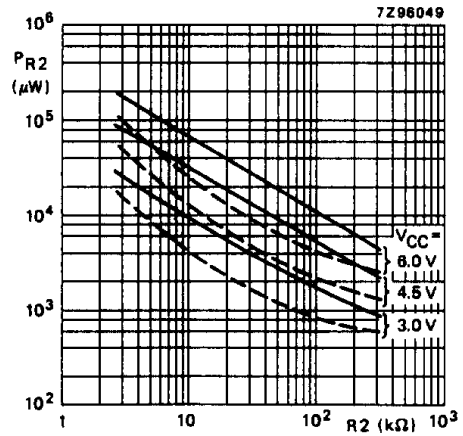
Phase-locked-loop with lock detector

74HC/HCT7046A



—  $C1 = 40\text{ pF}$   
 - - -  $C1 = 1\ \mu F$

Fig.20 Power dissipation versus the value of  $R1$ :  
 $C_L = 50\text{ pF}$ ;  $R2 = \infty$ ;  $V_{VCOIN} = 1/2 V_{CC}$ ;  
 $T_{amb} = 25\text{ }^\circ C$ .



—  $C1 = 40\text{ pF}$   
 - - -  $C1 = 1\ \mu F$

Fig.21 Power dissipation versus the value of  $R2$ :  
 $C_L = 50\text{ pF}$ ;  $R1 = \infty$ ;  $V_{VCOIN} = GND = 0\text{ V}$ ;  
 $T_{amb} = 25\text{ }^\circ C$ .

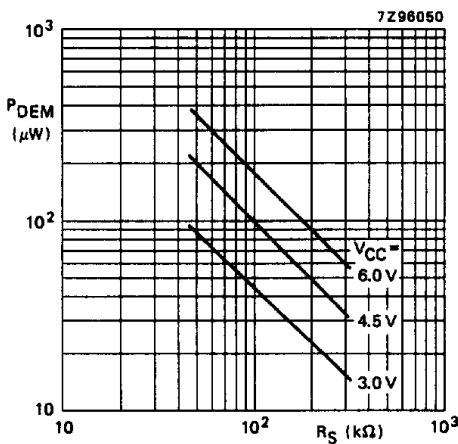


Fig.22 Typical dc power dissipation of demodulator section as a function of  $R_S$ :  $R1 = R2 = \infty$ ;  
 $T_{amb} = 25\text{ }^\circ C$ ;  $V_{VCOIN} = 1/2 V_{CC}$ .

Phase-locked-loop with lock detector

74HC/HCT7046A

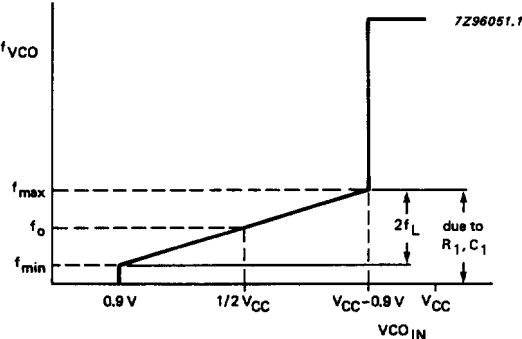
**APPLICATION INFORMATION**

This information is a guide for the approximation of values of external components to be used with the 74HC/HCT7046 in a phase-lock-loop system.

References should be made to Figs 27, 28 and 29 as indicated in the table.

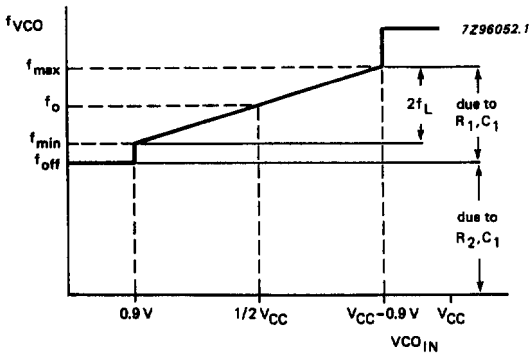
Values of the selected components should be within the following ranges:

- R1 between 3 kΩ and 300 kΩ;
- R2 between 3 kΩ and 300 kΩ;
- R1 + R2 parallel value > 2.7 kΩ;
- C1 greater than 40 pF.

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
VCO frequency <b>without extra offset</b>	PC1, PC2	<p><b>VCO frequency characteristic</b></p> <p>With <math>R2 = \infty</math> and <math>R1</math> within the range <math>3\text{ k}\Omega &lt; R1 &lt; 300\text{ k}\Omega</math>, the characteristics of the VCO operation will be as shown in Fig. 23. (Due to <math>R1, C1</math> time constant a small offset remains when <math>R2 = \infty</math>.)</p>  <p>Fig. 23 Frequency characteristic of VCO operating without offset: <math>f_o</math> = centre frequency; <math>2f_L</math> = frequency lock range.</p>
	PC1	<p><b>Selection of R1 and C1</b></p> <p>Given <math>f_o</math>, determine the values of <math>R1</math> and <math>C1</math> using Fig.27.</p>
	PC2	<p>Given <math>f_{max}</math> and <math>f_o</math>, determine the values of <math>R1</math> and <math>C1</math> using Fig.27, use Fig.29 to obtain <math>2f_L</math> and then use this to calculate <math>f_{min}</math>.</p>

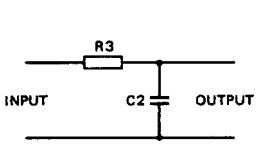
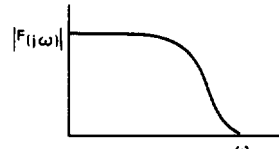
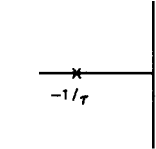
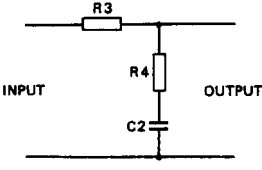
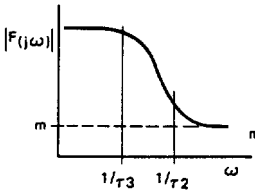
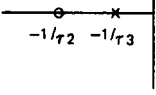
Phase-locked-loop with lock detector

74HC/HCT7046A

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
<p>VCO frequency with extra offset</p>	<p>PC1, PC2</p>	<p><b>VCO frequency characteristic</b></p> <p>With R1 and R2 within the ranges <math>3\text{ k}\Omega &lt; R1 &lt; 300\text{ k}\Omega</math>, <math>3\text{ k}\Omega &lt; R2 &lt; 300\text{ k}\Omega</math>, the characteristics of the VCO operation will be as shown in Fig. 24.</p>  <p>Fig. 24 Frequency characteristic of VCO operating with offset:  <math>f_0</math> = centre frequency; <math>2f_L</math> = frequency lock range.</p>
	<p>PC1, PC2</p>	<p><b>Selection of R1, R2 and C1</b></p> <p>Given <math>f_0</math> and <math>f_L</math>, determine the value of product <math>R1C1</math> by using Fig.29.            Calculate <math>f_{off}</math> from the equation <math>f_{off} = f_0 - 1.6f_L</math>.            Obtain the values of <math>C1</math> and <math>R2</math> by using Fig.28.            Calculate the value of <math>R1</math> from the value of <math>C1</math> and the product <math>R1C1</math>.</p>

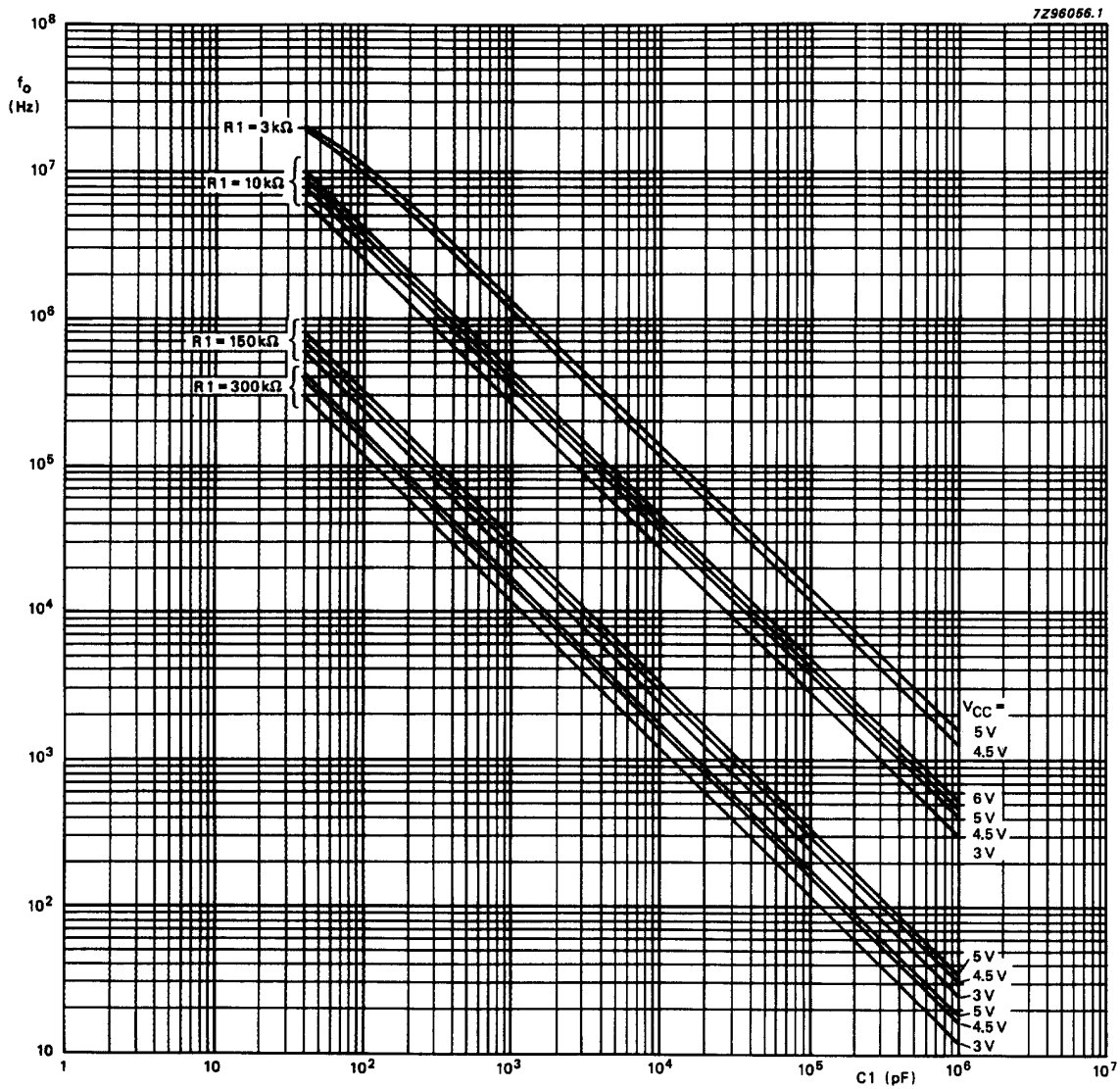
Phase-locked-loop with lock detector

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SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
PLL conditions with no signal at the SIG <sub>IN</sub> input	PC1	VCO adjusts to $f_o$ with $\phi_{\text{DEMOUT}} = 90^\circ$ and $V_{\text{VCOIN}} = 1/2 V_{\text{CC}}$ (see Fig.6).
	PC2	VCO adjusts to $f_o$ with $\phi_{\text{DEMOUT}} = -360^\circ$ and $V_{\text{VCOIN}} = \text{min.}$ (see Fig.8).
PLL frequency capture range	PC1, PC2	<p><b>Loop filter component selection</b></p>    <p>(a) <math>\tau = R3 \times C2</math>    (b) amplitude characteristic    (c) pole-zero diagram</p> <p>Fig. 25 Simple loop filter for PLL <b>without</b> offset; <math>R3 \geq 500 \Omega</math>.</p>
		   <p>(a) <math>\tau1 = R3 \times C2</math>;    (b) amplitude characteristic    (c) pole-zero diagram  <math>\tau2 = R4 \times C2</math>;  <math>\tau3 = (R3 + R4) \times C2</math></p> <p>Fig. 26 Simple loop filter for PLL <b>with</b> offset; <math>R3 + R4 \geq 500 \Omega</math>.</p>
PLL locks on harmonics at centre frequency	PC1	yes
	PC2	no
noise rejection at signal input	PC1	high
	PC2	low
AC ripple content when PLL is locked	PC1	$f_r = 2f_i$ , large ripple content at $\phi_{\text{DEMOUT}} = 90^\circ$
	PC2	$f_r = f_i$ , small ripple content at $\phi_{\text{DEMOUT}} = 0^\circ$

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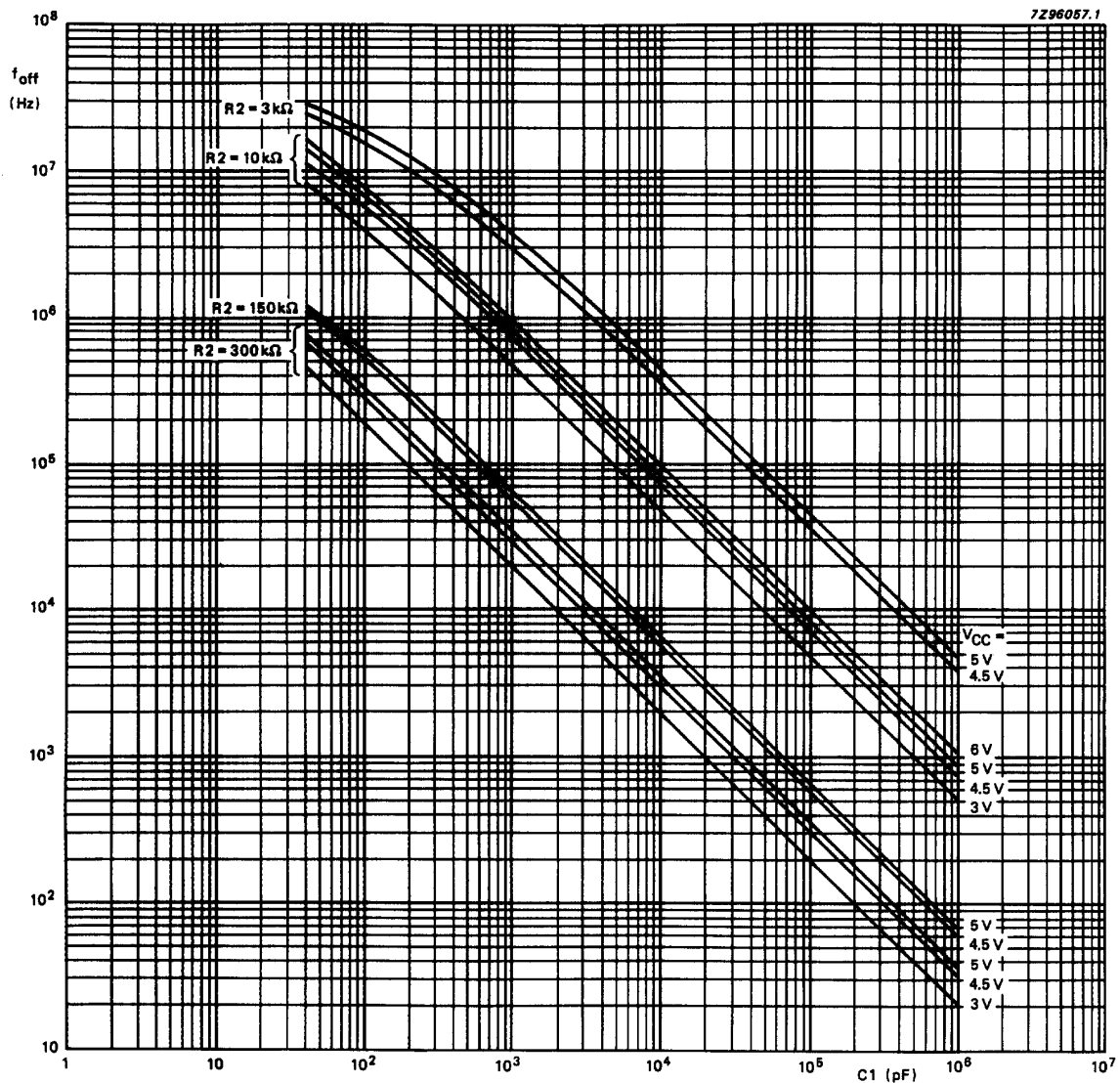
- (1) To obtain optimum VCO performance,  $C1$  must be as small as possible but larger than 100 pF.
- (2) Interpolation for various values of  $R1$  can be easily calculated because a constant  $R1C1$  product will produce almost the same VCO output frequency.

Fig.27 Typical value of VCO centre frequency ( $f_o$ ) as a function of  $C1$ :  $R2 = \infty$ ;  $V_{VCOIN} = 1/2 V_{CC}$ ;  $INH = GND$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ .

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APPLICATION INFORMATION



- (1) To obtain optimum VCO performance,  $C_1$  must be as small as possible but larger than 100 pF.
- (2) Interpolation for various values of  $R_2$  can be easily calculated because a constant  $R_2C_2$  product will produce almost the same VCO output frequency.

Fig.28 Typical value of frequency offset as a function of  $C_1$ :  $R_1 = \infty$ ;  $V_{VCOIN} = 1/2 V_{CC}$ ;  $INH = GND$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ .

Phase-locked-loop with lock detector

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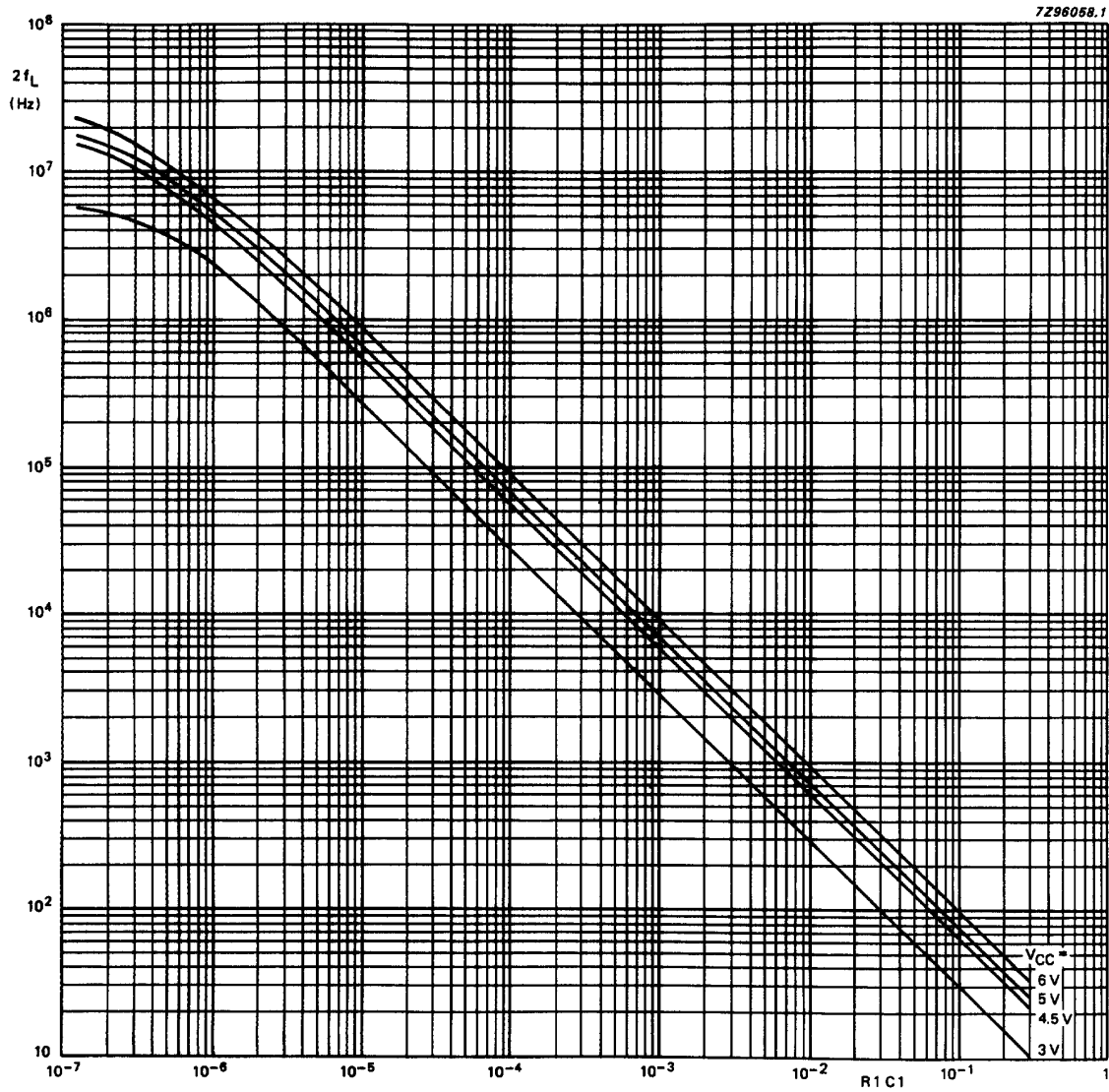


Fig.29 Typical frequency lock range ( $2f_L$ ) versus the product  $R1C1$ :  $V_{VCOIN}$  range = 0.9 to  $(V_{CC} - 0.9)$  V;  $R2 = \infty$ ; VCO gain:

$$K_V = \frac{2f_L}{V_{VCOIN} \text{ range}} 2\pi \text{ (r/s/V)}.$$



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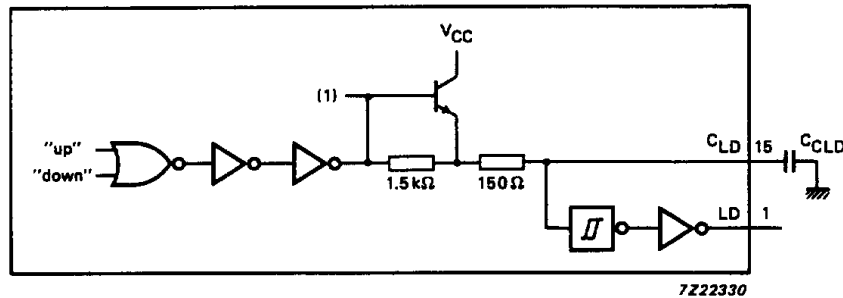
## APPLICATION INFORMATION

### Lock-detection circuit

The built-in lock-detection circuit will only work when used in conjunction with the phase comparator PC2. The lock-indication is derived from the phase error between SIG<sub>IN</sub> and COMP<sub>IN</sub>. The PC2 has a typical phase error of zero degrees over the entire VCO operating range. However, to remain in-lock the circuit requires some small adjustments. The variation is dependent on the loop parameters and back-lash time (typically 5 ns). Depending

on the application, the phase error can be defined as the limit, a phase error of greater magnitude would be considered out-of-lock. An example of an in-lock detection circuit using the "7046A" is shown in Fig.30.

If the PLL is in-lock, only very small pulses will come from the "up" or "down" connections of PC2. These pulses are filtered out by a RC network. A Schmitt trigger produces a steady state level, a HIGH level indicates an in-lock condition and a pulsed output indicates an out-of-lock condition as shown in Fig.31.



See Fig.31 for input waveform.

Fig.30 An example of an in-lock detection circuit using the "7046A".

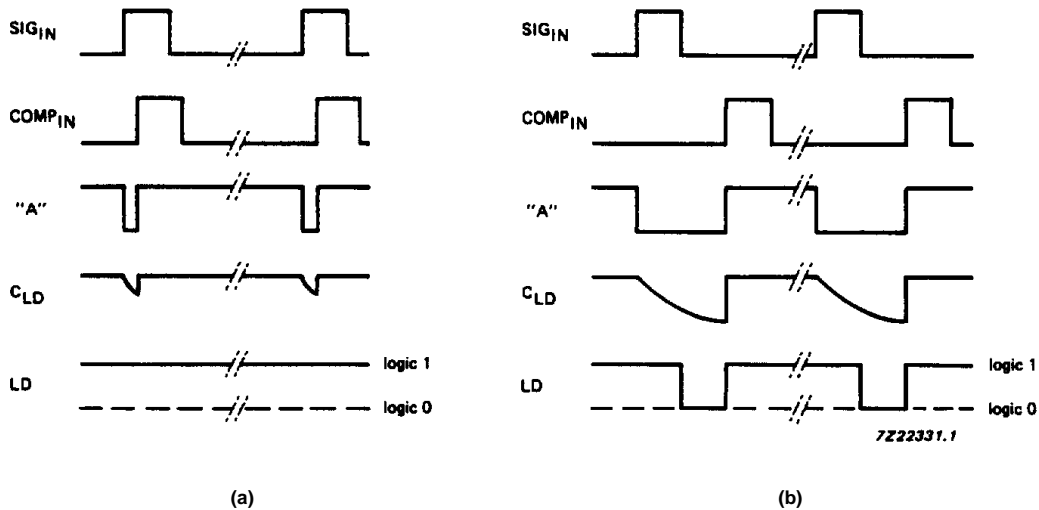
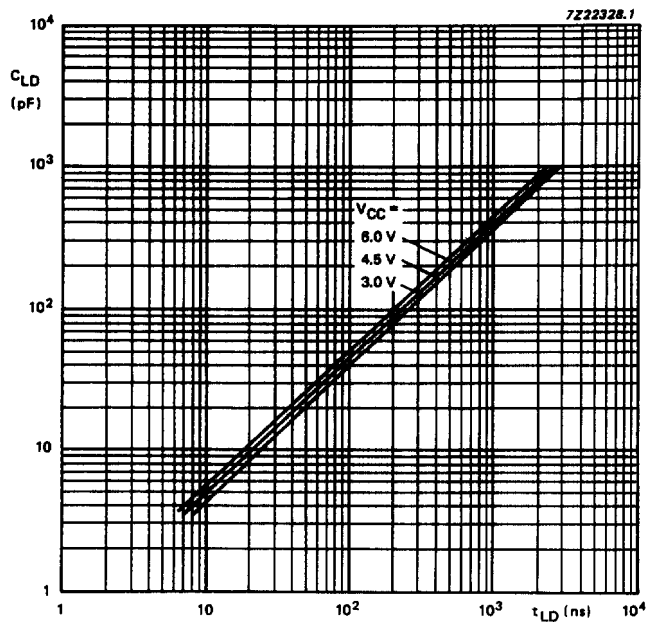


Fig.31 Waveforms showing the lock detection process; (a) in-lock; (b) out-of-lock.

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- $C_{LD}$  = capacitor connected to pin 15  
(includes the parasitic input capacitance of the IC, approximately 3.5 pF).
- $t_{LD}$  = phase difference between  $SIG_{IN}$  and  $COMP_{IN}$  (positive-going edges).

Fig.32  $C_{LD}$  capacitor value versus typical  $t_{LD}$ .

Phase-locked-loop with lock detector

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The maximum permitted phase error must be defined, before  $t_{LD}$  can be defined using the following formula:

$$t_{LD} = \frac{\phi_{max}}{360} \times \frac{1}{f_{IN}}$$

Using this calculated value in Fig.32, it is possible to define the value of  $C_{LD}$ , e.g. assuming the phase error is  $36^\circ$  and  $f_{IN} = 2$  MHz:

$$t_{LD} = \frac{36^\circ}{360} \times \frac{1}{2 \text{ MHz}} = 50 \text{ ns,}$$

and using Fig.32, it can be seen that  $C_{LD}$  is 26 pF.

With the addition of one retriggerable monostable (e.g. "123", "423" or "4538") a steady state LOW and HIGH indication can be obtained, as shown in Fig.33.

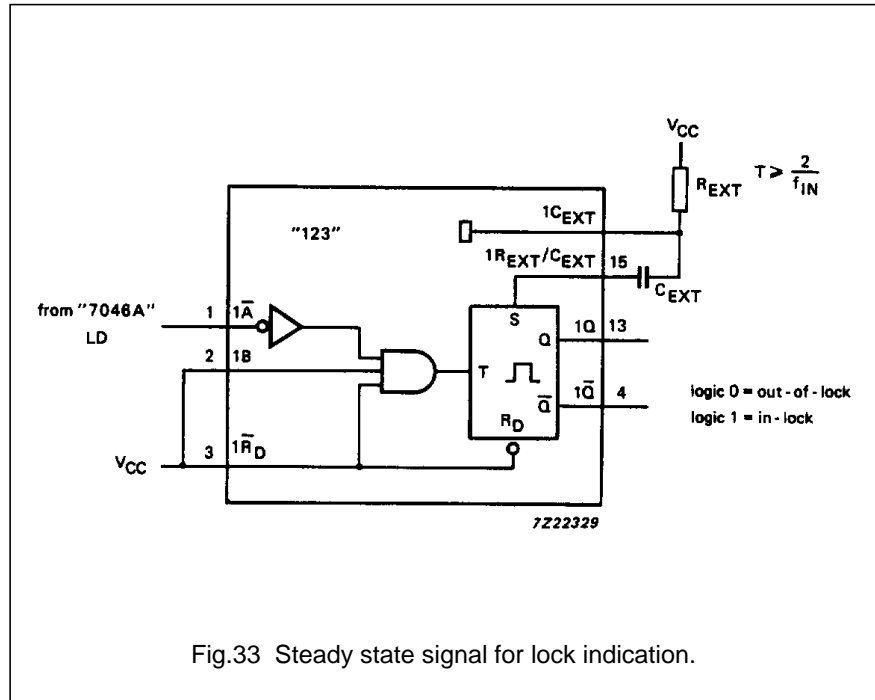


Fig.33 Steady state signal for lock indication.

## Phase-locked-loop with lock detector

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**PLL design example**

The frequency synthesizer, used in the design example shown in Fig.34, has the following parameters:

Output frequency: 2 MHz to 3 MHz  
 frequency steps : 100 kHz  
 settling time : 1 ms  
 overshoot : < 20%

The open-loop gain is  $H(s) \times G(s) = K_p \times K_f \times K_o \times K_n$ .

**Where:**

$K_p$  = phase comparator gain  
 $K_f$  = low-pass filter transfer gain  
 $K_o$  =  $K_v/s$  VCO gain  
 $K_n$  = 1/n divider ratio

The programmable counter ratio  $K_n$  can be found as follows:

$$N_{\min.} = \frac{f_{\text{out}}}{f_{\text{step}}} = \frac{2 \text{ MHz}}{100 \text{ kHz}} = 20$$

$$N_{\max.} = \frac{f_{\text{out}}}{f_{\text{step}}} = \frac{3 \text{ MHz}}{100 \text{ kHz}} = 30$$

The VCO is set by the values of R1, R2 and C1, R2 = 10 k $\Omega$  (adjustable). The values can be determined using the information in the section "DESIGN CONSIDERATIONS".

With  $f_o = 2.5$  MHz and  $f_L = 500$  kHz this gives the following values ( $V_{CC} = 5.0$  V):

R1 = 10 k $\Omega$   
 R2 = 10 k $\Omega$   
 C1 = 500 pF

The VCO gain is:

$$K_v = \frac{2f_L \times 2 \times \pi}{0.9 - (V_{CC} - 0.9)} = = \frac{1 \text{ MHz}}{3.2} \times 2\pi \approx 2 \times 10^6 \text{ r/s/V}$$

The gain of the phase comparator is:

$$K_p = \frac{V_{CC}}{4 \times \pi} = 0.4 \text{ V/r.}$$

The transfer gain of the filter is given by:

$$K_f = \frac{1 + \tau_2 s}{1 + (\tau_1 + \tau_2) s}$$

**Where:**

$\tau_1 = R3C2$  and  $\tau_2 = R4C2$ .

The characteristics equation is:

$$1 + H(s) \times G(s) = 0.$$

This results in:

$$s^2 + \frac{1 + K_p \times K_v \times K_n \times \tau_2}{(\tau_1 + \tau_2)} s + \frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)} = 0.$$

The natural frequency  $\omega_n$  is defined as follows:

$$\omega_n = \sqrt{\frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)}}.$$

and the damping value  $\zeta$  is defined as follows:

$$\zeta = \frac{1}{2\omega_n} \times \frac{1 + K_p \times K_v \times K_n \times \tau_2}{\tau_1 + \tau_2}.$$

The overshoot and settling time percentages are now used to determine  $\omega_n$ . From Fig.35 it can be seen that the damping ratio  $\zeta = 0.8$  will produce an overshoot of less than 20% and settle to within 5% at  $\omega_n t = 4.5$ . The required settling time is 1 ms. This results in:

$$\omega_n = \frac{5}{t} = \frac{5}{0.001} = 5 \times 10^3 \text{ r/s.}$$

Rewriting the equation for natural frequency results in:

$$(\tau_1 + \tau_2) = \frac{K_p \times K_v \times K_n}{\omega_n^2}.$$

The maximum overshoot occurs at  $N_{\max.}$ :

$$(\tau_1 + \tau_2) = \frac{0.4 \times 2 \times 10^6}{5000^2 \times 30} = 0.0011 \text{ s.}$$

When C2 = 470 nF, then

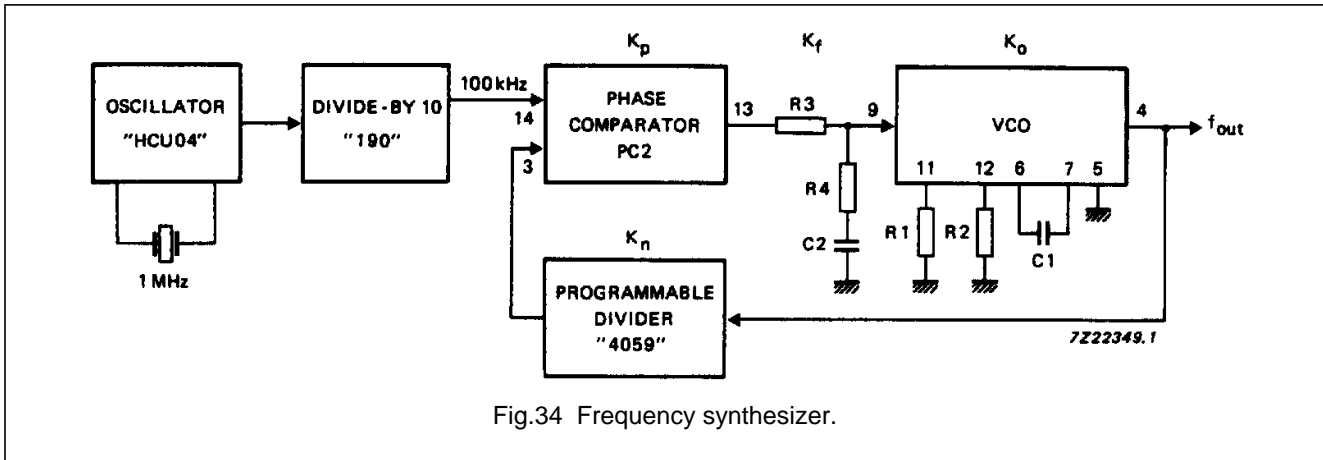
$$R4 = \frac{(\tau_1 + \tau_2) \times 2 \times \omega_n \times \zeta - 1}{K_p \times K_v \times K_n} = 790 \text{ } \Omega.$$

R3 is calculated using the damping ratio equation:

$$R3 = \frac{\tau_1}{C2} - R4 = 2 \text{ k}\Omega.$$

Phase-locked-loop with lock detector

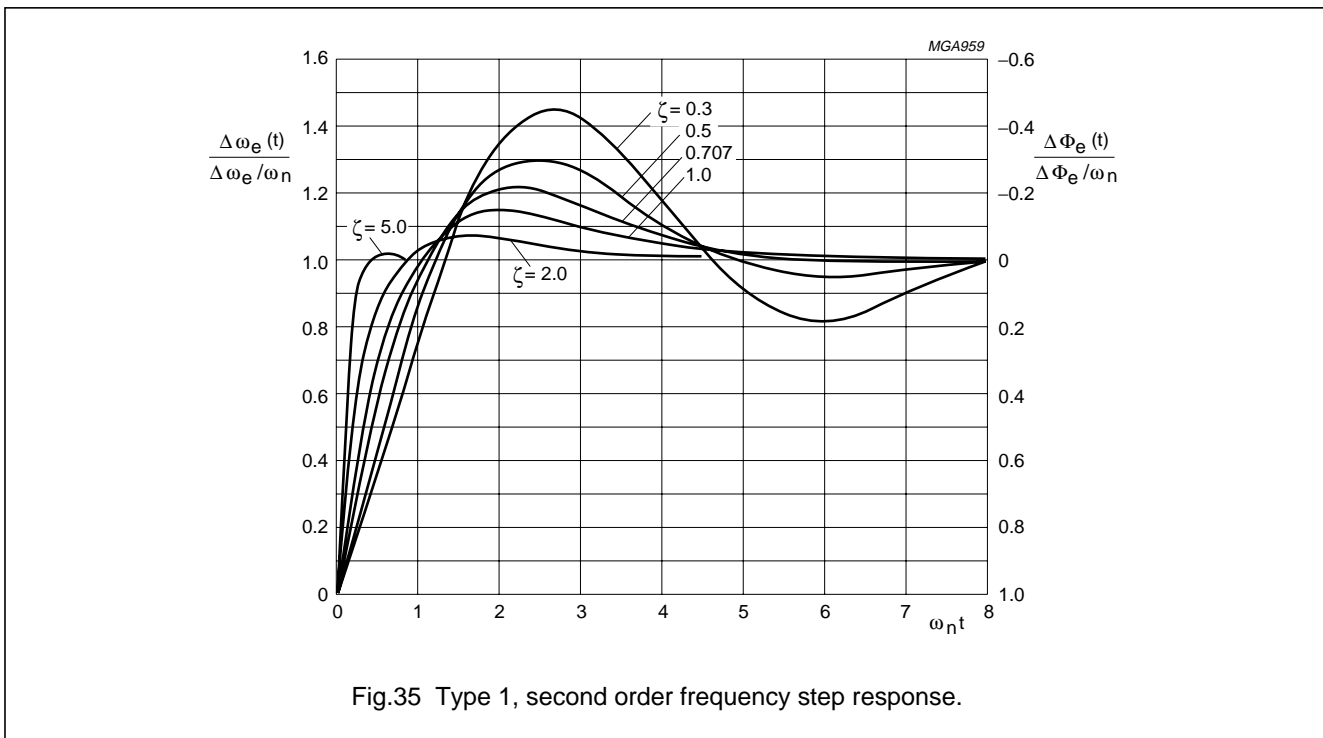
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**Note**

For an extensive description and application example please refer to application note ordering number 9398 649 90011.

Also available a computer design program for PLL's ordering number 9398 961 10061.



Since the output frequency is proportional to the VCO control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin 9 of the VCO. The average frequency response, as calculated by the Laplace method, is found experimentally by smoothing this voltage at pin 9 with a simple RC filter, whose time constant is long compared to the phase detector sampling rate but short compared to the PLL response time.

# Phase-locked-loop with lock detector

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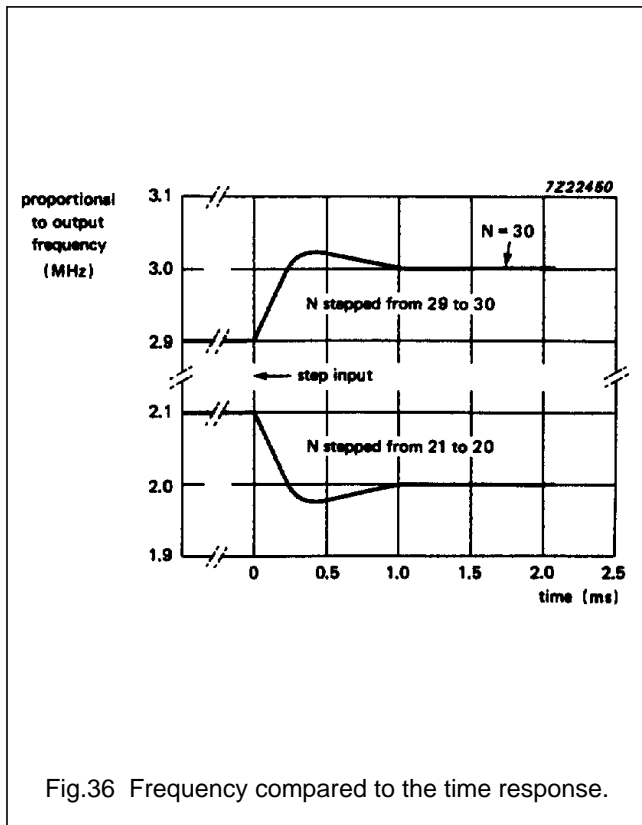


Fig.36 Frequency compared to the time response.

## PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.