Am73/8303B

Octal Three-State Inverting Bidirectional Transceiver

DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- Three-state inputs/outputs for interfacing with bus-oriented systems
- PNP inputs reduce input loading
- V_{CC} – 1.15V V_{OH} interfaces with TTL, MOS, and CMOS
- 48mA, 300pF bus drive capability
- Transmit/$\overline{\text{Receive}}$ and Chip Disable simplify control logic
- 20 pin ceramic and molded DIP package
- Low power – 8mA per bidirectional bit
- Advanced Schottky processing
- Bus port stays in hi-impedance state during power up/down
- 100% product assurance screening to MIL-STD-883 requirements

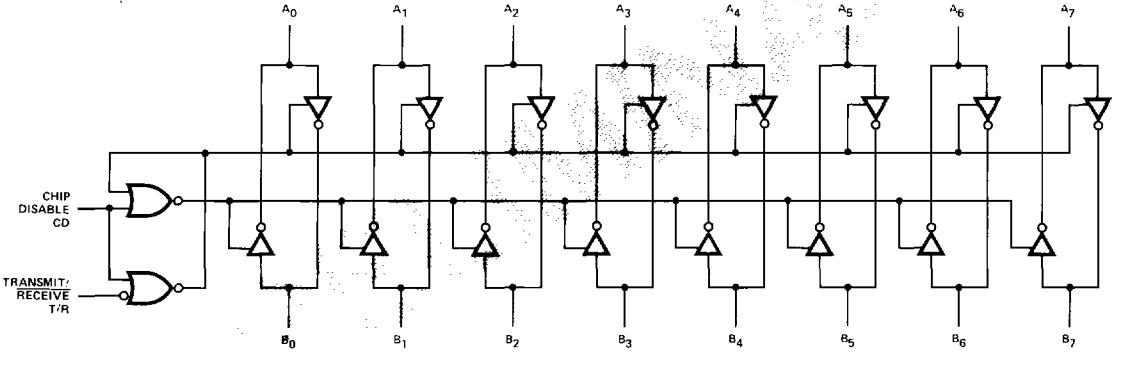
GENERAL DESCRIPTION

The Am73/8303Bs are 8-bit three-state Schottky inverting transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 16mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

One input, Transmit/$\overline{\text{Receive}}$ determines the direction of logic signals through the bidirectional transceiver. The Chip Disable input disables both A and B ports by placing them in a three-state condition.

The output high voltage (V_{OH}) is specified at V_{CC} – 1.15V minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

LOGIC DIAGRAM



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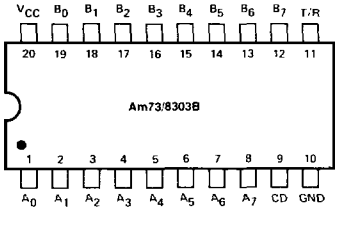
CONNECTION DIAGRAM
Top View



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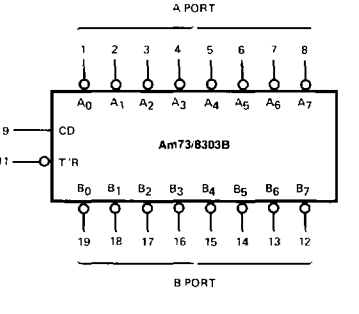
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

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ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Lead Temperature (Soldering, 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

Am7303B T_A = −55°C to +125°C V_{CC}MIN = 4.5V V_{CC}MAX = 5.5V
Am8303B T_A = 0°C to +70°C V_{CC}MIN = 4.75V V_{CC}MAX = 5.25V

DC ELECTRICAL CHARACTERISTICS over operating temperature range

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
		A PORT (A_0-A_7)					
V_{IH}	Logical "1" Input Voltage	CD = 0.8V, T/$\overline{R}$ = 2.0V		2.0			Volts
V_{IL}	Logical "0" Input Voltage	CD = 0.8V, T/$\overline{R}$ = 2.0V	Am8303B			0.8	Volts
			Am7303B			0.7	
V_{OH}	Logical "1" Output Voltage	CD = 0.8V, T/$\overline{R}$ = 0.8V	I_{OH} = −0.4mA	V_{CC}−1.15	V_{CC}−0.7		Volts
			I_{OH} = −3.0mA	2.7	3.95		
V_{OL}	Logical "0" Output Voltage	CD = 0.8V, T/$\overline{R}$ = 0.8V	I_{OL} = 8mA		0.3	0.4	Volts
			Am8303B, I_{OL} = 16mA		0.35	0.50	
I_{OS}	Output Short Circuit Current	CD = 0.8V, T/$\overline{R}$ = 0.8V, V_O = 0V, V_{CC} = MAX., Note 2		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	CD = 0.8V, T/$\overline{R}$ = 2.0V, V_I = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = MAX., V_I = V_{CC} MAX.				1	mA
I_{IL}	Logical "0" Input Current	CD = 0.8V, T/$\overline{R}$ = 2.0V, V_I = 0.4V			−70	−200	μA
V_C	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12mA			−0.7	−1.5	Volts
I_{OD}	Output/Input Three-State Current	CD = 2.0V	V_O = 0.4V			−200	μA
			V_O = 4.0V			80	
		B PORT (B_0-B_7)					
V_{IH}	Logical "1" Input Voltage	CD = 0.8V, T/$\overline{R}$ = 0.8V		2.0			Volts
V_{IL}	Logical "0" Input Voltage	CD = 0.8V, T/$\overline{R}$ = 0.8V	Am8303B			0.8	Volts
			Am7303B			0.7	
V_{OH}	Logical "1" Output Voltage	CD = 0.8V, T/$\overline{R}$ = 2.0V	I_{OH} = −0.4mA	V_{CC}−1.15	V_{CC}−0.8		Volts
			I_{OH} = −5mA	2.7	3.9		
			I_{OH} = −10mA	2.4	3.6		
V_{OL}	Logical "0" Output Voltage	CD = 0.8V, T/$\overline{R}$ = 2.0V	I_{OL} = 20mA		0.3	0.4	Volts
			I_{OL} = 48mA		0.4	0.5	
I_{OS}	Output Short Circuit Current	CD = 0.8V, T/$\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = MAX., Note 2		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	CD = 0.8V, T/$\overline{R}$ = 0.8V, V_I = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = MAX., V_I = V_{CC} MAX.				1	mA
I_{IL}	Logical "0" Input Current	CD = 0.8V, T/$\overline{R}$ = 0.8V, V_I = 0.4V			−70	−200	μA
V_C	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12mA			−0.7	−1.5	Volts
I_{OD}	Output/Input Three-State Current	CD = 2.0V	V_O = 0.4V			−200	μA
			V_O = 4.0V			200	
		CONTROL INPUTS CD, T/$\overline{R}$					
V_{IH}	Logical "1" Input Voltage			2.0			Volts
V_{IL}	Logical "0" Input Voltage					0.8	Volts
I_{IH}	Logical "1" Input Current	V_I = 2.7V			0.5	20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX., V_I = V_{CC} MAX.				1.0	mA
I_{IL}	Logical "0" Input Current	V_I = 0.4V	T/$\overline{R}$		−0.1	−.25	mA
			CD		−0.25	−.5	
V_C	Input Clamp Voltage	I_{IN} = −12mA			−0.8	−1.5	Volts
		POWER SUPPLY CURRENT					
I_{CC}	Power Supply Current	CD = 2.0V, V_{CC} = MAX., V_{IN} = 0.4V			60	130	mA
		CD = V_{INA} = 0.4V, T/$\overline{R}$ = 2V, V_{CC} = MAX.			80	160	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

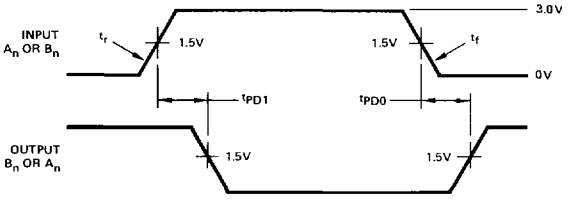
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
A PORT DATA/MODE SPECIFICATIONS						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF		8		ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF		7		ns
t_{PLZA}	Propagation Delay from a Logical "0" to Three-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF		11		ns
t_{PHZA}	Propagation Delay from a Logical "1" to Three-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF		8		ns
t_{PZLA}	Propagation Delay from Three-State to a Logical "0" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF		27		ns
t_{PZHA}	Propagation Delay from Three-State to a Logical "1" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF		19		ns
B PORT DATA/MODE SPECIFICATIONS						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF		12		ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF		7		
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF		10		ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF		7		
t_{PLZB}	Propagation Delay from a Logical "0" to Three-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF		13		ns
t_{PHZB}	Propagation Delay from a Logical "1" to Three-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF		8		ns
t_{PZLB}	Propagation Delay from Three-State to a Logical "0" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF		32		ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF		16		
t_{PZHB}	Propagation Delay from Three-State to a Logical "1" from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF		26		ns
		S_3 = 0, R_5 = 667Ω, C_4 = 45pF		14		
TRANSMIT RECEIVE MODE SPECIFICATIONS						
t_{PHZR}	Propagation Delay from a Logical "1" to Three-State from T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 0, R_3 = 1k, C_2 = 15pF		7		ns
t_{PLZR}	Propagation Delay from a Logical "0" to Three-State from T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 1, R_3 = 1k, C_2 = 15pF		10		ns
t_{PHZT}	Propagation Delay from a Logical "1" to Three-State from T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 15pF S_2 = 1, R_3 = 5k, C_2 = 30pF		16		ns
t_{PLZT}	Propagation Delay from a Logical "0" to Three-State from T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 1k, C_3 = 15pF S_2 = 0, R_3 = 1k, C_2 = 30pF		17		ns
t_{PRL}	Propagation Delay from Transmit Mode to a Logical "0", T/$\overline{R}$ to A Port	$t_{PRL} = t_{PHZT} + t_{PDHLA}$		23		ns
t_{PRH}	Propagation Delay from Transmit Mode to a Logical "1", T/$\overline{R}$ to A Port	$t_{PRH} = t_{PLZT} + t_{PDLHA}$		28		ns
t_{PTL}	Propagation Delay from Receive Mode to a Logical "0", T/$\overline{R}$ to B Port	$t_{PTL} = t_{PHZR} + t_{PDHLB}$		23		ns
t_{PTH}	Propagation Delay from Receive Mode to a Logical "1", T/$\overline{R}$ to B Port	$t_{PTH} = t_{PLZR} + t_{PDLHB}$		24		ns

Notes: 1. All typical values given are for V_{CC} = 5.0V and T_A = 25°C.
2. Only one output at a time should be shorted.

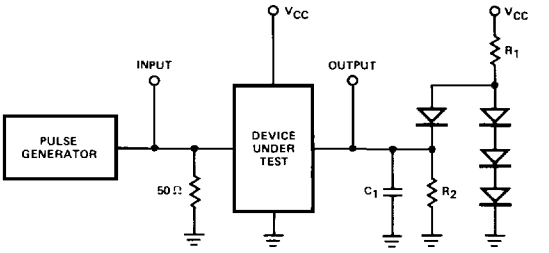
FUNCTIONAL TABLE

Inputs	Conditions		
Chip Disable	0	0	1
Transmit/$\overline{Receive}$	0	1	X
A Port	Out	In	HI-Z
B Port	In	Out	HI-Z

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS



$t_r = t_f < 10ns$
10% to 90%



Note: C_1 includes test fixture capacitance.

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Figure 1. Propagation Delay from A Port to B Port or from B Port to A Port.

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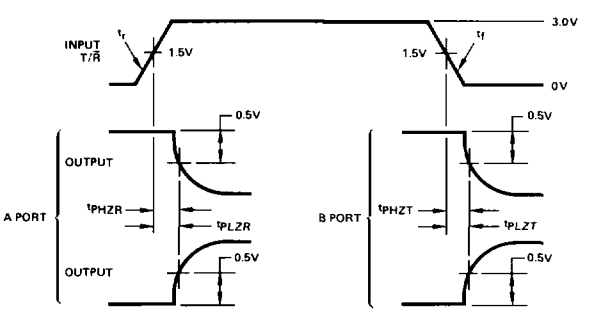
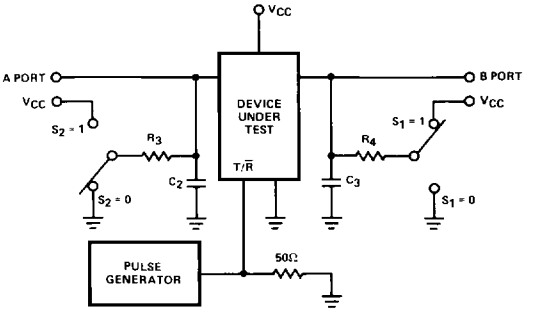


$t_r = t_f < 10ns$
10% to 90%



Note: C_2 and C_3 include test fixture capacitance.

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Figure 2. Propagation Delay from T/$\overline{R}$ to A Port or B Port.

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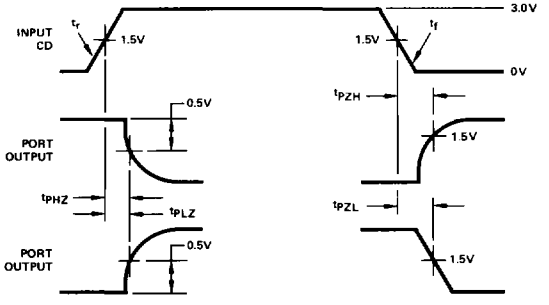
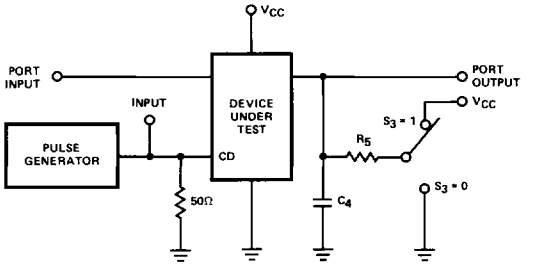


$t_r = t_f < 10ns$
10% to 90%



Note: C_4 includes test fixture capacitance.
Port input is in a fixed logical condition.

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Figure 3. Propagation Delay from CD to A Port or B Port.

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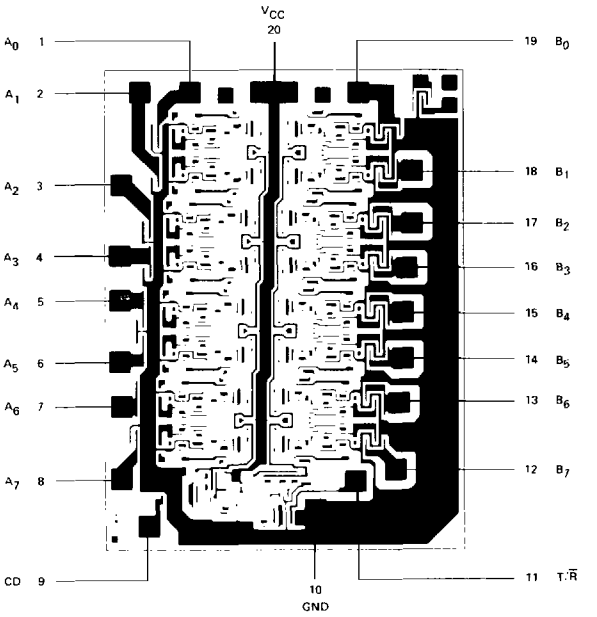
Metallization and Pad Layout



DIE SIZE 0.066" x 0.086"

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	DP7303BJ
Hermetic DIP	0°C to +70°C	DP8303BJ
Molded DIP	0°C to +70°C	DP8303BN
Dice	0°C to +70°C	AM8303BX