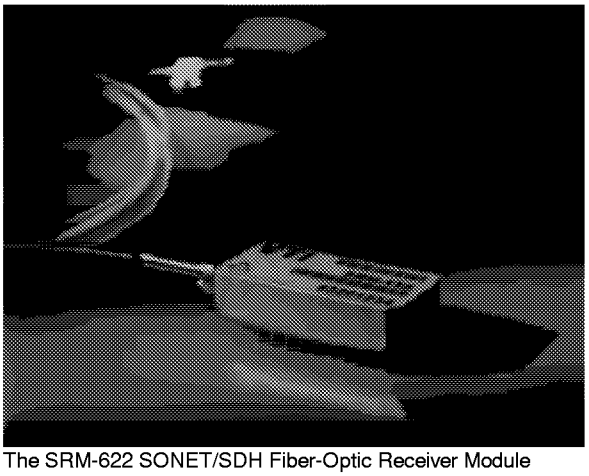
VECTRON INTERNATIONAL
A DOVER TECHNOLOGIES COMPANY

Product Data Sheet

SRM-622

SONET/SDH Fiber-Optic Receiver Module with SAW Filter Clock Recovery and Data Retiming



The SRM-622 SONET/SDH Fiber-Optic Receiver Module

Features

- SONET OC-12 and SDH STM-4 Compatible
- SAW Filter Clock Recovery and Data Retiming
- 10 ps Typical Output Jitter
- PECL Clock and Data Outputs
- Single +5 Volt Supply
- CMOS Loss of Signal Flag
- Operation at 1300 nm and 1550 nm
- -45° to +85°C Operation
- Wide Dynamic Range
- Multi-Sourced 20 Pin DIL Footprint
- Custom Frequencies Available from 124 to 622 MHz

Applications

- Telecom Receiver Applications
  Medium and Long Haul SONET/SDH @ 622 Mb/s
- High Performance Datacom Receiver Applications
  ATM @ 622 Mb/s

Description

VTI's SRM-622 is a fully integrated fiber-optic receiver module with SAW filter clock recovery and data retiming. It is ideally suited for SONET OC-12, SDH STM-4 and other 622 Mb/s fiber-optic transmission applications that demand superior performance and stability.

Functional Overview

This highly integrated module converts a 622 Mb/s fiber-optic NRZ signal to differential PECL recovered clock and retimed data outputs. A CMOS flag alerts the user to a loss of signal condition when the optical input falls below an acceptable level.

A single +5 Volt supply provides bias for the module's pin-photodiode, preamplifier, Quantizer, and SAW filter timing recovery circuit. All elements are integrated into fiber-coupled 1.3" X 0.635" 20 pin DIL package. The SRM-622 footprint and pinout are industry common for ease of integration.

The optical signal is coupled through a short length of multimode optical fiber to a hermetic module which encases the InGaAs pin-photodiode and preamplifier. The pin-photodiode converts the optical signal to an electrical current. The signal is then converted to a voltage and amplified by a low noise transimpedance amplifier. Further gain is provided by the quantizer, which also provides a Flag output when the optical signal falls below an acceptable level. The signal is then processed by the SAW-filter timing recovery circuit where the clock signal is recovered and realigned with the reshaped data signal.

The clock recovery and data retiming function is achieved using a SAW filter technique which is well established and proven through years of application in high performance telecom systems.

The clock is extracted from the input NRZ data by first passing it through a frequency doubler to generate sufficient spectral energy at 622 MHz. The SAW filter, a precision narrow band filter, then suppresses jitter by rejecting unwanted frequency spectrum. The extracted clock is then precisely aligned with the data and the signals are reshaped.

The output signal is thus free of undesirable jitter and distortion. Unlike phase-looked loop designs, the jitter transfer function of the SRM-622's timing recovery circuit is uniquely stable because it is determined by the shape of the SAW filter's response, which is precisely controlled. In addition to low output jitter and excellent stability, the SRM-622's timing recovery circuit exhibits fast acquisition time and robust operation.

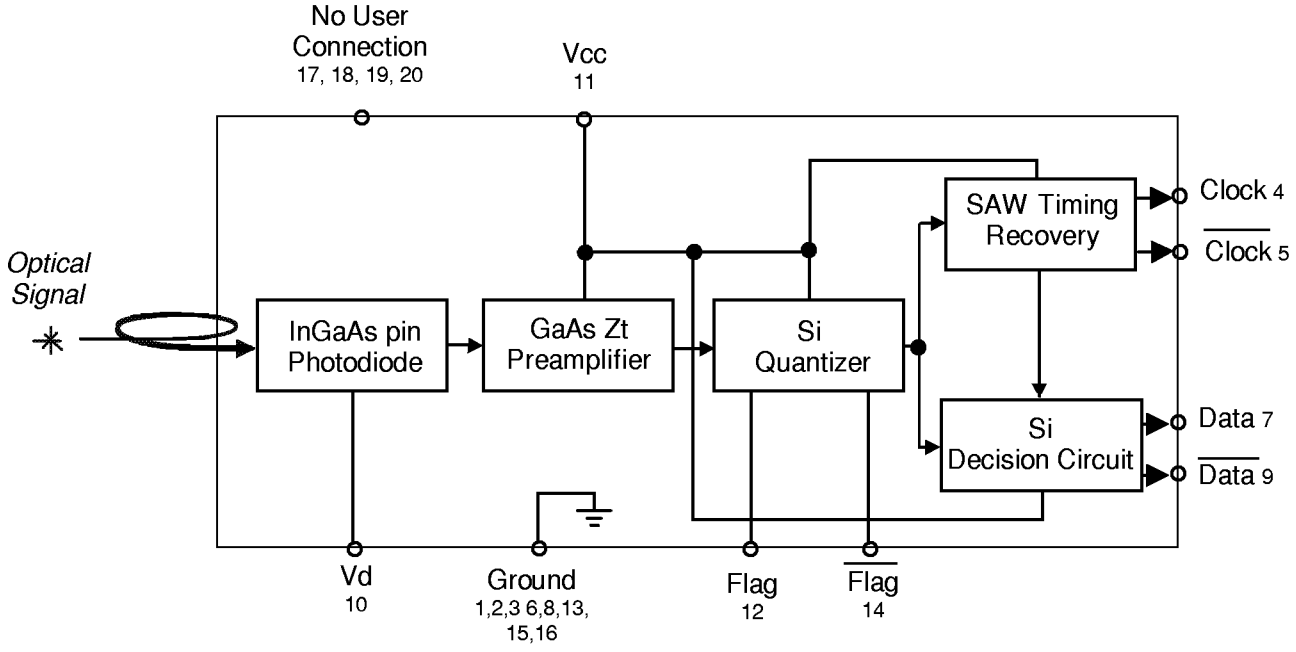


Figure 1. SRM-622 Functional Block Diagram

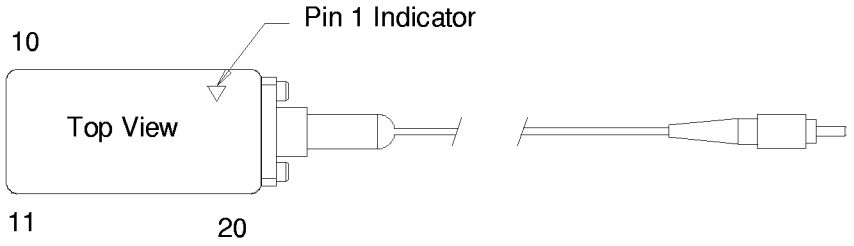


Figure 2. Pin Diagram (Top View)

Table 1. Pin Function

Pin	Symbol	Function
4	Clock	PECL Recovered Clock Output.
5	$\overline{\text{Clock}}$	PECL Complementary Recovered Clock Output.
7	Data	PECL Retimed Data Output.
9	$\overline{\text{Data}}$	PECL Complementary Retimed Data Output.
10	V_D	Detector Anode Bias. Connect to +5 Volts or connect to 5 Volts through a series resistor for received optical power monitoring.[1]
11	V_{CC}	5 Volt Supply Voltage.
12	Flag	Input Signal Level Status. This CMOS output switches low when the received optical power falls below the status minimum optical power level.
14	$\overline{\text{Flag}}$	Complementary Input Signal Status. CMOS complement of Flag.
1,2,3,6,8,13,15,16	GND	Ground.
17,18,19,20	NC	No User Connection.

1. By connecting pin 10 to a +5 Volt bias through a series resistor (eg. 1 kΩ) received optical power can be monitored as a voltage drop across the resistor.

Absolute Maximum Ratings

Absolute maximum ratings are provided here as worst case and short duration exposure conditions only. Exposure to conditions more severe than the Absolute Maximum Ratings may result in permanent damage. Exposure to conditions at the Absolute Maximum Ratings for extended periods may also adversely affect device performance or reliability. Functional operation of the device is not implied at these conditions.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Storage Temperature Range	T_S	-40	85	°C
Supply Voltage	V_{CC}	0	+6	V
pin Detector Bias	V_D	0	+6	V
Lead Soldering Conditions			250/10	°C/s

Performance Characteristics

Table 2. Electrical Performance

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Signal Rate[1]	f_O	621.956	622.08	622.204	Mb/s
Operating Temperature	T_O	-40		+85	°C
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
pin Detector Bias Voltage (pin10)	V_D	0	5.0	5.5	V
Power Supply Current	I_{CC}			300	mA
Data and Clock Output Levels [2]					
Low	V_{OL}	V_{CC} - 1.95		V_{CC} - 1.63	V
High	V_{OH}	V_{CC} - 1.03		V_{CC} - 0.88	V
Clock to Data Alignment [3]	T_{CDA}	-100		+100	ps
Data and Clock Output Rise and Fall Times [4]	T_R, T_F	275	375	500	ps
Output Clock Duty Cycle	Duty	45	50	55	%
Received Power Level Flag	LOS				
Decreasing Optical Power			-34		dBm
Increasing Optical Power			-31		dBm
Flag Hysteresis	Hyst		3		dB
Acquisition Time [5]	T_A			2	µs
Output Clock Random Jitter [6]	J_C		10		ps rms

1. Other center frequencies are available in the 124 to 622 MHz frequency range. Please contact VTI for further details.
2. Measured with a load of R_L = 50Ω to V_{CC} - 2 V. See figures 3 and 4. ECL levels are specified for dc measurement, an additional tolerance of 50 mV should be included for dynamic measurements.
3. Alignment of clock and data outputs (see Figure 5.).
4. Measured at 20% to 80% levels.
5. Time required to achieve valid data and clock outputs with a transition density of at least 50%.
6. Measured with an input data pseudorandum word 2^{23} - 1.

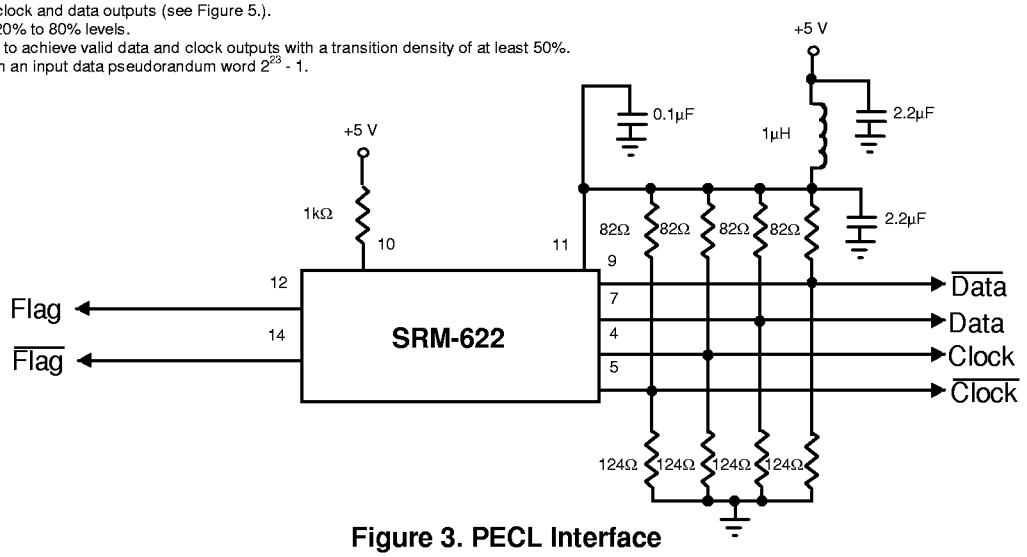


Figure 3. PECL Interface

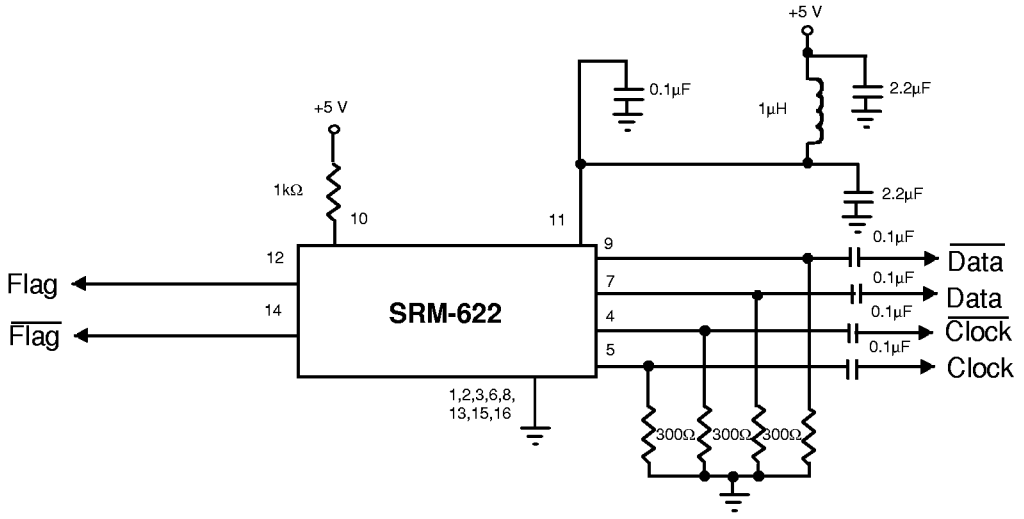


Figure 4. ECL (AC Coupled) Interface

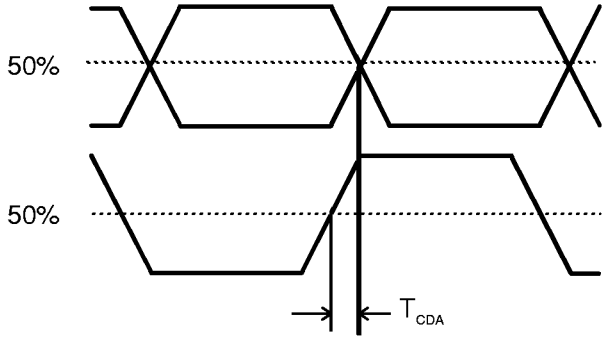


Figure 5. Clock to Data Alignment

Table 3. Optical Performance

Parameter	Symbol	Minimum	Typical	Maximum	Units
Average Sensitivity [1]	Sens.	-31	-33		dBm
Optical Input Power[1]	P_{MAX}			-6	dBm
Input Wavelength	λ	1100		1580	nm

1. For a BER less than 1E-10. Measured using a 2^{23} - 1 pseudorandum word and a 50% average optical duty cycle and a 10 dB Extinction Ratio.

Qualification

The SRM-622 has been designed to comply with the intent of Bellcore specifications TR-NWT-000468 and TA-TSSY-000983 and will be subject to a complete qualification test plan to demonstrate full compliance. All of the technologies used in the assembly of the module represent standard microelectronics technologies that are used in similar products, and have extensive field reliability data.

While all components and technologies used in the optical receiver are backed by qualification data and should present no reliability risk, VTI is presently qualifying the fully assembled module with the final design. The qualification plan will entail mechanical and environmental tests along with accelerated life tests. The tests will include those parameters listed below.

Table 4. Qualification Plan

Parameter	Test Method	Sample Size
Physical Dimensions	MIL-STD-883, Method 2016	11
Mechanical Shock	MIL-STD-883, Method2007, Test B	11
Vibration, variable frequency	MIL-STD-883, Method 2007, Test A	11
Lead Solderability	MIL-STD-883, Method 2003	22
Lead Integrity	MIL-STD-883, Method 2004	15
Temperature Cycling	-40°C/85°C, 300 cycles	11
High Temperature Aging	85°C under bias, 3000 hours	11
Low Temperature Storage	-40°C, 168 hours	11
ESD	Method 3015	3
Destructive Bond Pull	MIL-STD-883	40

Optical Fiber Characteristics

The fiber pigtail is a 34.75 +/-1 inch (measured from the package case to the connector tip) Type 2A multimode fiber with a 62.5 um core. The fiber is encased in a slate colored Strengthened Buffered Jacket (SBJ) cable sheath having a 900 um outer jacket diameter. The minimum fiber bend radius is 1.25 inches. Connectors, fiber length and fiber type may be selected to meet the specific requirements of each application.

Outline Diagram

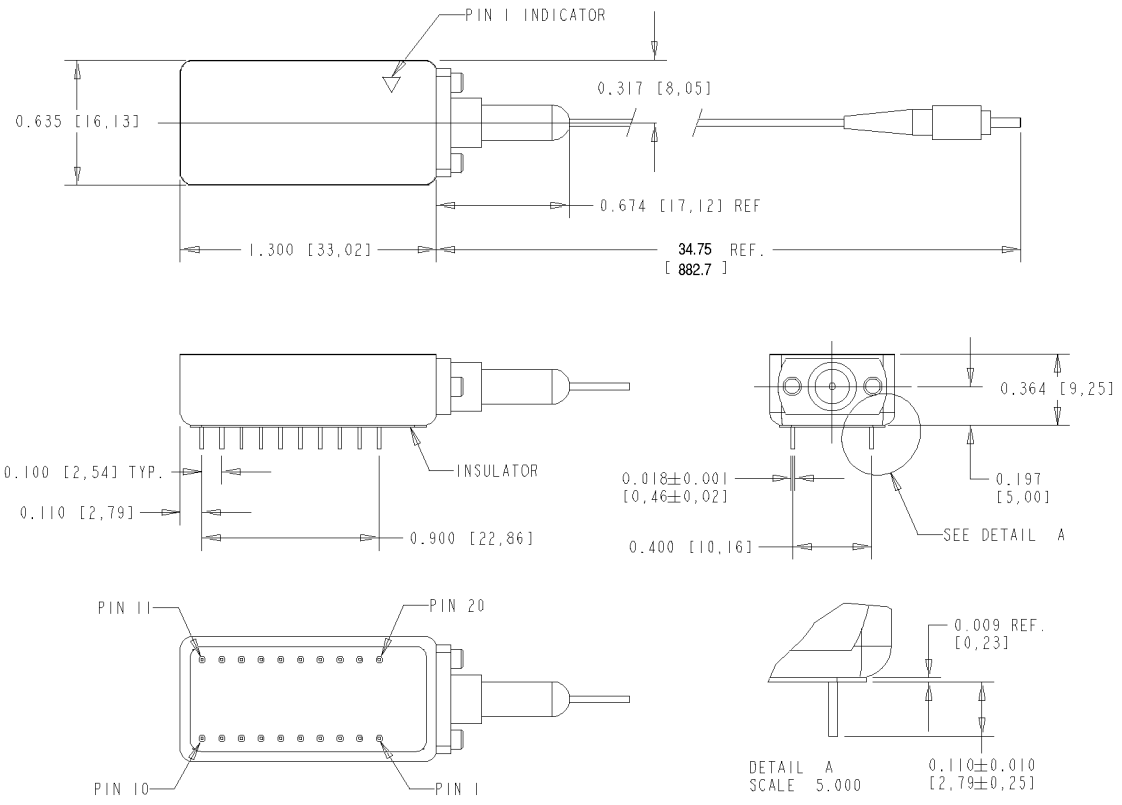


Figure 6. Outline Diagram

Ordering Information

Table 5. Part Numbers

Fiber-Optic Connector[1]	Model Number	VTI Code Number
None	SRM-622	330002999
FC/PC	SRM-622A	330003005
ST	SRM-622B	330003015
SC	SRM-622C	330003021

1. Other connectors or fiber requirements are available to meet specific application requirements.

Notes:

For Additional Information Please Contact:

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