Features

- **Fast Read Access Time - 120 ns**
- **Automatic Page Write Operation**
    - **Internal Address and Data Latches for 64 Words**
    - **Internal Control Timer**
- **Fast Write Cycle Times**
    - **Page Write Cycle Time: 10 ms maximum**
    - **1 to 64 Word Page Write Operation**
- **Low Power Dissipation**
    - **100 mA Active Current**
    - **400 µA CMOS Standby Current**
- **Hardware and Software Data Protection**
- **DATA Polling for End of Write Detection**
- **High Reliability CMOS Technology**
    - **Endurance: 10^4 or 10^5 Cycles**
    - **Data Retention: 10 years**
- **Single 5 V ± 10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **JEDEC Approved Word-Wide Pinout**
- **Full Military, Commercial, and Industrial Temperature Ranges**

2

1 Megabit (64K x 16) Paged CMOS E²PROM

Description

The AT28C1024 is a high performance Electrically Erasable and Programmable Read Only Memory. Its 1 megabit of memory is organized as 65,536 words by 16 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times down to 120 ns with power dissipation of just 550 mW. When the device is deselected, the CMOS standby current is less than 400 µA.
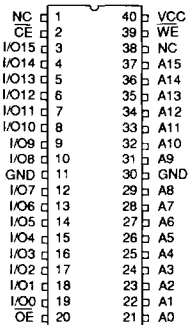
The AT28C1024 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-word page register to allow writing of up to 64 words simultaneously. During a write cycle, the addresses and 1 to 64 words of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7 or I/O15. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28C1024 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 words of E²PROM for device identification or tracking.
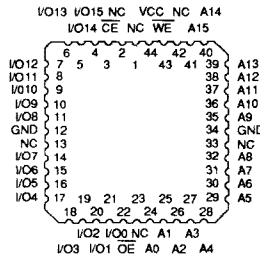
Pin Configurations

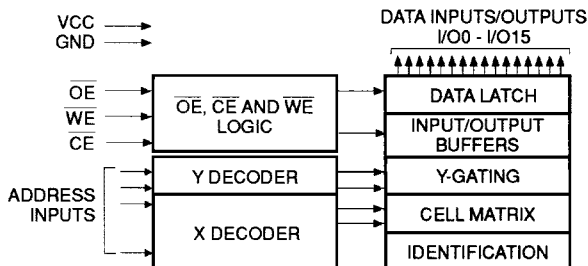| Pin Name	Function
A0 - A15	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O15	Data Inputs/Outputs
NC	No Connect

Top View

```
NC   ▯ 1      40 ▯ VCC
CE   ▯ 2      39 ▯ WE
I/O15 ▯ 3     38 ▯ NC
I/O14 ▯ 4     37 ▯ A15
I/O13 ▯ 5     36 ▯ A14
I/O12 ▯ 6     35 ▯ A13
I/O11 ▯ 7     34 ▯ A12
I/O10 ▯ 8     33 ▯ A11
I/O9  ▯ 9     32 ▯ A10
I/O8  ▯ 10    31 ▯ A9
GND   ▯ 11    30 ▯ GND
I/O7  ▯ 12    29 ▯ A8
I/O6  ▯ 13    28 ▯ A7
I/O5  ▯ 14    27 ▯ A6
I/O4  ▯ 15    26 ▯ A5
I/O3  ▯ 16    25 ▯ A4
I/O2  ▯ 17    24 ▯ A3
I/O1  ▯ 18    23 ▯ A2
I/O0  ▯ 19    22 ▯ A1
OE    ▯ 20    21 ▯ A0
```

Top View

```
        I/O13 I/O15 NC  VCC  NC  A14
         I/O14 CE  NC  WE   A15
         6   4   2  44  42  40
I/O12  7                      39  A13
I/O11  8                      38  A12
I/O10  9                      37  A11
I/O9   10                     36  A10
I/O8   11                     35  A9
GND    12                     34  GND
NC     13                     33  NC
I/O7   14                     32  A8
I/O6   15                     31  A7
I/O5   16                     30  A6
I/O4   17                     29  A5
       18  20  22  24  26  28
        17  19  21  23  25  27
         I/O2 I/O0 NC  A1  A3
          I/O3 I/O1 OE  A0  A2  A4
```

Block Diagram

Absolute Maximum Ratings*

Temperature Under Bias.................-55°C to +125°C
Storage Temperature......................-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground .... -0.6 V to +6.25 V
All Output Voltages with Respect to Ground ....-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{OE}$ and A9 with Respect to Ground ....-0.6 V to 13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C1024 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a write has been started it will automatically time itself to completion.

PAGE WRITE: The page write operation of the AT28C1024 allows one to one hundred sixty-four wordss of data to be written into the device during a single internal programming period.

A page write operation is initiated in the same manner as a single word write; the first eord written can then be followed by one to one sixty-three additional words. Each successive word must be written within 150 μs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28C1024 will cease accepting data and commence the internal programming operation. All data during a page write operation must reside on the same page as defined by the state of the A6-A15 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A6-A15 must be the same.

The A0 to A5 inputs are used to specify which words within the page are to be written. The words may be loaded in any order and may be altered within the same load period. Only words which are specified for writing will be written; unnecessary cycling of other words within the page does not occur.

Device Operation (Continued)

DATA POLLING: The AT28C1024 features $\overline{\text{DATA}}$ Polling to indicate the end of a write cycle. During a single word or page write cycle an attempted read of the last data written will result in the complement of the written data to be presented on I/O7 and I/O15. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{\text{DATA}}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{\text{DATA}}$ Polling the AT28C1024 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O14 toggling between one and zero. Once the write has completed, I/O14 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28C1024 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8 V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a write: (c) write inhibit - holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C1024. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C1024 is shipped from Atmel with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific data words are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the three word command sequence and after twc the entire AT28C1024 will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a single word or page write to the AT28C1024. This is done by preceding the data to be written by the same three word command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28C1024 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a single word or page write operation.

After setting SDP, any attempt to write to the device without the three word command sequence will start the internal write timers. No data will be written to the device; however, for the duration of twc, read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 64 words of E^2PROM memory are available to the user for device identification. By raising A9 to 12 V ± 0.5 V and using address locations FFC0H to FFFFH the additional words may be written to or read from in the same manner as the regular memory array.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

D.C. and A.C. Operating Range

		AT28C1024-12	AT28C1024-15	AT28C1024-20	AT28C0124-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
Vcc Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	$X^{(1)}$	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.

D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to Vcc + 1 V		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to Vcc		10	µA
I_{SB1}	Vcc Standby Current CMOS	$\overline{CE}$ = Vcc-0.3 V to Vcc + 1 V		400	µA
I_{SB2}	Vcc Standby Current TTL	$\overline{CE}$ = 2.0 V to Vcc + 1 V		5	mA
I_{CC}	Vcc Active Current	f = 5 MHz; I_{OUT} = 0 mA		100	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		.45	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

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AT28C1024

A.C. Read Characteristics

Symbol	Parameter	AT28C1024-12		AT28C1024-15		AT28C1024-20		AT28C1024-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200		250	ns
t_{CE} [1]	$\overline{CE}$ to Output Delay		120		150		200		250	ns
t_{OE} [2]	$\overline{OE}$ to Output Delay	0	60	0	70	0	80	0	100	ns
t_{DF} [3,4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	55	0	55	0	60	0	70	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

## A.C. Read Waveforms
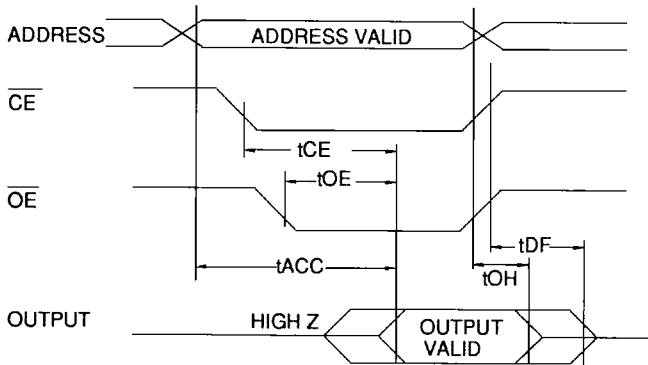
Notes:
1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level

t_R, t_F < 5 ns
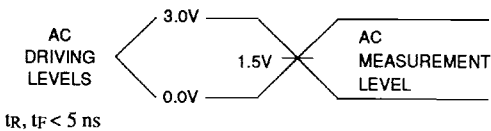
Output Test Load
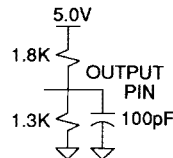
A.C. Write Characteristics

Symbol	Parameter	Min	Max	Units
tAS, tOES	Address, $\overline{OE}$ Set-up Time	0		ns
tAH	Address Hold Time	50		ns
tCS	Chip Select Set-up Time	0		ns
tCH	Chip Select Hold Time	0		ns
tWP	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
tDS	Data Set-up Time	50		ns
tDH,tOEH	Data, $\overline{OE}$ Hold Time	0		ns
tWC	Write Cycle Time		10	ms

A.C. Write Waveforms- $\overline{WE}$ Controlled
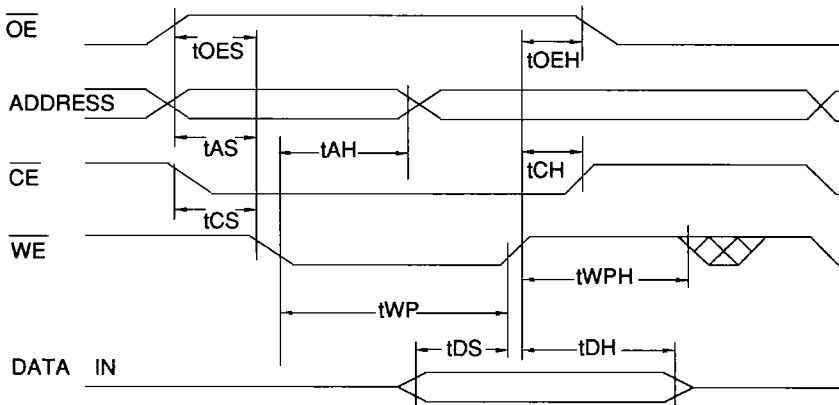
A.C. Write Waveforms- $\overline{CE}$ Controlled

AT28C1024
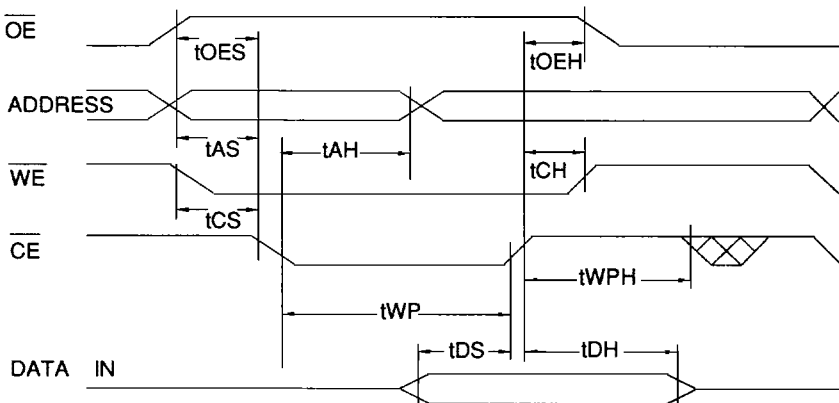
Page Mode Characteristics

Symbol	Parameter	Min	Max	Units
twc	Write Cycle Time		10	ms
tAS	Address Set-up Time	0		ns
tAH	Address Hold Time	50		ns
tDS	Data Set-up Time	50		ns
tDH	Data Hold Time	0		ns
tWP	Write Pulse Width	100		ns
tBLC	Byte Load Cycle Time		150	µs
tWPH	Write Pulse Width High	50		ns

Page Mode Write Waveforms
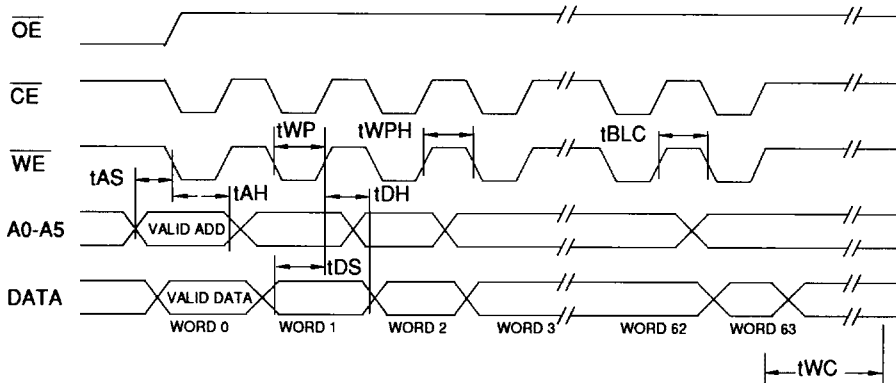
Software Data Protection Enable Algorithm [1]

```
┌─────────────────────┐
│   LOAD DATA AAAA    │
│        TO           │
│   ADDRESS 5555      │
└─────────────────────┘
          ↓
┌─────────────────────┐
│   LOAD DATA 5555    │
│        TO           │
│   ADDRESS AAAA      │
└─────────────────────┘
          ↓
┌─────────────────────┐
│   LOAD DATA A0A0    │
│        TO           │        WRITES ENABLED [2]
│   ADDRESS 5555      │
└─────────────────────┘
          ↓
┌─────────────────────┐
│   LOAD DATA XXXX    │
│        TO           │
│   ANY ADDRESS [4]   │
└─────────────────────┘
          ↓
┌─────────────────────┐
│   LOAD LAST WORD    │
│        TO           │
│   LAST ADDRESS      │       ENTER DATA
└─────────────────────┘       PROTECT STATE
```
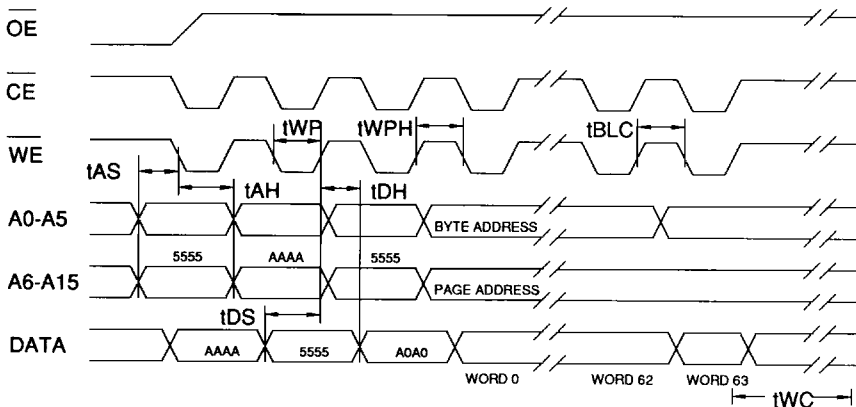
Notes:
1. Data Format: I/O15 - I/O0 (Hex);
   Address Format: A15 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 words of data are loaded.

Software Data Protection Disable Algorithm [1]

```
┌─────────────────────┐
│   LOAD DATA AAAA    │
│        TO           │
│   ADDRESS 5555      │
└─────────────────────┘
          ↓
┌─────────────────────┐
│   LOAD DATA 5555    │
│        TO           │
│   ADDRESS AAAA      │
└─────────────────────┘
          ↓
┌─────────────────────┐
│   LOAD DATA 8080    │
│        TO           │
│   ADDRESS 5555      │
└─────────────────────┘
          ↓
┌─────────────────────┐
│   LOAD DATA AAAA    │
│        TO           │
│   ADDRESS 5555      │
└─────────────────────┘
          ↓
┌─────────────────────┐
│   LOAD DATA 5555    │
│        TO           │
│   ADDRESS AAAA      │
└─────────────────────┘
          ↓
┌─────────────────────┐
│   LOAD DATA 2020    │
│        TO           │        EXIT DATA
│   ADDRESS 5555      │        PROTECT STATE [3]
└─────────────────────┘
          ↓
┌─────────────────────┐
│   LOAD DATA XXXX    │
│        TO           │
│   ANY ADDRESS [4]   │
└─────────────────────┘
          ↓
┌─────────────────────┐
│   LOAD LAST WORD    │
│        TO           │
│   LAST ADDRESS      │
└─────────────────────┘
```

Software Protected Program Cycle Waveform

Notes: A6 through A15 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
tDH	Data Hold Time	0			ns
tOEH	$\overline{\text{OE}}$ Hold Time	0			ns
tOE	$\overline{\text{OE}}$ to Output Delay			100	ns
tWR	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

WE

CE

tOEH

OE

tDH

tOE   HIGH Z   tWR

I/O7

A0-A15   An   An   An   An   An
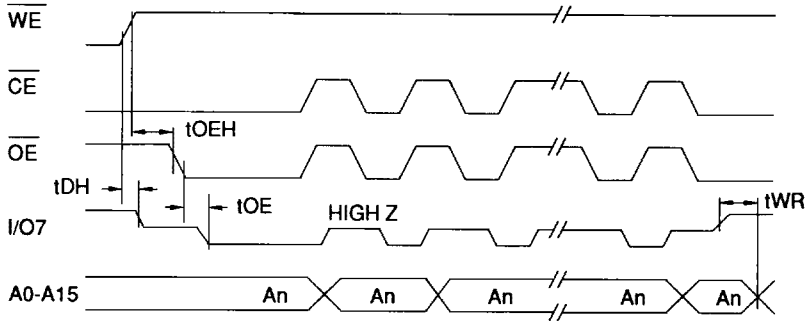
Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
tDH	Data Hold Time	10			ns
tOEH	$\overline{\text{OE}}$ Hold Time	10			ns
tOE	$\overline{\text{OE}}$ to Output Delay			100	ns
tOEHP	$\overline{\text{OE}}$ High Pulse	150			ns
tWR	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms

WE

CE

tOEH   tOEHP

OE

tDH   tOE   HIGH Z

I/O14   tWR
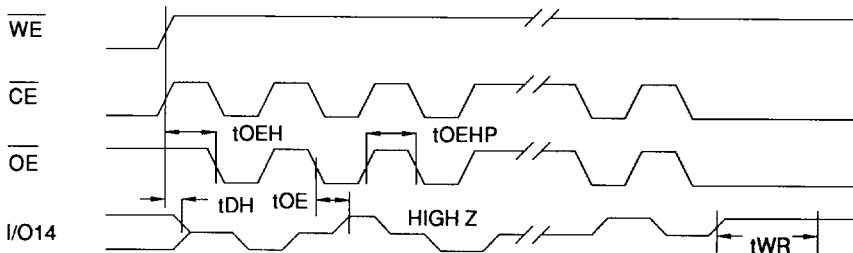
Notes:
1. Toggling either $\overline{\text{OE}}$ or $\overline{\text{CE}}$ or both $\overline{\text{OE}}$ and $\overline{\text{CE}}$ will operate toggle bit.
2. Beginning and ending state of I/O14 will vary.
3. Any address location may be used but the address should not vary.

2

Ordering Information

tACC (ns)	ICC (mA) Active	ICC (mA) Standby	Ordering Code	Package	Operation Range
120	100	0.4	AT28C1024-12BC AT28C1024-12LC	40B 44L	Commercial (0° to 70°C)
			AT28C1024-12BI AT28C1024-12LI	40B 44L	Industrial (-40° to 85°C)
150	100	0.4	AT28C1024-15BC AT28C1024-15LC	40B 44L	Commercial (0° to 70°C)
			AT28C1024-15BI AT28C1024-15LI	40B 44L	Industrial (-40° to 85°C)
			AT28C1024-15BM AT28C1024-15LM	40B 44L	Military (-55°C to 125°C)
			AT28C1024-15BM/883 AT28C1024-15LM/883	40B 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	100	0.4	AT28C1024-20BC AT28C1024-20LC	40B 44L	Commercial (0° to 70°C)
			AT28C1024-20BI AT28C1024-20LI	40B 44L	Industrial (-40° to 85°C)
			AT28C1024-20BM AT28C1024-20LM	40B 44L	Military (-55°C to 125°C)
			AT28C1024-20BM/883 AT28C1024-20LM/883	40B 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	100	0.4	AT28C1024-25BC AT28C1024-25LC AT28C1024-W	40B 44L DIE	Commercial (0° to 70°C)
			AT28C1024-25BI AT28C1024-25LI	40B 44L	Industrial (-40° to 85°C)
			AT28C1024-25BM AT28C1024-25LM	40B 44L	Military (-55°C to 125°C)
			AT28C1024-25BM/883 AT28C1024-25LM/883	40B 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
40B	40 Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)
44L	44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
W	Die

AT28C1024