

FEATURES

- Monolithic DBS Tuner IC
- On Chip Oscillator
- 6 dB Noise Figure
- 11 dB Conversion Gain
- Single + 5V Supply
- Small Size
- Low Cost
- High Reliability
- Surface Mount Package
- RoHS Compliant package Option



PRODUCT DESCRIPTION

The ANADIGICS DBS (Direct Broadcast Satellite) Tuner IC is intended for use in high volume, low cost manufacturing of compact DBS tuners for satellite receivers and integrated satellite ready TV/VTR receivers.

manufacturers the ability to produce, in high volumes, tuners with low component count, minimal tuning, small size, high reliability and exceptional price-performance ratios. The ADC20013 offers a high degree of functionality in a very small and user friendly configuration.

The ADC20013 Tuner IC provides DBS tuner

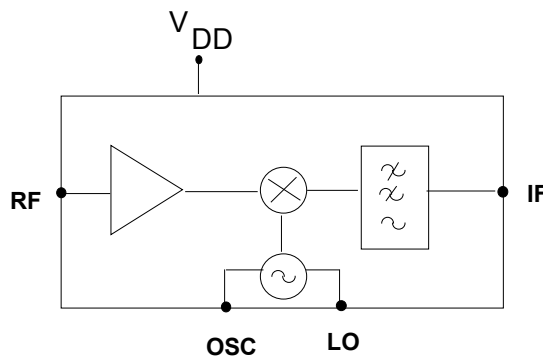


Figure 1: Functional Block Diagram

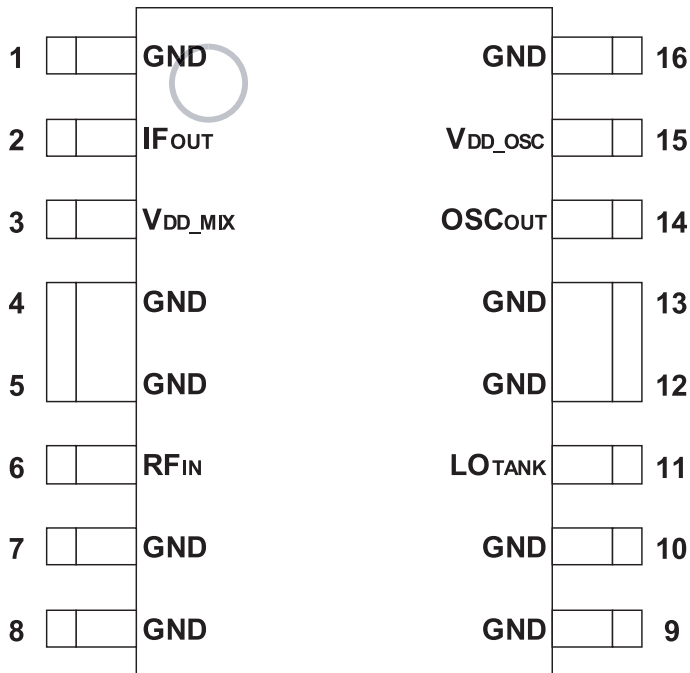


Figure 2: Pinout

Table 1: Pin Description

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	GND	Ground	16	GND	Ground
2	IF _{OUT}	IF Output	15	V _{DD_OSC}	Oscillator Supply
3	V _{DD_MIX}	Mixer Supply	14	OSC _{OUT}	Oscillator Output to PLL
4	GND	Ground	13	GND	Ground
5	GND	Ground	12	GND	Ground
6	RF _{IN}	RF Input	11	LO _{TANK}	LO Tank Circuit
7	GND	Ground	10	GND	Ground
8	GND	Ground	9	GND	Ground

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
V_{DD}/V_{IF}	0	+7	VDC
V_{LO}	-5	+0.5	VDC
V_{RF}	-10	+0.5	VDC
V_{OSC}	-5	+0.5	VDC
Storage Temperature	-55	+100	°C
Input Power RF		+10	dBm
Input Power LO		+17	dBm

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT	
Frequency	RF	950	-	2050	MHz
	LO	1430	-	2530	MHz
	IF	-	480	-	MHz
V_{DD}	-	+5	-	VDC	
Case Temperature	-55	-	+85	°C	

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Table 4: Electrical Specifications

 $(T_A = 25\text{ }^\circ\text{C}; V_{DD} = +5\text{V})$

PARAMETER	MIN	TYP	MAX	UNIT
Conversion Gain ⁽⁶⁾	6	11	-	dB
SSB Noise Figure ⁽⁶⁾	-	6.5	11	dB
Third Order IMD ⁽⁴⁾ (-20 dBm Tones, 5 MHz Apart)	-	- 40	-35	dBc
Second Order IMD (-20 dBm Input Level)	-	- 25	- 20	dBc
LO Leakage ^{(1),(2)} RF Port	-	- 30	- 25	dBm
IF Port	-	0	3	dBm
LO Output Level for PLL ⁽³⁾	-8	- 4	-	dBm
Tuning Voltage ⁽¹⁾ (VT)	1	-	20	Volts
VCO Phase Noise ⁽⁵⁾ 10 kHz Offset	-	- 70	- 65	dBc/Hz
100 kHz Offset	-	- 100	- 95	dBc/Hz
Input Impedance ⁽⁷⁾	-	-	-	-
Output Impedance ⁽⁷⁾	-	-	-	-
Power Supply Current	-	60	85	mA

Notes:

(1) Measured in ANADIGICS test fixture with Toshiba 1SV186 off-chip-varactor.

(2) Includes external coupling through test fixture.

(3) Oscillator output for external PLL. (Pin 14)

(4) Measured at 1450 and 1750 MHz.

(5) Measured using PLL (LBW = 1 KHz, Reference = 1.25 MHz, Step Size = 10 MHz).

(6) Measured in ANADIGICS test setup.

(7) See Smith charts.

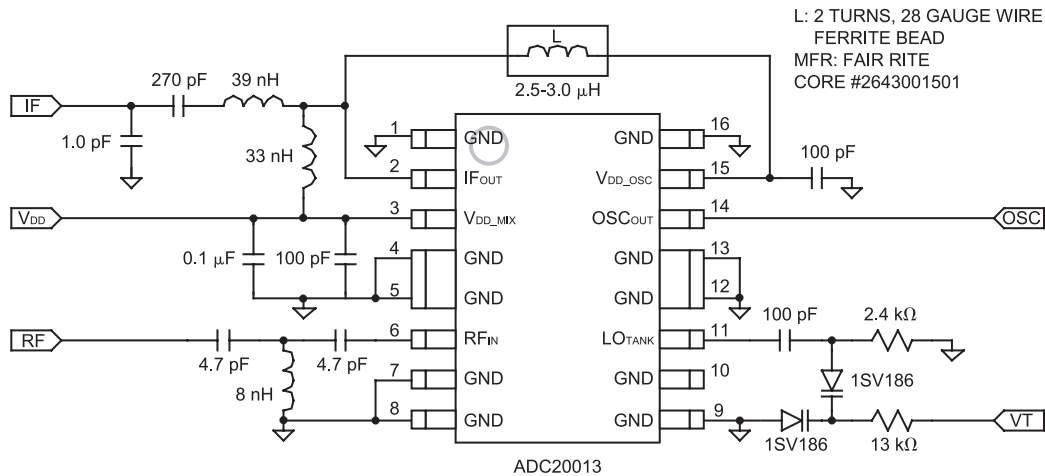


Figure 3: Test Circuit

PERFORMANCE DATA

Figure 4: Conversion Gain and Noise Figure vs Frequency

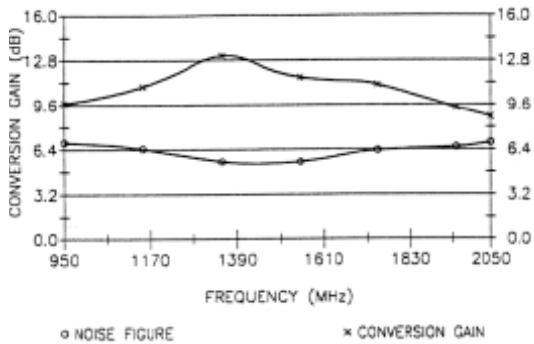


Figure 5: Oscillator Tuning Curve

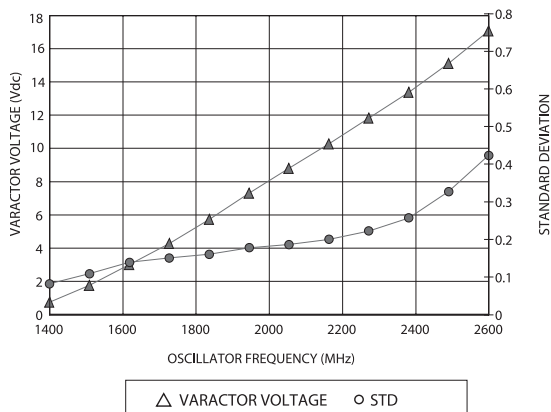


Figure 6: Third Order IMD
RF Input Power Level -20dBm/Tone

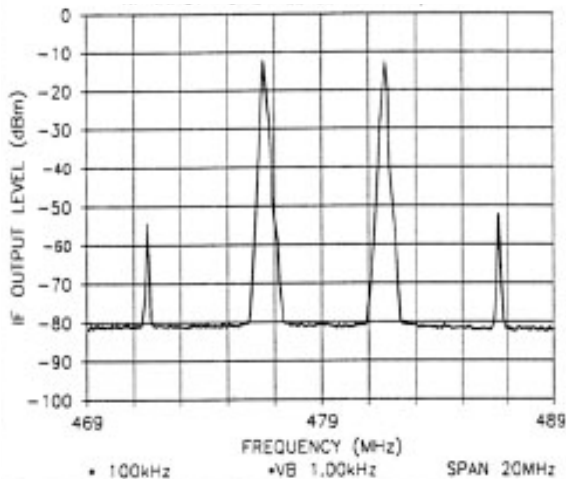
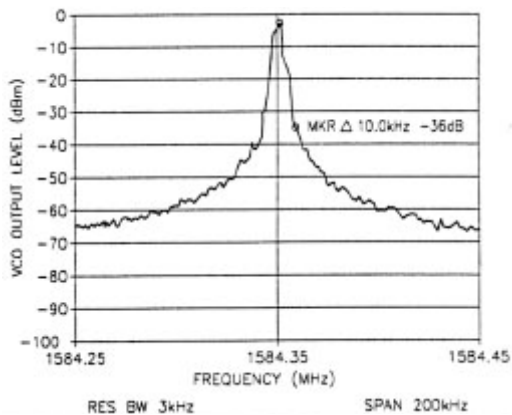
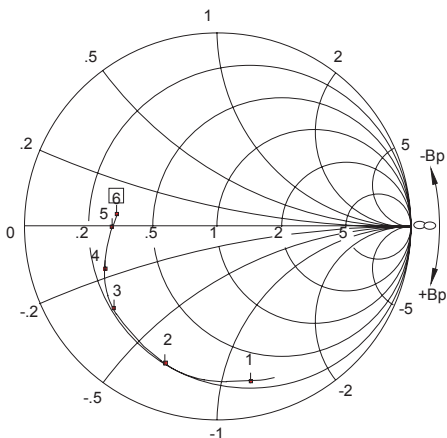


Figure 7: VCO Phase Noise



INPUT IMPEDANCE DATA (RF)

1. IMPEDANCE REFERENCE AT PIN 6
2. VCO ON $V_t = 3.20$ VOLTS
3. $V_{dd} = +5$ VOLTS
4. USE EXTERNAL BIAS TEE FOR IF



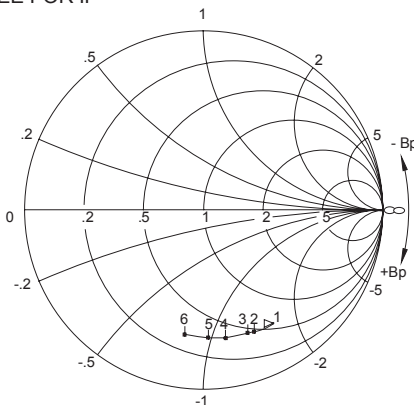
1	0.950 GHz	8.40	-61.53 j
2	1.250 GHz	8.12	-34.53 j
3	1.550 GHz	10.13	-19.90 j
4	1.750 GHz	12.75	-8.70 j
5	1.900 GHz	15.23	-3.03 j
6	2.050 GHz	16.33	-0.27 j

MEASURED IN 50 SYSTEM

Figure 8: Input Impedance Data (RF)

OUTPUT IMPEDANCE DATA (IF)

1. IMPEDANCE REFERENCE AT PIN 2
2. VCO ON $V_t = 3.20$ VOLTS
3. $V_{dd} = +5$ VOLTS
4. USE EXTERNAL BIAS TEE FOR IF

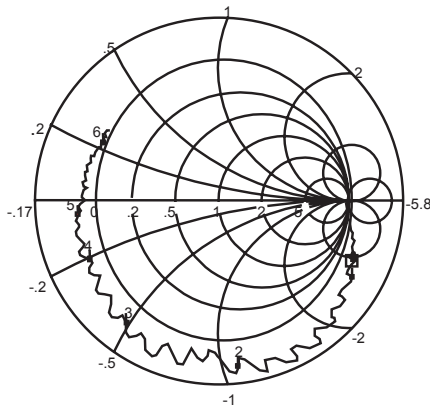


1	0.40 GHz	26.8	-82.8 j
2	0.48 GHz	22.2	-70.0 j
3	0.50 GHz	21.4	-67.5 j
4	0.60 GHz	18.1	-56.2 j
5	0.70 GHz	15.9	-48.7 j
6	0.80 GHz	14	-41.2 j

MEASURED IN 50 SYSTEM

Figure 9: Output Impedance Data (IF)

1. IMPEDANCE REFERENCE AT PIN 11
2. V_{dd} = + 5 VOLTS



- | | | | |
|---|------------|---------|------------|
| 1 | 1500.0 MHz | - 60.83 | - 169.80 j |
| 2 | 1000.0 MHz | -15.15 | -54.41 j |
| 3 | 1430.0 MHz | - 5.71 | - 24.62 j |
| 4 | 1700.0 MHz | - 2.80 | - 12.02 j |
| 5 | 1922.0 MHz | - 2.83 | - 4.25 j |
| 6 | 2768.0 MHz | 0.54 | -11.31 j |

MEASURED IN 50 SYSTEM

Figure 10: LO Impedance Data

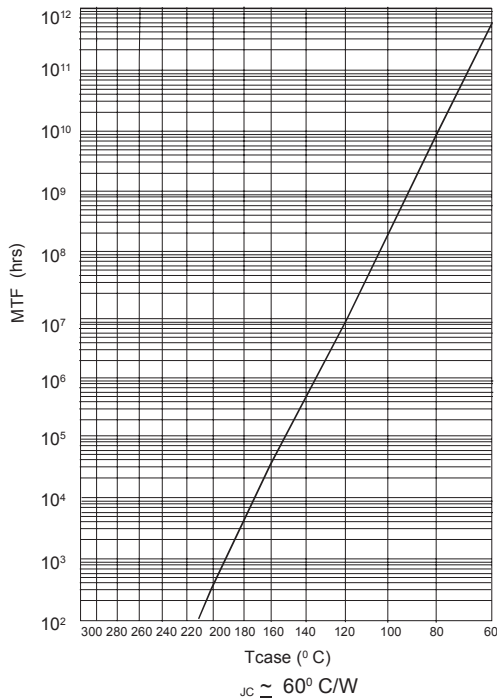
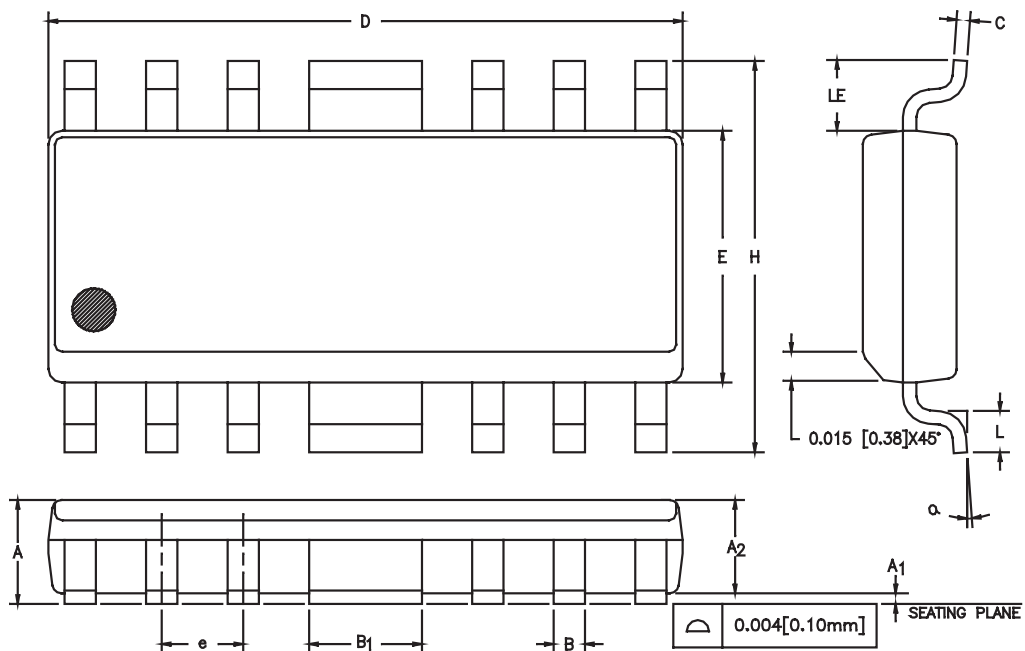


Figure 11: MTF vs. Tcase

PACKAGE OUTLINE



Symbol	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.058	0.068	1.47	1.73	
A1	0.004	0.010	0.10	0.25	
A2	0.055	0.065	1.40	1.65	
B	0.013	0.020	0.33	0.50	
B1	0.062	0.070	1.58	1.78	
C	0.008	0.010	0.20	0.25	4
D	0.380	0.400	9.66	10.16	2
E	0.150	0.160	3.81	4.06	3
e	0.050	BSC	1.27	BSC	
H	0.226	0.244	5.74	6.20	
L	0.016	0.040	0.41	1.02	
LE	0.030	—	0.76	—	
α	0°	8°	0°	8°	

NOTES:

1. CONTROLLING DIMENSION: INCHES
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 [0.15mm] PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.010 [0.25mm] PER SIDE.
4. MAXIMUM LEAD TWIST/SKEW TO BE ± 0.005 [0.13mm].
5. LEAD THICKNESS AFTER PLATING TO BE 0.013 [0.33mm] MAXIMUM.

Figure 12: S3 Package Outline - Modified 16 Pin SOIC

NOTES

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
ADC20013S3CTR	-55 °C to +85 °C	Modified 16 Pin SOIC	Tape and Reel, 3500 pieces per Reel
ADC20013RS3P1	-55 °C to +85 °C	RoHS Compliant Modified 16 Pin SOIC	Tape and Reel, 3500 pieces per Reel

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WARNING

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