

High Performance 512x4 PROM Ti-W PROM Family

53/63S240 53/63S241 53/63S241A

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Features/Benefits

- 35 ns maximum access time
- Reliable titanium-tungsten fuses (Ti-W) guarantees greater than 98% programming yields
- Low-voltage generic programming
- Pin-compatible with standard Schottky PROMs
- PNP inputs for low input current
- Open collector and three-state outputs

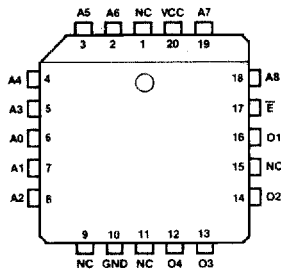
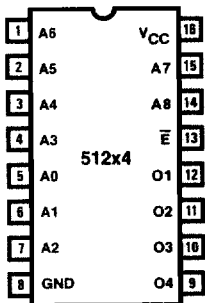
Applications

- Microprogram control store
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable logic element (PLE™) with 9 inputs, 4 outputs, 512 product terms per output

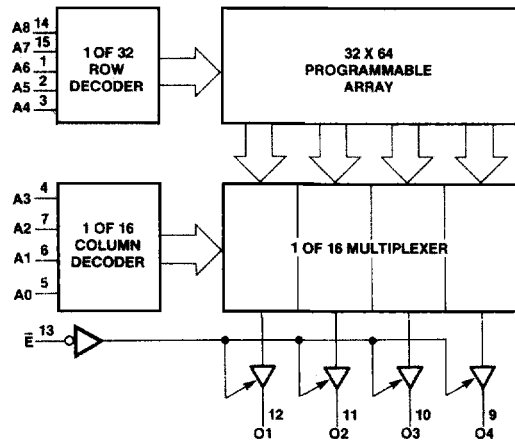
Selection Guide

MEMORY		PACKAGE		OUTPUT	PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	PINS	TYPE			0°C to +75°C	-55°C to +125°C
2 K	512x4	16 (20)	N,J, (NL), (L),(W)	TS	Enhanced	63S241A	53S241A
				OC	Standard	63S240	53S240

Pin Configurations



Block Diagram



PLE™ is a trademark of Monolithic Memories.

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Monolithic Memories

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Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Input current	-30 mA to +5 mA	
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP†	MAX	UNIT		
V_{IL}	Low-level input voltage					0.8	V		
V_{IH}	High-level input voltage					2	V		
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}$	$I_I = -18 \text{ mA}$			-1.5	V		
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4 \text{ V}$			-0.25	mA		
I_{IH}	High-level input current	$V_{CC} = \text{MAX}$	$V_I = V_{CC} \text{ MAX}$			40	μA		
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 16 \text{ mA}$	COM		0.45	V		
				MIL		0.5			
V_{OH}	High-level output voltage*	$V_{CC} = \text{MIN}$	COM $I_{OH} = -3.2 \text{ mA}$	2.4			V		
			MIL $I_{OH} = -2 \text{ mA}$						
I_{OZL}	Off-state output current*	$V_{CC} = \text{MAX}$	$V_O = 0.4 \text{ V}$			-40	μA		
I_{OZH}			$V_O = 2.4 \text{ V}$			40			
I_{CEX}	Open collector output current	$V_{CC} = \text{MAX}$	$V_O = 2.4 \text{ V}$			40	μA		
			$V_O = 5.5 \text{ V}$			100			
I_{OS}	Output short-circuit current**	$V_{CC} = 5 \text{ V}$	$V_O = 0 \text{ V}$			-20	-90	mA	
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, all inputs grounded, all outputs open.					80	130	mA

Switching Characteristics Over Operating Conditions (See standard test load)

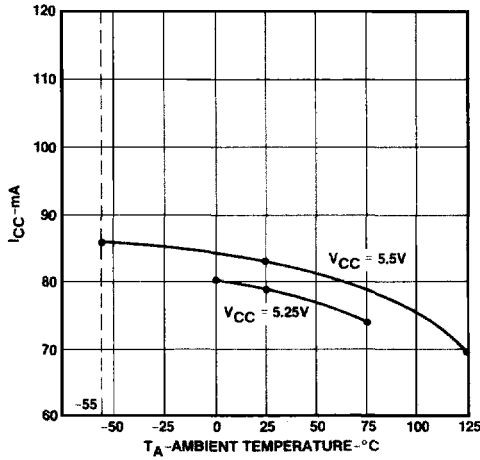
OPERATING CONDITIONS	DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME		t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME		UNIT
		TYP†	MAX	TYP†	MAX	
		COMMERCIAL	63S241A	25	35	
	63S240, 63S241	25	45	12	25	
MILITARY	53S241A	25	45	12	25	
	53S240, 53S241	25	55	12	30	

* Three-state only.

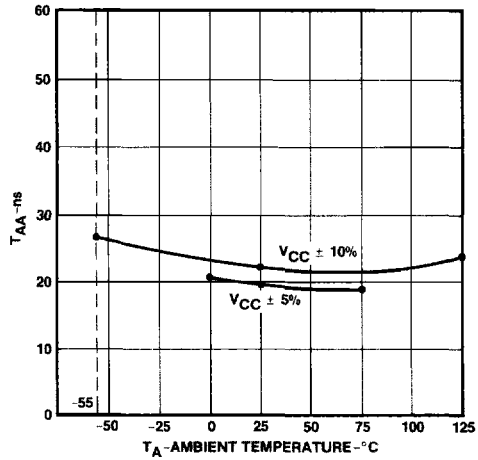
** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typical at 5.0 V V_{CC} and 25° C T_A .

Typical I_{CC} vs Temperature

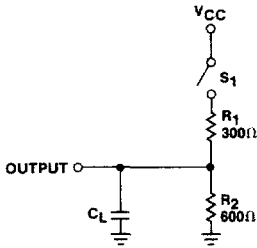


Typical T_{AA} vs Temperature



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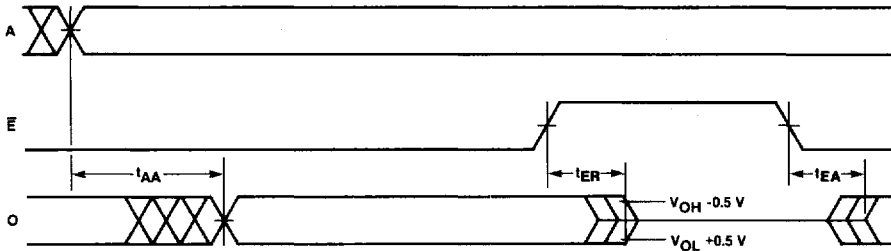
Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE	NOT APPLICABLE

Definition of Waveforms



- NOTES:
1. Input pulse amplitude 0 V to 3.0 V.
 2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
 3. Input access measured at the 1.5 V level.
 4. t_{AA} is tested with switch S_1 closed. $C_L = 30$ pF and measured at 1.5 V output level.
 5. For open collector devices, TEA and TER are measured at the 1.5 V output level with S_1 closed and $C_L = 30$ pF.
 6. For three-state devices, TEA is measured at the 1.5 V output level with $C_L = 30$ pF. S_1 is open for high-impedance to "1" test and closed for high-impedance to "0" test.
TER is tested with $C_L = 5$ pF. S_1 is open for "1" to high-impedance test, measured at $V_{OH} - 0.5$ output level, S_1 is closed for "0" to high-impedance test measured at $V_{OL} + 0.5$ output level.

Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 98%. If your programming yield is lower, check your programmer. It may not be properly calibrated.

Programming is final manufacturing — it must be quality-controlled. Equipment must be calibrated as a regular routine,

ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember — The best PROMs available can be made unreliable by improper programming techniques.

PROM PROGRAMMING EQUIPMENT INFORMATION

SOURCE AND LOCATION

Data I/O Corp.
10525 Willows Rd. N.E.
Redmond, WA 98052

Kontron Electronics, Inc.
630 Price Ave.
Redwood City, CA 94036

Digelec Inc.
7335 E. Acorna Dr.
Suite 103
Scottsdale, AZ 85260

Stag Systems Inc.
1120 San Antonio Rd.
Palo Alto, CA 94303

Metal Mask Layout

