FEATURES

- **Interfaces Directly with an 8 Bit Microprocessor**
- **Wide Application Range**
- **Reduced Number of Counter ICs**
- **Reduced Parts Count**
- **40 Pin Plastic Dual Inline Package**
- **60 Pin Quad Flat Package**
- **+ 5 V Single Power Supply**
- **32 Bit Command Counter**
- **24 Bit Error Counter**
- **Adjustable Output Rate to the D/A**
- **10 MHz Clock**

APPLICATIONS

- **Motion Control Systems**
- **Robotics**
- **Drawing Machines**
- **Electrical Discharge Machines**
- **Special Machinery**

See KM3702AD/AQ Operation Manual for further detail.

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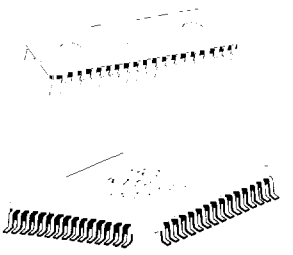
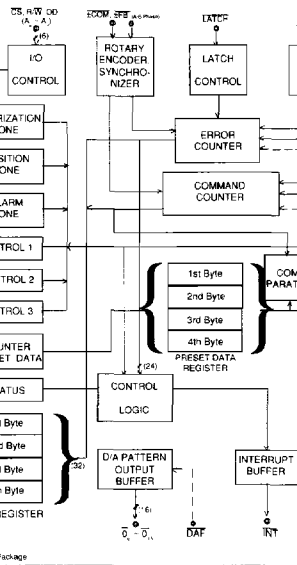
KM3702A



DESCRIPTION

The KM3702AD/AQ is a position control CMOS LSI which monitors the difference between the COMMAND (±COM) and FEEDBACK (±FB) pulses, under the conditions set by the CPU, and uses this position error to output a bit pattern to the D/A converter. The KM3702AD/AQ uses a single +5V power supply and has TTL-compatible input and output. Its system clock (CP) frequency is 10 MHz maximum. To keep track of the input pulses, there are two binary up/down counters: COMMAND COUNTER - 32 bits, cumulative value of +COM and -COM input pulses, and ERROR COUNTER - 24 bits, difference between +COM and -COM input and +FB and -FB input pulses. ±COM and ±FB pulses can be input either synchronously or asynchronously. Data can be preset into these counters, and the counter values can be read out by the host CPU. Commands from the CPU can be used to create a zero clamp condition or a floating state condition on the outputs to the D/A converter. Zero clamp means that for the purposes of the D/A converter, the output pattern will be zero even though the ERROR COUNTER continues to function normally.

BLOCK DIAGRAM



ORDERING INFORMATION

KM3702A □ □ □□

- Tape/Reel Code
- Temp. Range
- Package Code

PACKAGE CODE	TEMP. RANGE	TAPE/REEL CODE
D: Plastic Dip	C : -20 to +75 °C	BX: Bulk/Bag
Q: QFP		MG: Magazine

ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... V_{SS} -0.3 to V_{DD} +0.3 V
Supply Voltage ..... V_{SS} -0.3 to V_{DD} +7.0 V
Power Dissipation (KM3702AD) ..... 1.25 W
Power Dissipation (KM3702AQ) ..... 1.00 W

Storage Temperature Range ..... -65 to +150 °C
Operating Temperature Range ..... -20 to +75 °C
Lead Soldering Temp. (10 sec.) ..... 300 °C

ELECTRICAL CHARACTERISTICS

D. C. CHARACTERISTICS

Test conditions: V_{SS} = 0 V, T_A = -20 to +75 °C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage		4.75	5.0	5.25	V
I_{DD}	Supply Current				5.0	mA
Input Signal 1 (Note 1)						
V_{IL}	Low Level Input Voltage		0.0		0.6	V
V_{IH}	High Level Input Voltage		3.0		V_{DD}	V
I_{LEAK}	Input Leak Current				±10	µA
Output Signal 2 (Note 2)						
I_{IL}	Low Level Input Current	V_{IL} = 0 V	-200		-10	µA
I_{IH}	High Level Input Current	$V_{IH} = V_{DD}$			±10	µA
Output Signal 3 (Note 3)						
V_{OL1}	Low Level Output Voltage	I_{OL1} = 2.0 mA			0.4	V
V_{OH1}	High Level Output Voltage	I_{OH1} = -200 µA	2.4			V
Output Signal 4 (Note 4)						
V_{OL2}	Low Level Output Voltage	I_{OL2} = 5.0 mA			0.4	V
V_{OH2}	High Level Output Voltage	I_{OH2} = -500 µA	2.4			V
I_{OFF2}	High Impedance Output Voltage				±10	µA

Note 1: $\overline{CS}$, R/$\overline{W}$, OD, A_2, A_1, A_0, $\overline{LATCH}$, +$\overline{COM}$, -$\overline{COM}$, +FB, -FB, $\overline{RESET}$, CP
Note 2: D_7, D_6, D_5, D_4, D_3, D_2, D_1, D_0, $\overline{CHR}$, $\overline{EHR}$, $\overline{DAF}$
Note 3: $\overline{INT}$, CCMP
Note 4: D_7, D_6, D_5, D_4, D_3, D_2, D_1, D_0
Note 5: 0_{15}, 0_{14}, 0_{13}, 0_{12}, 0_{11}, 0_{10}, 0_9, 0_8, 0_7, 0_6, 0_5, 0_4, 0_3, 0_2, 0_1, 0_0,

ELECTRICAL CHARACTERISTICS (CONT.)

A. C. CHARACTERISTICS

Test conditions: V_{DD} = 5 V + 5%, T_A = -20 to +75 °C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Signal 5 (Note 5)						
V_{OL3}	Low Level Output Voltage	I_{OL3} = 2.0 mA			0.4	V
V_{OH3}	High Level Output Voltage	I_{OH3} = -200 µA	2.4			V
I_{OFF3}	High Impedance Output Voltage				±10	µA
CLOCKED SIGNAL 1 (Note 2)						
T_{CYC}	Clock Pulse Period		0.1		10	µS
T_W	Clock Pulse Width		30		T_{CYC} -30	ns
T_{CR}	Clock Pulse Rise Time				30	ns
T_{CF}	Clock Pulse Fall Time				30	ns
INPUT SIGNAL 2 (Note 3)						
T_H	Data Hold Time For Input		10			ns
T_{SU}	Data Set Up Time For Input		T_W + 20			ns
t_{DAF}	DAF To OUTPUT (-5)				50	ns
OUTPUT SIGNAL 3 (Note 4)						
T_{D1}	Output Delay Time 1	C_L = 60 pF			25	ns
T_{D0}	Output Delay Time 2	C_L = 60 pF			50	ns
CPU INTERFACE 4 (Note 5)						
t_A	Access Time	C_L = 100 pF			120	ns
T_{CO}	CS To Output	C_L = 100 pF			100	ns
T_{OD}	OD To Output	C_L = 100 pF			100	ns
T_{OW}	Width Of OD		120			ns
T_{RDH}	Data Hold Time After OD		0			ns

Note 2: $\overline{CS}$, R/$\overline{W}$, $\overline{OD}$, A_2, A_1, A_0, LATCH, +COM, -COM, +FB, -FB, $\overline{RESET}$, CP

Note 3: D_7, D_6, D_5, D_4, D_3, D_2, D_1, D_0, $\overline{CHR}$, $\overline{EHR}$, $\overline{DAF}$

Note 4: $\overline{INT}$, CCMP

Note 5: D_7, D_6, D_5, D_4, D_3, D_2, D_1, D_0

Note 6: 0_{15}, 0_{14}, 0_{13}, 0_{12}, 0_{11}, 0_{10}, 0_9, 0_8, 0_7, 0_6, 0_5, 0_4, 0_3, 0_2, 0_1, 0_0,

ELECTRICAL CHARACTERISTICS (CONT.)

A. C. CHARACTERISTICS

Test conditions: V_{DD} = 5 V + 5%, T_A = -20 to +75 °C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CPU INTERFACE 4 (Note 5)						
t_{CA}	Address Valid After CONTROL		0			ns
t_{AC}	Address Valid Before CONTROL		40			ns
t_{CH}	CS Hold After CONTROL		0			ns
t_{CSC}	CS Valid Before Control		0			ns
t_{CW}	CS To WRITE		100			ns
t_{CC}	Width of R/W		100			ns
t_{WDS}	Data Set Up Time		120			ns
t_{WDH}	Data Hold Time After R/W		0			ns

Note 5: D_7, D_6, D_5, D_4, D_3, D_2, D_1, D_0

PIN FUNCTION (KM3702AD)

SIGNAL	SYMBOL	PIN NO.	I/O	DESCRIPTION
Power Supply	V_{DD}	40	--	+5V ± 5%
Ground	V_{SS}	20	--	Ground
Chip Select	$\overline{CS}$	1	I	Device select signal
Write	R/W	2	I	Write control signal
Output Disable	OD	3	I	Output disable signal
Address	A_2~A_0	4~6	I	Address select signal
Data	D_7~D_0	7~14	I/O	Read/Write data I/O common 3-state I/O
Error Counter Latch	LATCH	15	I	If more than 3 clock pulses then, ERROR COUNTER value are transferred to the DATA REGISTER.
+Command	+COM	16	I	+Command pulse
-Command	-COM	17	I	-Command pulse
+Feedback	+FB	18	I	+Feedback pulse
-Feedback	-FB	19	I	-Feedback pulse
Reset	$\overline{RESET}$	21	I	Reset signal
Clock Pulse	CP	22	I	System clock
Interrupt	$\overline{INT}$	23	O	CPU interrupt signal
Output for D/A Converter	0_0~0_{15}	24~39	O	Output pattern for D/A converter 3-state output

PIN FUNCTION (KM3702AQ)

NAME	SYMBOL	PIN NO.	I/O	DESCRIPTION
Power Supply	V_{DD}	23, 53	–	+5 V ± 5%
Power Supply	V_{SS}	2,8,31,38,46	–	GND
Chip Select	CS	49	I	Device Slect Signal
Write	R/W	50	I	Write Signal
Output Disable	OD	51	I	Read Signal
Address	A_2- A_6	55 TO 57	I	Address Signal
Data	D_7 to D_6	1, 3 to 6, 58 to 60	I/O	Read/Write Data, I/O Common 3 State I/O
Error Counter Latch	LATCH	11	I	If more than 3 clock pulses than, Error Counter Value are transferred to the data register
+ Command	+ COM	18	I	+ Command Pulse
- Command	- COM	10	I	- Command Pulse
+ Feedback	+FB	20	I	+ Feedback Pulse
- Feedback	-FB	21	I	- Feedback Pulse
Reset	RESET	10	I	Reset Signal
Clock Pulse	CP	9	I	Basic Clock
Interrupt	INT	48	O	CPU Interrupt Error Counter
Output for D/A Converter	0_8 to 0_{15}	25 to 30, 32 to 37, 40 to 43	O	D/A Converter Output
Command Counter Reset	CHR	12	I	Command Counter Reset Signal
Error Counter Reset	EHR	13	I	Error Counter Reset Signal
D/A Converter for Output Floating	DAF	22	I	D/A Converter Output Floating
Command Counter Comparator Output	CCMP	47	O	Command Counter Data Over Preset Data Signal

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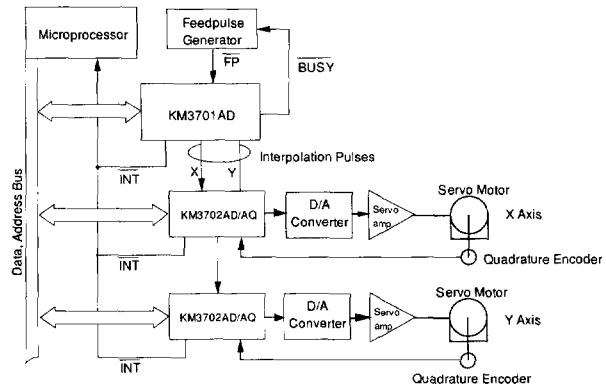
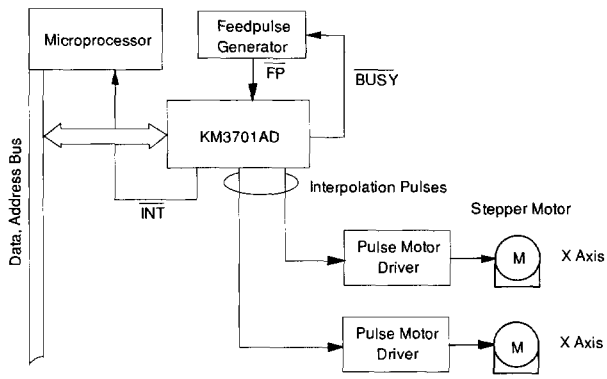
APPLICATIONS

1. Control of 2 axes can be accomplished by using one KM3701AD and two KM3702AD/AQs.



1. One KM3701AD can control two stepper motors.



INTERPOLATION

The interpolation pulse distribution rate is in accordance with the rate of the clock pulse (CP) and the internal calculation time. The internal calculation requires 11 clocks in the case of linear interpolation and 21 clocks in the case of circular or other interpolations.

Interpolation	Interpolation Pulse Distribution Rate
Linear interpolation	454.4KPPs
Circular or other	238.1KPPs