Integrated Device Technology, Inc.

LOW POWER 3.3V CMOS FAST SRAM 256K (32K x 8-BIT)

IDT71V256SA

FEATURES

- Ideal for high-performance processor secondary cache
- Fast access times:
  — 10/12/15/20ns
- Low standby current (maximum):
  — 2mA full standby
- Small packages for space-efficient layouts:
  — 28-pin 300 mil SOJ
  — 28-pin 300 mil plastic DIP
  — 28-pin TSOP Type I
- Ideal configuration for large cache sizes, with minimum space and minimum power:
  — 32K x 8
- Produced with advanced high-performance CMOS technology
- Inputs and outputs are LVTTL-compatible
- Single 3.3V(±0.3V) power supply

DESCRIPTION

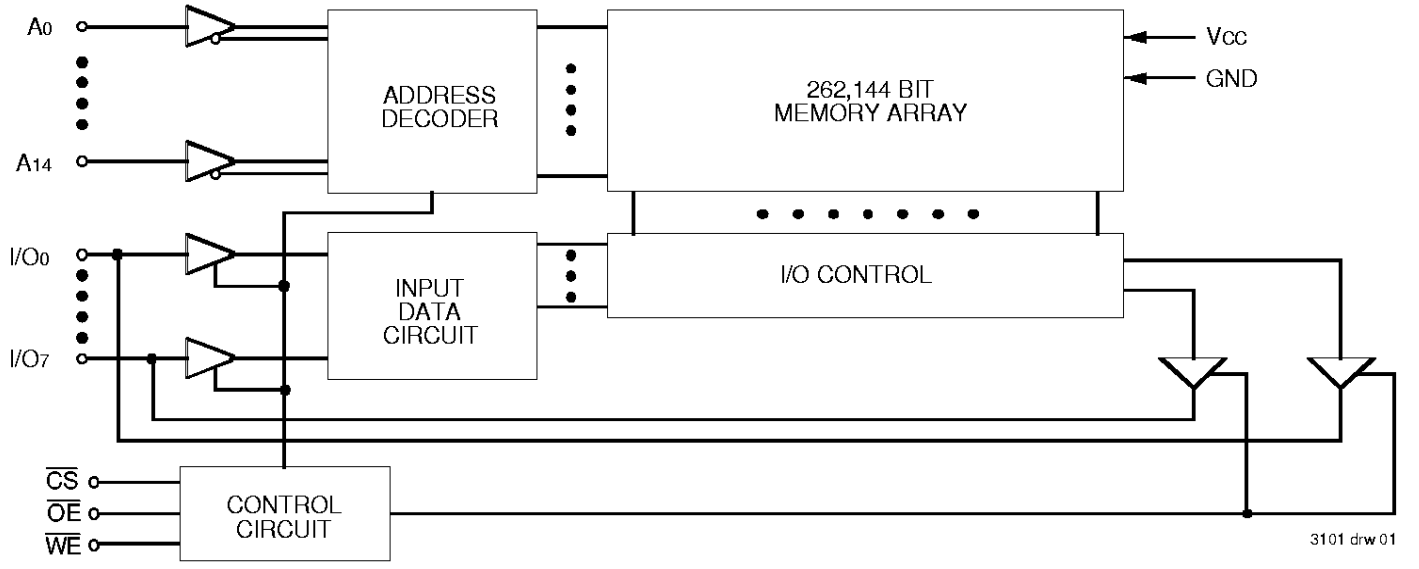
The IDT71V256SA is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

The IDT71V256SA has outstanding low power characteristics while at the same time maintaining very high performance. Address access times of as fast as10 ns are ideal for 3.3V secondary cache in 3.3V desktop designs.

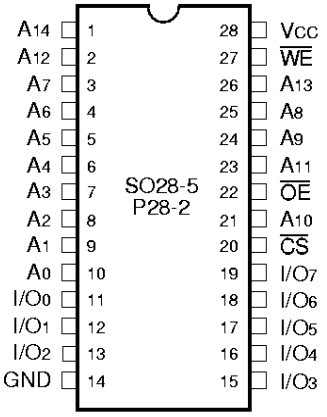
When power management logic puts the IDT71V256SA in standby mode, its very low power characteristics contribute to extended battery life. By taking $\overline{CS}$ HIGH, the SRAM will automatically go to a low power standby mode and will remain in standby as long as $\overline{CS}$ remains HIGH. Furthermore, under full standby mode ($\overline{CS}$ at CMOS level, f=0), power consumption is guaranteed to always be less than 6.6mW and typically will be much smaller.

The IDT71V256SA is packaged in 28-pin 300 mil SOJ, 28-pin 300 mil plastic DIP, and 28-pin 300 mil TSOP Type I packaging.

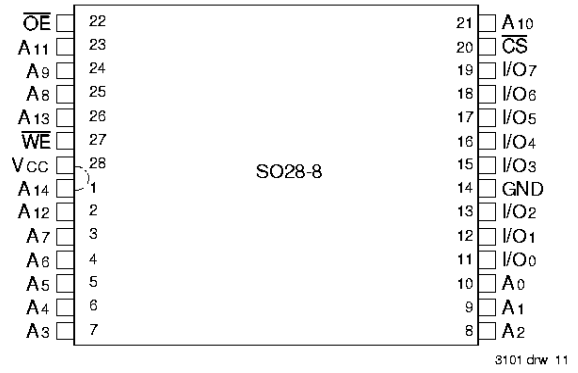
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP/SOJ
TOP VIEW



TSOP
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A_0–A_{14}	Addresses
I/O_0–I/O_7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
Vcc	Power

3101 tbl 01

TRUTH TABLE(1)

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
X	H	X	High-Z	Standby (ISB)
X	V_{HC}	X	High-Z	Standby (ISB1)
H	L	H	High-Z	Output Disable
H	L	L	D_{OUT}	Read
L	L	X	D_{IN}	Write

NOTE: 3101 tbl 02
1. H = V_{IH}, L = V_{IL}, X = Don't Care

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to VCC+0.5	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTES: 3101 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals only.
3. Input, Output, and I/O terminals; 4.6V maximum.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	7	pF

NOTE: 3101 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 0.3V

3101 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage - Inputs	2.0	—	5.0	V
V_{IH}	Input High Voltage - I/O	2.0	—	Vcc+0.3	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 3101 tbl 06
1. V_{IL} (min.) = –1.0V for pulse width less than 5ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS(1, 2)

(V_{CC} = 3.3V ± 0.3V, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	71V256SA10(3) Com'l	71V256SA12 Com'l	71V256SA15 Com'l.	71V256SA20 Com'l.	Unit
I_{CC}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	100	90	85	85	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} = V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}(2)	20	20	20	20	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, V_{CC} = Max., Outputs Open, f = 0(2), $V_{IN} \le V_{LC}$ or $V_{IN} \ge V_{HC}$	2	2	2	2	mA

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC}, only address inputs cycling at fmax; f = 0 means that no inputs are cycling.
3. 10 ns specification is preliminary.

3101 tbl 07

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V± 0.3V

Symbol	Parameter	Test Condition	IDT71V256SA Min.	Typ.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	—	2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS} = V_{IH}$, V_{OUT} = GND to V_{CC}	—	—	2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	—	V

3101 tbl 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3101 tbl 09

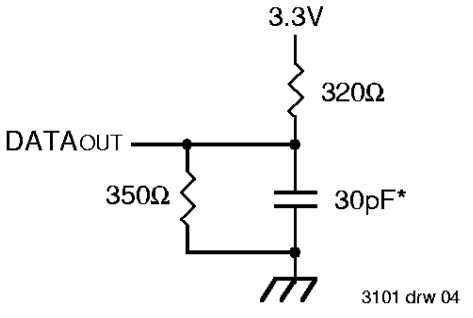


Figure 1. AC Test Load

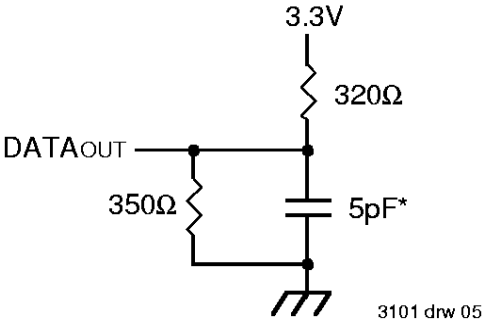


Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

*Includes scope and jig capacitances

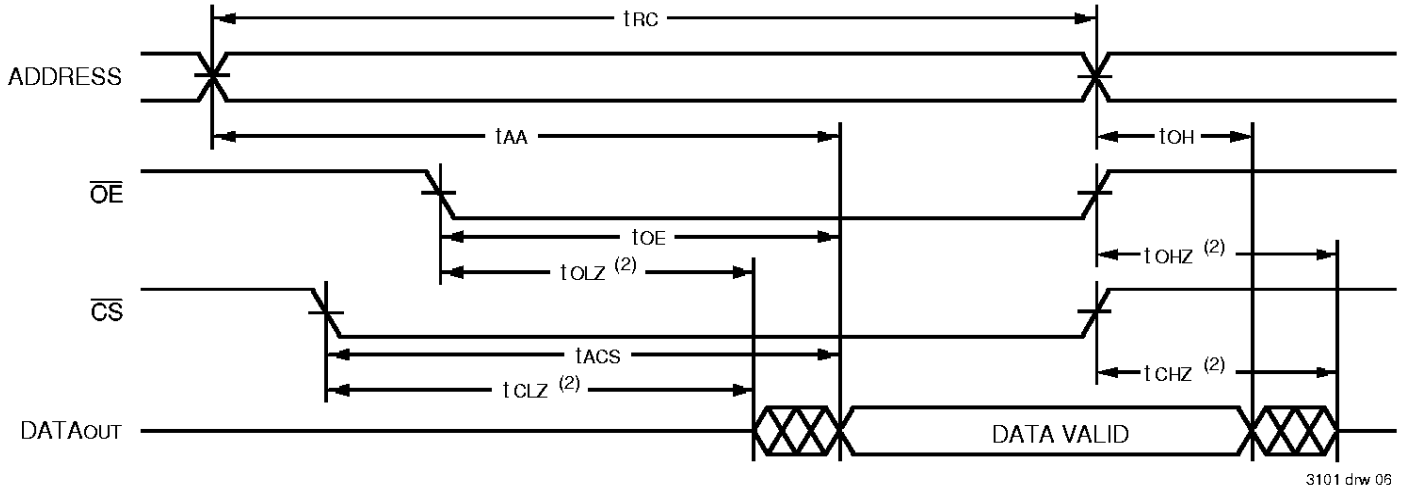
AC ELECTRICAL CHARACTERISTICS (VCC = 3.3V ± 0.3V, Commercial Temperature Range)

Symbol	Parameter	71V256SA10[2]		71V256SA12		71V256SA15		71V256SA20		Unit
		Max.	Min.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRC	Read Cycle Time	10	—	12	—	15	—	20	—	ns
tAA	Address Access Time	—	10	—	12	—	15	—	20	ns
tACS	Chip Select Access Time	—	10	—	12	—	15	—	20	ns
tCLZ[1]	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	ns
tCHZ[1]	Chip Select to Output in High-Z	0	8	0	8	0	9	0	10	ns
tOE	Output Enable to Output Valid	—	6	—	6	—	7	—	8	ns
tOLZ[1]	Output Enable to Output in Low-Z	3	—	3	—	0	—	0	—	ns
tOHZ[1]	Output Disable to Output in High-Z	2	6	2	6	0	7	0	8	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
Write Cycle										
tWC	Write Cycle Time	10	—	12	—	15	—	20	—	ns
tAW	Address Valid to End-of-Write	9	—	9	—	10	—	15	—	ns
tCW	Chip Select to End-of-Write	9	—	9	—	10	—	15	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	9	—	9	—	10	—	15	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	Data to Write Time Overlap	6	—	6	—	7	—	8	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
tOW[1]	Output Active from End-of-Write	4	—	4	—	4	—	4	—	ns
tWHZ[1]	Write Enable to Output in High-Z	1	8	1	8	1	9	1	10	ns

NOTE: 3101 tbl 10

1. This parameter guaranteed with the AC test load (Figure 2) by device characterization, but is not production tested.
2. 10 ns specification is preliminary.

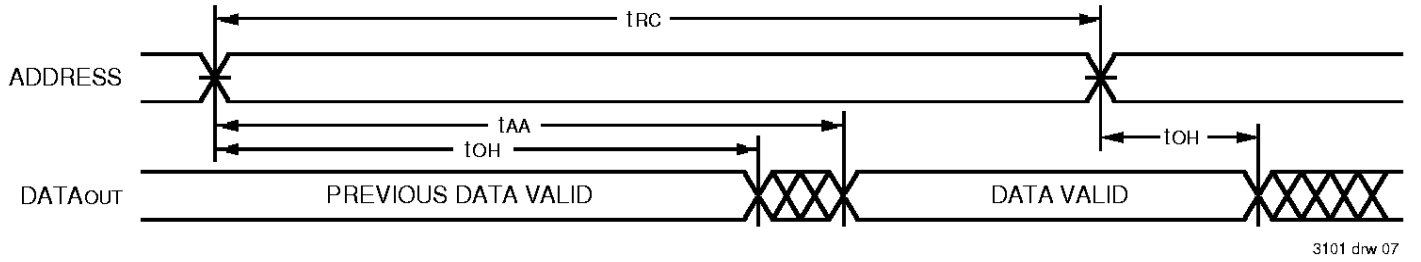
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



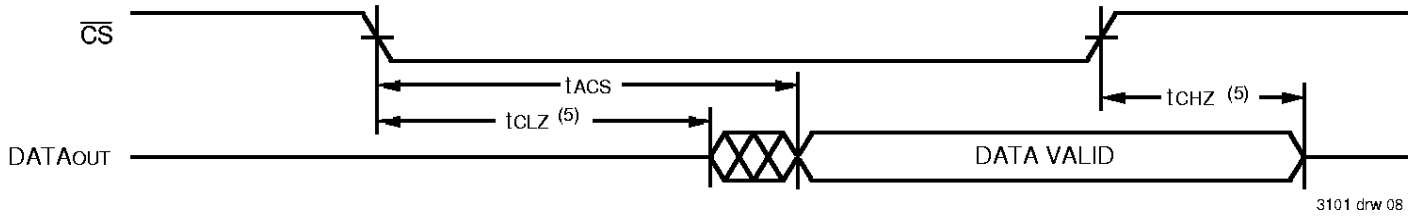
NOTES:

1. $\overline{WE}$ is HIGH for Read cycle.
2. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

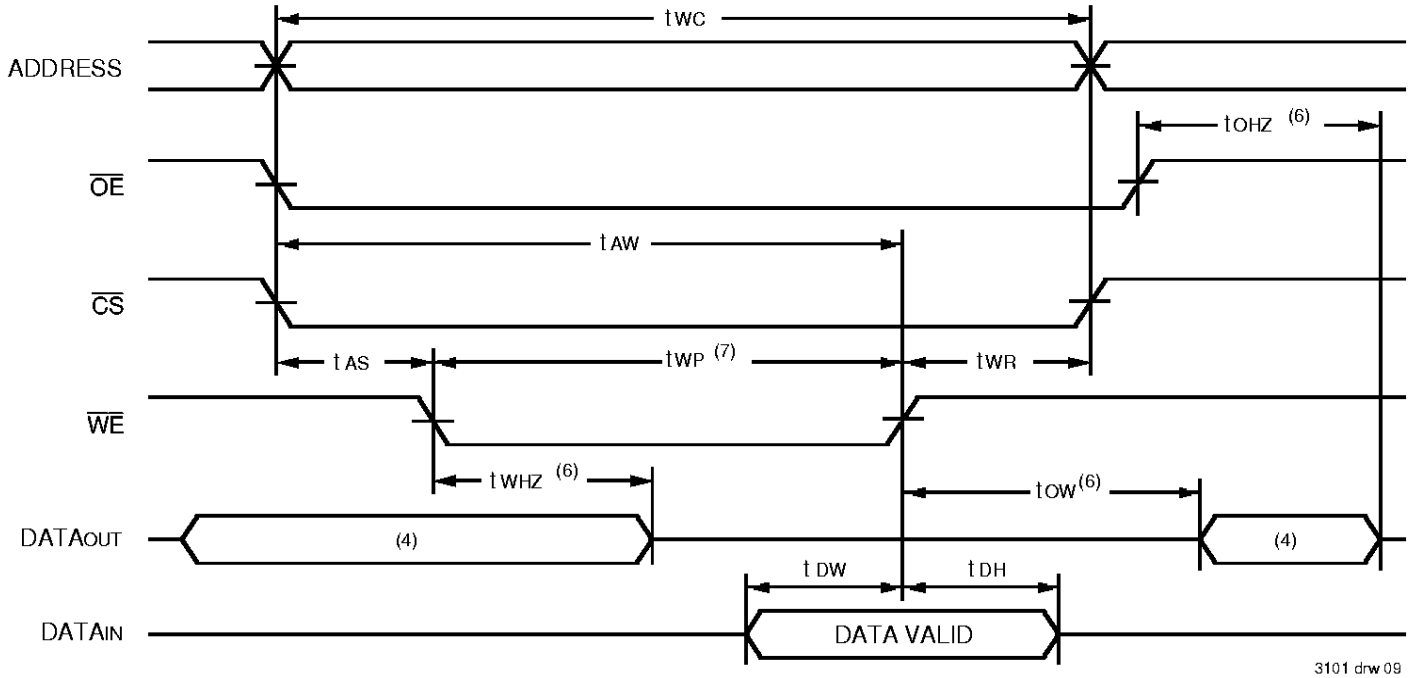


TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



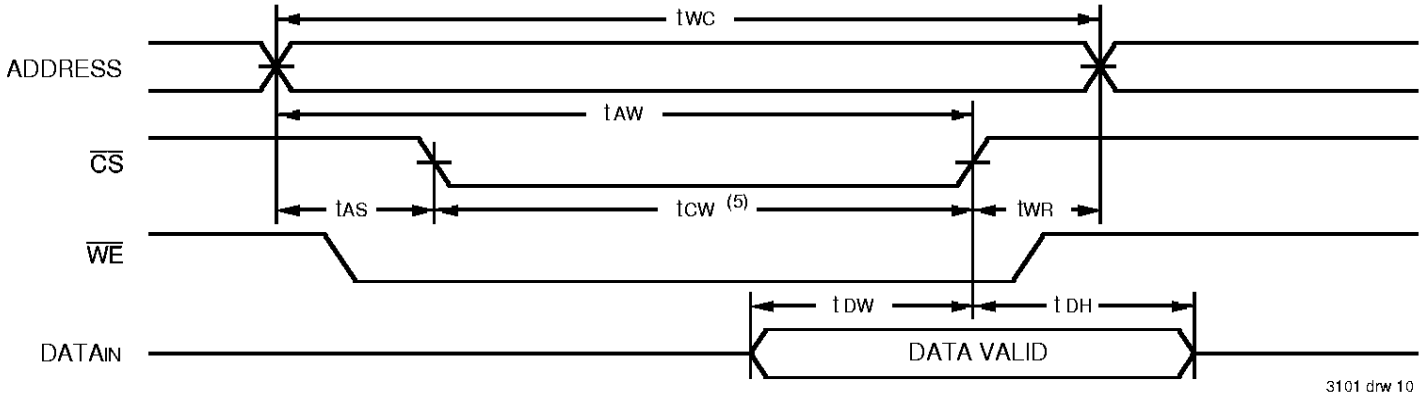
NOTES:
1. $\overline{WE}$ is HIGH for Read cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 5, 7)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 4)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
5. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP

ORDERING INFORMATION