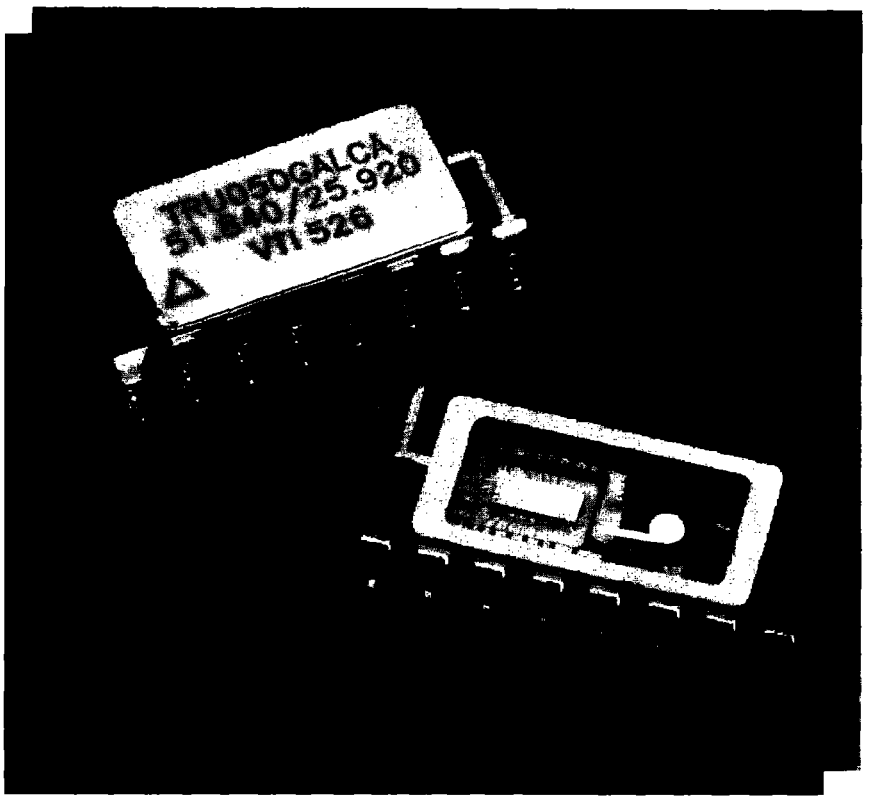
TRU050
Clock Recovery and Data Retiming Module



TRU050 Clock Recovery and Data Retiming Module

Features

- Drop-in frequency translator
- Compact phase-locked loop (PLL) saves board space
- Quartz crystal stabilized by internal VCXO
- User-defined loop filter for tailoring performance
- Input data and clock rates from 50 kb/s to 52 Mb/s
- NRZ data compatible
- Low transition density capability
- Superior jitter performance
- TTL output compatible
- 3-state clock and data output
- Loss of signal indicator
- Clock return to nominal frequency with loss of input data
- Single 5 V positive power supply
- Hermetically sealed, 16-pin, ceramic DIP
- Machine insertable

Description

The TRU050 Clock Recovery and Data Retiming Module is a crystal-stabilized, phase-locked loop design that extracts the clock signal from a digital data stream and regenerates the data. Its jitter performance and ability to recover sparse data patterns are superior to non-crystal-stabilized devices and reduce the need for data encoding. Input data should originate in a device with a crystal-stabilized clock source and be in an NRZ format at TTL or CMOS logic levels. The TRU050 contains a phase detector, operational amplifier, voltage-controlled crystal oscillator, and divider section on a single CMOS silicon chip. This chip and a quartz resonator are housed in a 16-pin, ceramic, dual in-line package. The quartz crystal frequency and divide factor (up to 256) are factory set per customer specification. Loop dynamics are determined by a user-supplied filter. Other applications include frequency translation and clock smoothing.

Pin Information

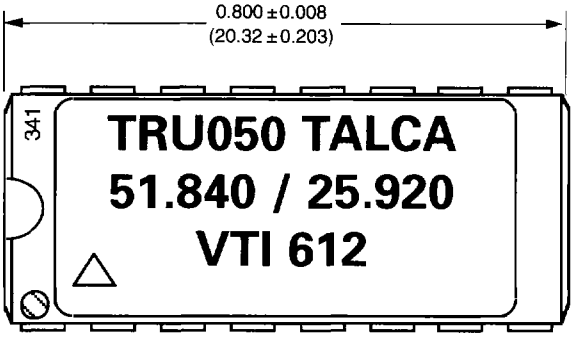


Figure 1. Pin Diagram

Table 1. Pin Descriptions

Note: Please refer to Figures 1 and 5.

Pin	Symbol	Type	Function
1	V_C	I	Control voltage input to internal voltage-controllable crystal oscillator (VCXO).
2	OPN	I	Negative input terminal to internal operational amplifier.
3	OPOUT	O	Output terminal of internal operational amplifier.
4	OPP	I	Positive input terminal to internal operational amplifier.
5	LOSIN	I	With LOSIN set to a logic high, the external input to the VCXO (V_C) is disabled and the VCXO returns to its nominal center frequency. With LOSIN set to logic low, the external input to the VCXO is enabled. The LOSIN input has an internal pull-down resistor.
6	PHO	O	Output signal produced by phase detector and used as V_C at Pin 1.
7	DATAIN	I	Input data stream to phase detector (TTL switching thresholds).
8	GND	I	Circuit and cover ground.
9	CLKIN	I	Input clock signal to phase detector (TTL switching thresholds).
10	LOS	O	Loss of signal indicator is set to a logic high if no transitions are detected at DATAIN after 256 clock cycles. As soon as a transition occurs at DATAIN, LOS is set to a logic low.
11	RCLK	O	TTL compatible recovered clock.
12	RDATA	O	TTL compatible recovered data stream.
13	OUT2	O	Divided version of internal VCXO output clock (TTL).
14	HIZ	I	When set to a logic low, output pins OUT1, OUT2, RCLK, and RDATA buffers are set to high-impedance state. When set to a logic high or no connect, the device functions and output pins OUT1, OUT2, RCLK, and RDATA are active. This input has an internal pull-up resistor.
15	OUT1	O	Output clock of internal VCXO (TTL).
16	V_{DD}	I	5 V ± 10% supply voltage.

Electrical Characteristics (continued)

Table 3. Electrical Specifications

Parameter	Symbol	Min	Max	Unit
Input NRZ Data Rates	DATAIN	0.008	52.0	MHz
Input RZ Data and Clock Rates[1]	DATAIN	0.016	26.0	MHz
Nominal Output Frequency:				
Output 1	OUT1	14.0	52.0	MHz
Output 2[2]	OUT2	0.05	26.0	MHz
Supply Voltage	V_{DD}	4.5	5.5	V
Supply Current (V_{DD} = 4.5 V)	I_{DD}	25	60	mA
Output Voltage Levels (V_{DD} = 4.5 V):				
Output Logic High[3]	V_{OH}	2.5	-	V
Output Logic Low[3]	V_{OL}	-	0.5	V
Transition Times[3]:				
Rise Time (0.5 V to 2.5 V)	t_R	0.5	5	ns
Fall Time (2.5 V to 0.5 V)	t_F	0.5	5	ns
Symmetry or Duty Cycle[4]:				
Output 1	SYM1	40	60	%
Output 2	SYM2	45	55	%
Recovered Clock	R_{CLK}	40	60	%
Input Data:				
Input Logic High[3]	V_{IH}	2.0	-	V
Input Logic Low[3]	V_{IL}	-	0.8	V
Control Voltage Bandwidth (-3 dB, V_C = 2.50 V)	BW	50	-	kHz
Sensitivity @ $V_C = V_O$	$\Delta F/\Delta V_C$	See Figure 4.		ppm/V
Loss of Signal Indication[5]:	L_{OS}			
Output Logic High[3]	V_{OH}	2.5	-	V
Output Logic Low[3]	V_{OL}	-	0.5	V
Nominal Output Frequency on Loss of Signal:				
Output 1	OUT1	-75 ppm	75 ppm	ppm from fo1
Output 2	OUT2	-75 ppm	75 ppm	ppm from fo2
Phase Detector Gain	K_D	-0.53 x Data Density		rad/V

1. For input RZ data, Manchester encoded data, and input clock recovery applications, the output clock must run at two times the input rate to ensure that the input is clocked correctly. Since the output clock has a maximum frequency of 52.0 MHz, these inputs are limited to a maximum rate of 26 MHz.
2. OUT2 is a binary submultiple of OUT1, as specified in the device code shown in Figure 6. OUT2 may also be disabled.
3. Figure 2 defines these parameters. Figure 3 illustrates the equivalent five-gate MTTL load and operating conditions under which these parameters are specified and tested.
4. Symmetry is the ON TIME/PERIOD in percent with VS = 1.4 V for TTL, per Figure 2.
5. A loss of signal (LOS) indicator is set to a logic high if no transitions are detected at DATAIN after 256 clock cycles. As soon as a transition occurs at DATAIN, LOS is set to a logic low.

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. VTI employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the mode. Although no industry-wide standard has been adopted for the CDM, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained using these circuit parameters.

Table 2. ESD Threshold Voltage

Model	ESD Threshold, Minimum	Unit
Human Body	2000*	V
Charged Device	2000	V

* MIL-STD-883D, Method 3015, Class 1

Electrical Characteristics

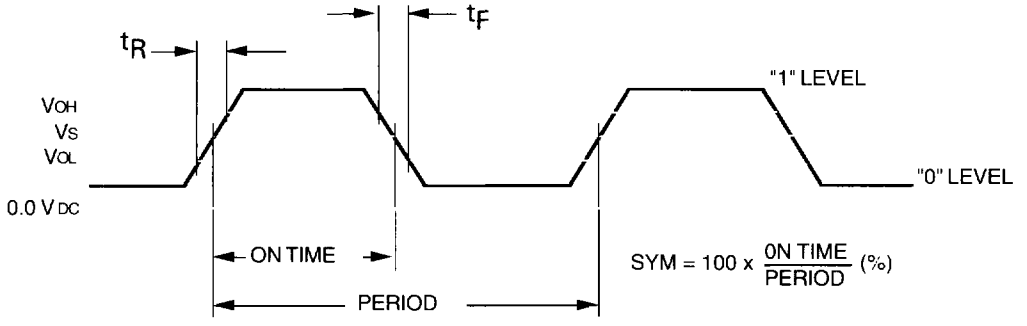
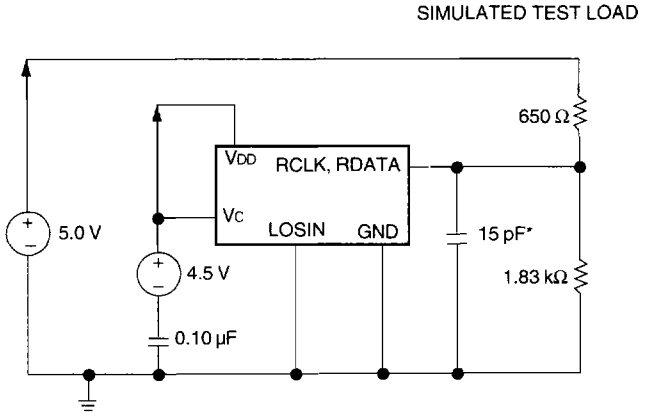


Figure 2. Waveform Parameters



* Includes test fixture capacitance.

Figure 3. Output Test Conditions

Characteristic Curve

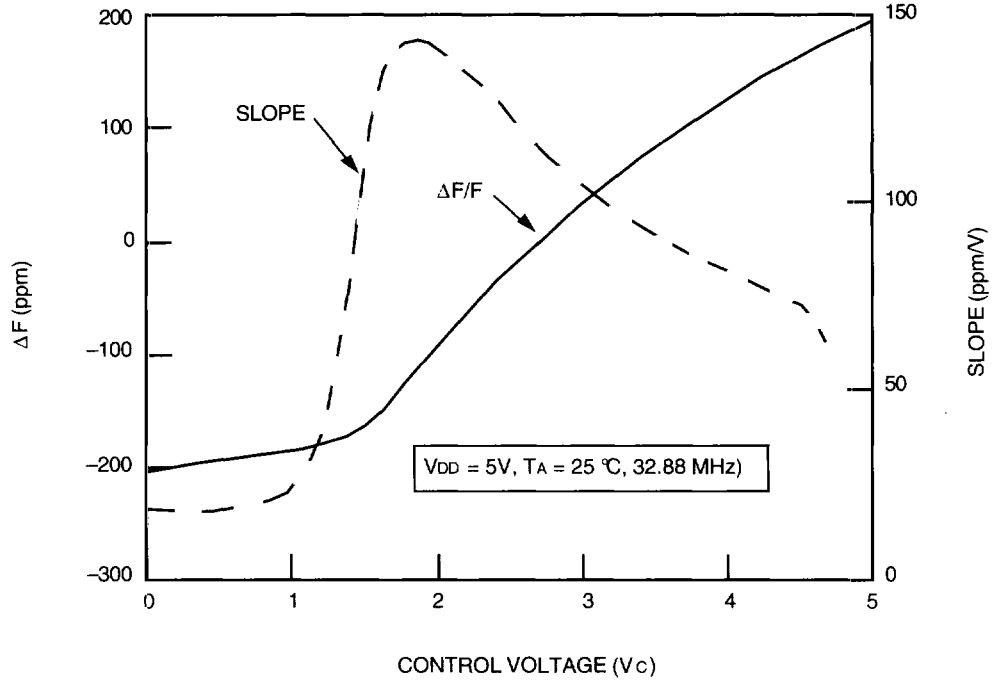


Figure 4. Output Frequency vs. Control Voltage

Absolute Pull Range

Parameter	Symbol	Min	Max	Unit
Absolute Frequency Pull Range	APR	-APR	APR	ppm from F_O

Absolute pull range (APR) is specified by the fourth character of the product code (see Figure 6). The APR is the minimum guaranteed frequency shift from F_0 over variations in temperature, aging, power supply, and load. Both frequency and environment limit the specified APR. **The total pull range for the VCXO contained in the TRU050 is typically between 200 ppm and 400 ppm.**

A 50 ppm APR TRU050 fully tracks a 50 ppm source oscillator or any other 50 ppm reference over the operating temperature range, life of the product, power supply and measurement variations.

Aging

Timing recovery units exhibit a change in output frequency with time. Two dominant mechanisms for this phenomena are change in the stresses on the quartz resonator and mass-loading of the quartz resonator.

Changes in output frequency due to stress are a result of relaxation in the mounting stresses of the quartz resonator or transmittal of environmental stresses through the mounting arrangement. The TRU050 contains a state-of-the-art miniature rectangular AT-Cut resonator (rather than the traditional round resonator) which allows for a mounting arrangement that has very little stress relaxation and isolates the quartz resonator from external stresses.

Mass-loading of the quartz resonator, which generally drives the frequency lower, is a result of an outgassing of materials within a package or a lack of package hermeticity. Higher frequency resonators are more susceptible to this aging mechanism. The TRU050 contains a minimum number of parts internal to the package (a monolithic IC and a quartz resonator) resulting in an internal environment that is well controlled and characterized.

With an application of 40°C and under normal conditions, the oscillator aging is typically 2 ppm the first year, 1 ppm for the second year and continues to logarithmicly decline every year thereafter.

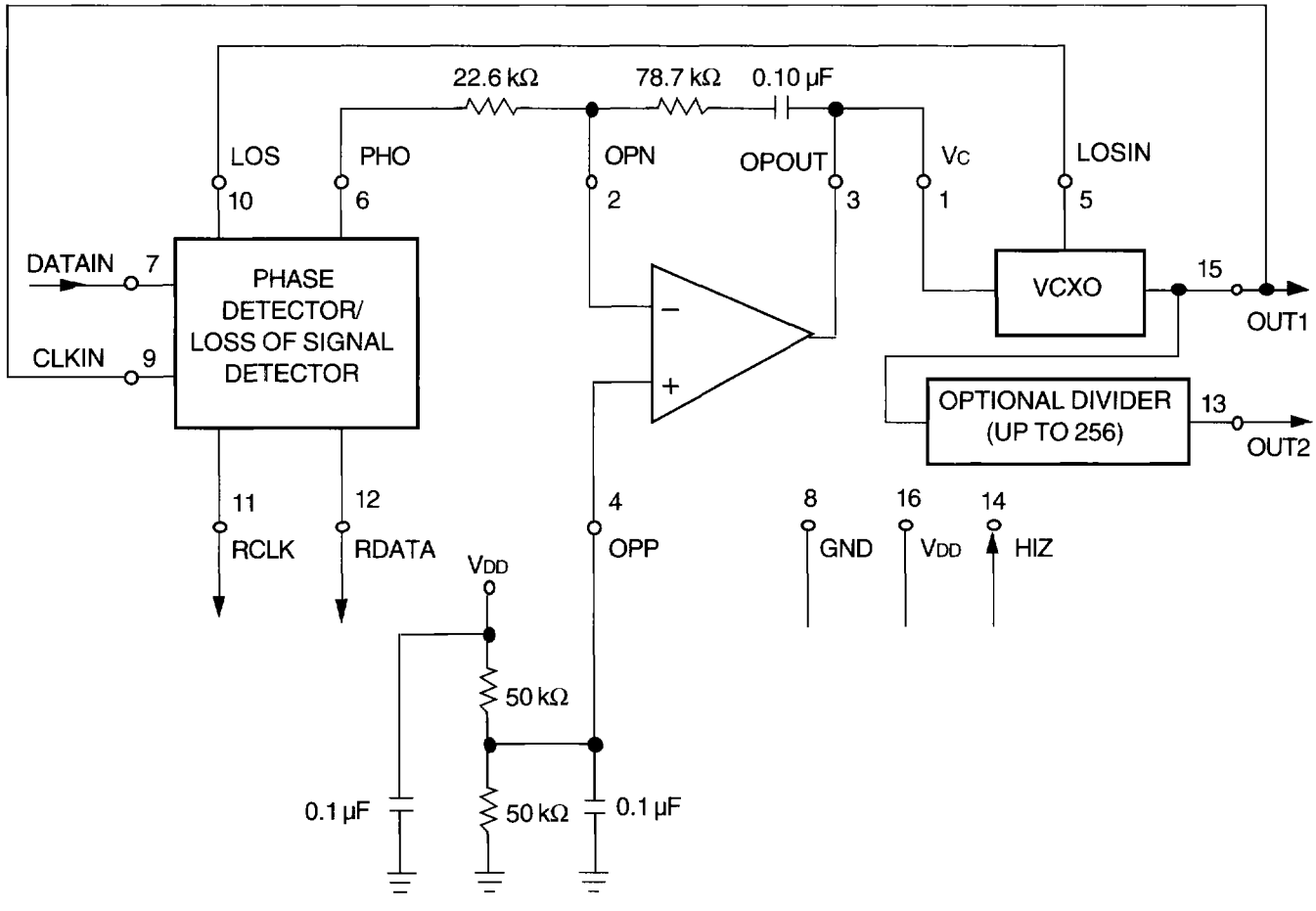
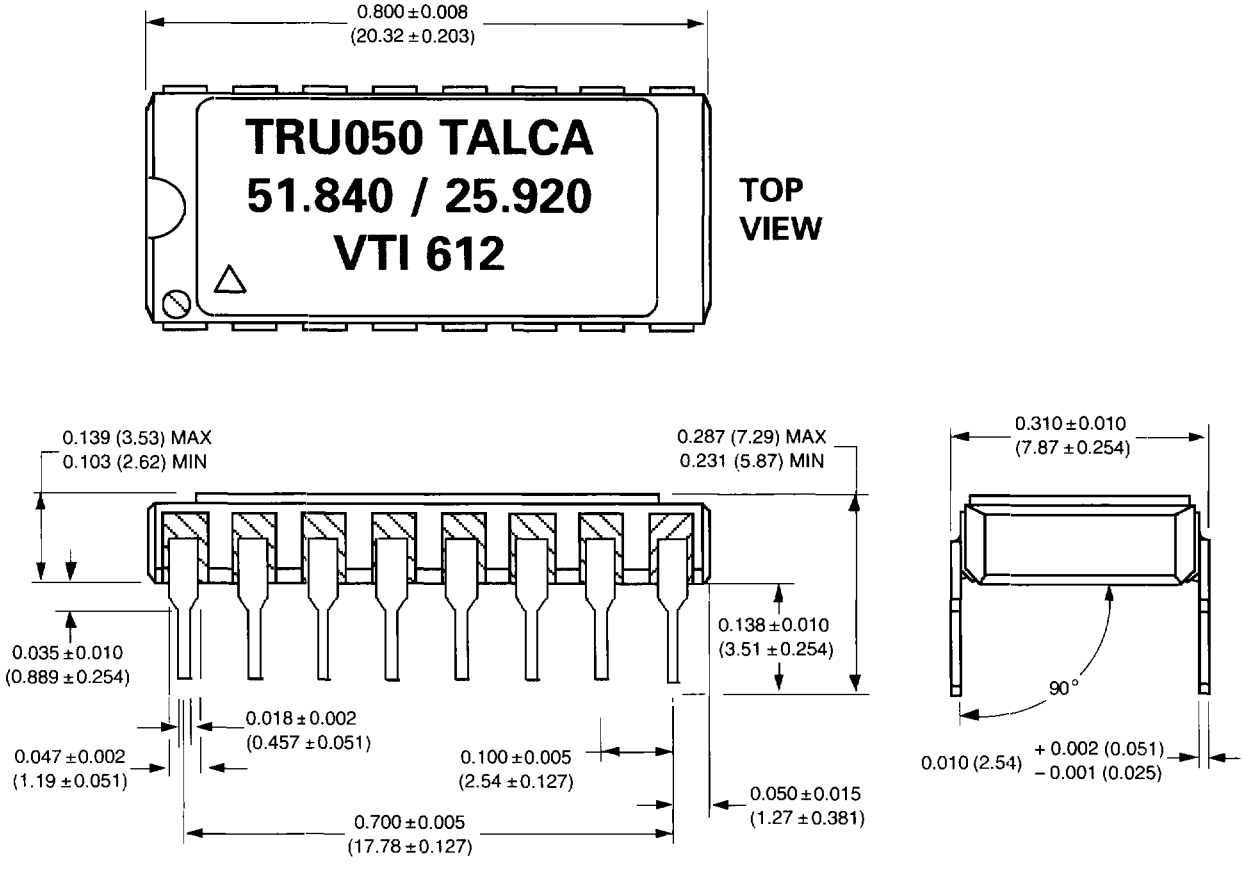


Figure 5. Typical NRZ Data Retiming Application

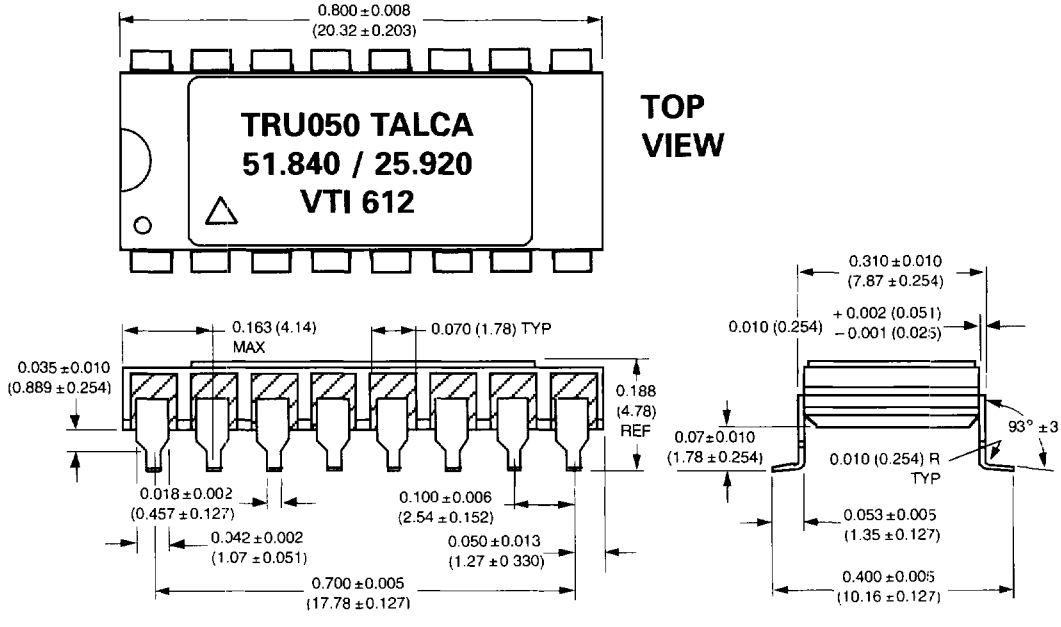
Outline Diagrams

Dimensions are in inches and (millimeters).

TRU050 Thru-Hole Package



TRU050 Gull-Wing Package



Ordering Information

Standard Frequencies* (MHz) Using OUT 1						
12.032	12.288	12.624	13.824	16.000	16.128	16.384
16.777	16.896	17.920	18.432	18.936	20.000	20.480
22.1184	22.579	24.576	24.704	25.000	25.248	28.000
30.720	32.000	32.768	33.330	34.368	38.880	40.000
41.2416	41.943	44.736	47.457	49.152	49.408	50.000
51.840						

Standard Frequencies* (MHz) Using OUT 2						
1.000	1.024	1.544	2.048	3.088	3.240	4.032
4.096	4.1925	4.224	5.592	6.016	6.144	6.312
6.480	6.912	7.680	8.000	8.192	8.448	8.960
9.468	9.720	10.000	10.240	11.0592	12.352	12.500
12.960	14.000	16.000	16.384	16.665	19.440	20.000
20.6208	20.9715	22.368	23.7285	24.576	24.704	25.920

*Other frequencies available upon request.

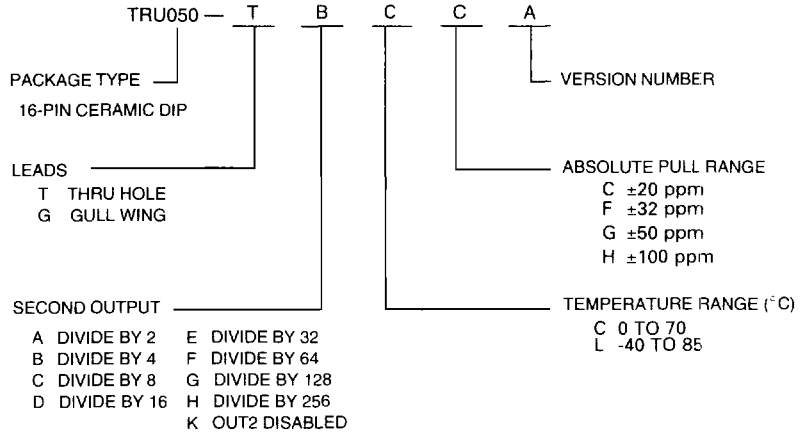


Figure 6. Part Numbering Information