

## 3.3V DRAM Modules

**HYM64Vx005GCD(L)-60**

### 144 pin SO-DIMM EDO-DRAM Modules 8MB , 16MB, 32MB & 64MB density

- 144 Pin JEDEC Standard, 8 Byte Small Outline Dual In-line Memory Modules with 8 Byte busses for PC notebook applications
- Chip-on Board (COB) Assembly Technique
- One bank 1M x 64, 2M x 64, 4M x 64 and 8M x 64 non-parity module organisations
- Performance:

|      |                          | -60    |
|------|--------------------------|--------|
| tRAC | RAS Access Time          | 60 ns  |
| tCAC | CAS Access Time          | 15 ns  |
| tAA  | Access Time from Address | 30 ns  |
| tRC  | Cycle Time               | 104 ns |
| tHPC | EDO Mode Cycle Time      | 25 ns  |

- Single +3.3V( $\pm 0.3V$ ) power supply
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh,  $\overline{\text{RAS}}$ -only-refresh
- L-versions use low power DRAMs and support Self Refresh (sleep mode)
- Decoupling capacitors mounted on substrate
- All inputs, outputs are LVTTTL compatible
- Optional serial presence detect
- Gold contact pad

These SIEMENS modules are industry standard 144-pin 8-byte EDO-DRAM Small Outline Dual In-line Memory Modules (SO-DIMM) which are organised as x 64 high speed memory arrays designed for use in non-parity applications. These SO-DIMMs are assemble in Chip-On-Board (COB) assembly technique. L-versions support low power DRAMs with Self Refresh (sleep mode)

These modules use serial presence detects implemented via a serial E<sup>2</sup>PROM using the two pin I<sup>2</sup>C protocol. This communication protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master and the slave E<sup>2</sup>PROM device. The device address for the E<sup>2</sup>PROM is set to zero at the module. The first 128 bytes are utilized by the SODIMM manufacturer and the second 128 bytes are available to the end user.

All SIEMENS 144-pin SO-DIMMs provide a high performance, flexible 8-byte interface in a 67,5 mm long footprint with 25,4 mm height.

### Product Spectrum:

#### Standard versions:

|         |                  | DRAMs used | Rows | Columns | Refresh | Period |
|---------|------------------|------------|------|---------|---------|--------|
| 1M x 64 | HYM64V1005GCD-60 | 4 1Mx16    | 10   | 10      | 1k      | 16 ms  |
| 2M x 64 | HYM64V2005GCD-60 | 8 2Mx8     | 11   | 10      | 2k      | 32 ms  |
| 4M x 64 | HYM64V4005GCD-60 | 4 4Mx16    | 12   | 10      | 4k      | 64 ms  |
| 8M x 64 | HYM64V8005GCD-60 | 8 8Mx8     | 12   | 11      | 4k      | 64 ms  |

#### Low Power Versions with Self Refresh:

|         |                        | DRAMs used | Rows | Columns | Refresh | Period |
|---------|------------------------|------------|------|---------|---------|--------|
| 1M x 64 | HYM64V1005GC DL-50/-60 | 4 1Mx16    | 10   | 10      | 1k      | 128 ms |
| 2M x 64 | HYM64V2005GC DL-50/-60 | 8 2Mx8     | 11   | 10      | 2k      | 128 ms |
| 4M x 64 | HYM64V4005GC DL-50/-60 | 4 4Mx16    | 12   | 10      | 4k      | 128 ms |
| 8M x 64 | HYM64V8005GC DL-50/-60 | 8 8Mx8     | 12   | 11      | 4k      | 128 ms |

### Card Dimensions:

| Organisation | PCB-Board    | L x H x T [mm]       |
|--------------|--------------|----------------------|
| 1M x 64      | L-DIM-144-C1 | 67.60 x 25.40 x 3.80 |
| 2M x 64      | L-DIM-144-C2 | 67.60 x 25.40 x 3.80 |
| 4M x 64      | L-DIM-144-C3 | 67.60 x 25.40 x 3.80 |
| 8M x 64      | L-DIM-144-C4 | 67.60 x 25.40 x 3.80 |

### Pin Names

|             |                                     |
|-------------|-------------------------------------|
| A0-Ax       | Address Inputs                      |
| DQ0 - DQ63  | Data Inout/Output                   |
| RAS0        | Row Address Strobe                  |
| CAS0 - CAS7 | Column Address Strobe               |
| WE          | Read / Write Input                  |
| OE          | Output Enable                       |
| Vcc         | Power (+3.3 Volt)                   |
| Vss         | Ground                              |
| SCL         | Clock for Presence Detect           |
| SDA         | Serial Data Out for Presence Detect |
| N.C.        | No Connection                       |

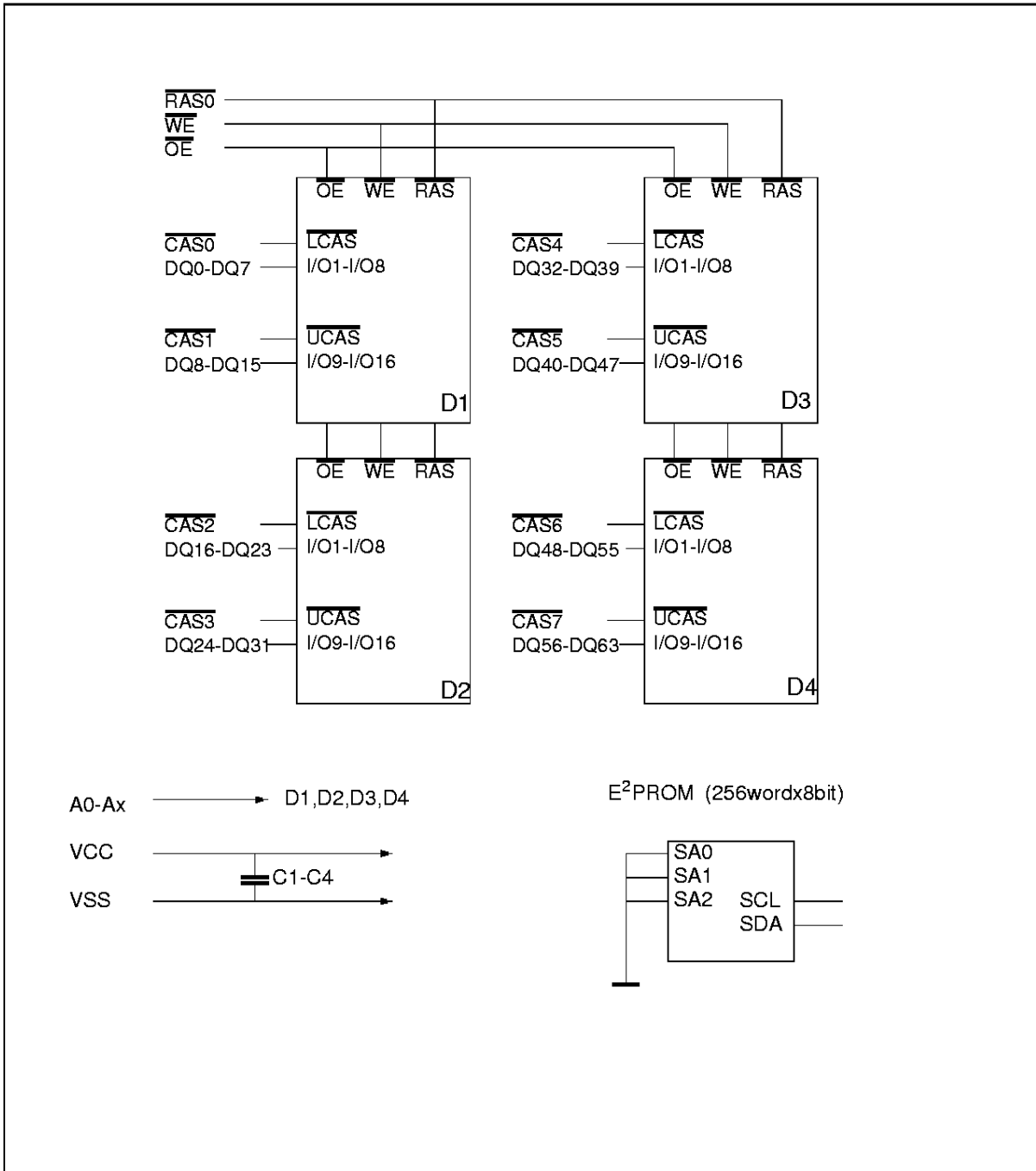
### Capacitance

$T_A = 0$  to  $70$  °C;  $V_{CC} = 3.3$  V  $\pm$  0.3 V;  $f = 1$  MHz

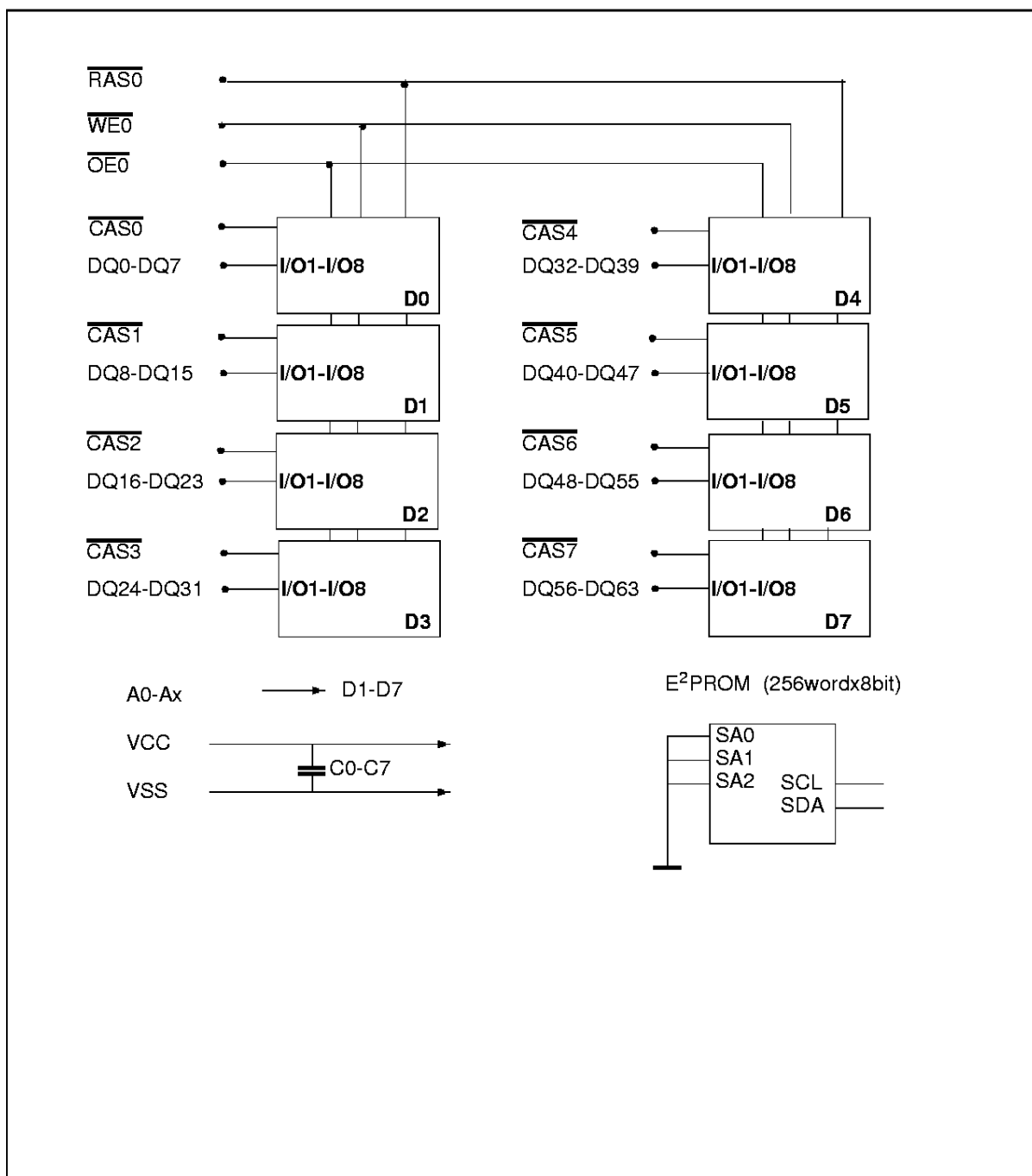
| Parameter                                               | Symbol    | Limit Values |       | Unit |
|---------------------------------------------------------|-----------|--------------|-------|------|
|                                                         |           | 2M x 64      | 4Mx64 |      |
| Input capacitance (Addresses)                           | $C_{I1}$  | 32           | 25    | pF   |
| Input capacitance ( $\overline{RAS0}$ )                 | $C_{I2}$  | 32           | 22    | pF   |
| Input capacitance ( $\overline{CAS0-CAS7}$ )            | $C_{I3}$  | 10           | 8     | pF   |
| Input capacitance ( $\overline{WE}$ , $\overline{OE}$ ) | $C_{I4}$  | 32           | 20    | pF   |
| I/O capacitance (DQ0-DQ63)                              | $C_{IO1}$ | 8            | 9     | pF   |
| Input Capacitance ( $\overline{SCL}$ )                  | $C_{scl}$ | 8            | 8     | pF   |
| Input/Output capacitance (SDA)                          | $C_{sda}$ | 10           | 10    | pF   |

### Pin Configuration

| PIN # | Front Side | PIN # | Back Side |  | PIN # | Front Side | PIN # | Back Side |
|-------|------------|-------|-----------|--|-------|------------|-------|-----------|
| 1     | VSS        | 2     | VSS       |  | 73    | OE         | 74    | NC        |
| 3     | DQ0        | 4     | DQ32      |  | 75    | Vss        | 76    | Vss       |
| 5     | DQ1        | 6     | DQ33      |  | 77    | NC         | 78    | NC        |
| 7     | DQ2        | 8     | DQ34      |  | 79    | NC         | 80    | NC        |
| 9     | DQ3        | 10    | DQ35      |  | 81    | Vcc        | 82    | Vcc       |
| 11    | VCC        | 12    | Vcc       |  | 83    | DQ16       | 84    | DQ48      |
| 13    | DQ4        | 14    | DQ36      |  | 85    | DQ17       | 86    | DQ49      |
| 15    | DQ5        | 16    | DQ37      |  | 87    | DQ18       | 88    | DQ50      |
| 17    | DQ6        | 18    | DQ38      |  | 89    | DQ19       | 90    | DQ51      |
| 19    | DQ7        | 20    | DQ39      |  | 91    | Vss        | 92    | Vss       |
| 21    | Vss        | 22    | Vss       |  | 93    | DQ20       | 94    | DQ52      |
| 23    | CAS0       | 24    | CAS4      |  | 95    | DQ21       | 96    | DQ53      |
| 25    | CAS1       | 26    | CAS5      |  | 97    | DQ22       | 98    | DQ54      |
| 27    | Vcc        | 28    | Vcc       |  | 99    | DQ23       | 100   | DQ55      |
| 29    | A0         | 30    | A3        |  | 101   | Vcc        | 102   | Vcc       |
| 31    | A1         | 32    | A4        |  | 103   | A6         | 104   | A7        |
| 33    | A2         | 34    | A5        |  | 105   | A8         | 106   | A11       |
| 35    | Vss        | 36    | Vss       |  | 107   | Vss        | 108   | Vss       |
| 37    | DQ8        | 38    | DQ40      |  | 109   | A9         | 110   | (A12)     |
| 39    | DQ9        | 40    | DQ41      |  | 111   | A10        | 112   | (A13)     |
| 41    | DQ10       | 42    | DQ42      |  | 113   | Vcc        | 114   | Vcc       |
| 43    | DQ11       | 44    | DQ43      |  | 115   | CAS2       | 116   | CAS6      |
| 45    | Vcc        | 46    | Vcc       |  | 117   | CAS3       | 118   | CAS7      |
| 47    | DQ12       | 48    | DQ44      |  | 119   | Vss        | 120   | Vss       |
| 49    | DQ13       | 50    | DQ45      |  | 121   | DQ24       | 122   | DQ56      |
| 51    | DQ14       | 52    | DQ46      |  | 123   | DQ25       | 124   | DQ57      |
| 53    | DQ15       | 54    | DQ47      |  | 125   | DQ26       | 126   | DQ58      |
| 55    | Vss        | 56    | Vss       |  | 127   | DQ27       | 128   | DQ59      |
| 57    | NC         | 58    | NC        |  | 129   | Vcc        | 130   | Vcc       |
| 59    | NC         | 60    | NC        |  | 131   | DQ28       | 132   | DQ60      |
| 61    | DU         | 62    | DU        |  | 133   | DQ29       | 134   | DQ61      |
| 63    | Vcc        | 64    | Vcc       |  | 135   | DQ30       | 136   | DQ62      |
| 65    | DU         | 66    | DU        |  | 137   | DQ31       | 138   | DQ63      |
| 67    | WE         | 68    | NC        |  | 139   | Vss        | 140   | Vss       |
| 69    | RAS0       | 70    | NC        |  | 141   | SDA        | 142   | SCL       |
| 71    | NC         | 72    | NC        |  | 143   | Vcc        | 144   | Vcc       |



**Block Diagram for 1M x 64 and 4M x 64 SODIMM modules**



Block Diagram for 2M x 64 and 8M x 64 SODIMM modules

### TRUTH TABLE

| FUNCTION                                                         |           | $\overline{\text{RAS}}$ | $\overline{\text{CAS}}$ | $\overline{\text{WRITE}}$ | $\overline{\text{OE}}$ | ROW ADDR | COL ADDR | DQ0-DQ63          |
|------------------------------------------------------------------|-----------|-------------------------|-------------------------|---------------------------|------------------------|----------|----------|-------------------|
| Standby                                                          |           | H                       | X                       | X                         | X                      | X        | X        | High Impedance    |
| Read                                                             |           | L                       | L                       | H                         | L                      | ROW      | COL      | Data Out          |
| Early-Write                                                      |           | L                       | L                       | L                         | X                      | ROW      | COL      | Data In           |
| Late-Write                                                       |           | L                       | L                       | H - L                     | H                      | ROW      | COL      | Data In           |
| Read-Modify-Write (RMW)                                          |           | L                       | L                       | H - L                     | L - H                  | ROW      | COL      | Data Out, Data In |
| EDO Page Mode Read                                               | 1st Cycle | L                       | H - L                   | H                         | L                      | ROW      | COL      | Data Out          |
|                                                                  | 2nd Cycle | L                       | H - L                   | H                         | L                      | n/a      | COL      | Data Out          |
| EDO Page Mode Write                                              | 1st Cycle | L                       | H - L                   | L                         | X                      | ROW      | COL      | Data In           |
|                                                                  | 2nd Cycle | L                       | H - L                   | L                         | X                      | n/a      | COL      | Data In           |
| EDO Page Mode RMW                                                | 1st Cycle | L                       | H - L                   | H - L                     | L - H                  | ROW      | COL      | Data Out, Data In |
|                                                                  | 2st Cycle | L                       | H - L                   | H - L                     | L - H                  | n/a      | COL      | Data Out, Data In |
| $\overline{\text{RAS}}$ only refresh                             |           | L                       | H                       | X                         | X                      | ROW      | n/a      | High Impedance    |
| $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh |           | H - L                   | L                       | H                         | X                      | X        | n/a      | High Impedance    |
| Hidden Refresh                                                   | READ      | L-H-L                   | L                       | H                         | L                      | ROW      | COL      | Data Out          |
|                                                                  | WRITE     | L-H-L                   | L                       | L                         | X                      | ROW      | COL      | Data In           |
| Self Refresh                                                     |           | H - L                   | L                       | H                         | X                      | X        | X        | High Impedance    |

### Absolute Maximum Ratings

|                                        |                                           |
|----------------------------------------|-------------------------------------------|
| Operating temperature range .....      | 0 to + 70 °C                              |
| Storage temperature range .....        | - 55 to + 125 °C                          |
| Input/output voltage .....             | -0.5 to min (V <sub>CC</sub> +0.5, 4.6) V |
| Power supply voltage .....             | -0.5 to 4.6 V                             |
| Power dissipation .....                | 3.68 W                                    |
| Data out current (short circuit) ..... | 50 mA                                     |

**Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### DC Characteristics

$T_A = 0$  to  $70$  °C,  $V_{SS} = 0$  V,  $V_{CC} = 3.3$  V  $\pm$  0.3 V

| Parameter                                                                                            | Symbol     | Limit Values         |                      | Unit | Note |
|------------------------------------------------------------------------------------------------------|------------|----------------------|----------------------|------|------|
|                                                                                                      |            | min.                 | max.                 |      |      |
| Input high voltage                                                                                   | $V_{IH}$   | 2.0                  | V <sub>CC</sub> +0.3 | V    | 1)   |
| Input low voltage                                                                                    | $V_{IL}$   | - 0.3                | 0.8                  | V    | 1)   |
| Output high voltage (LVTTL)<br>Output $\bar{H}$ -level voltage (I <sub>out</sub> = -2mA)             | $V_{OH}$   | 2.4                  | -                    | V    |      |
| Output low voltage (LVTTL)<br>Output $\bar{L}$ -level voltage (I <sub>out</sub> = +2mA)              | $V_{OL}$   | -                    | 0.4                  | V    |      |
| Output high voltage (LVCMOS)<br>Output $\bar{H}$ -level voltage (I <sub>out</sub> = -100uA)          | $V_{OH}$   | V <sub>CC</sub> -0.2 | -                    | V    |      |
| Output low voltage (LVCMOS)<br>Output $\bar{L}$ -level voltage (I <sub>out</sub> = +100uA)           | $V_{OL}$   | -                    | 0.2                  | V    |      |
| Input leakage current, any input<br>(0 V < V <sub>in</sub> < V <sub>CC</sub> , all other pins = 0 V) | $I_{I(L)}$ | -10                  | 10                   | μA   |      |
| Output leakage current<br>(DO is disabled, 0 V < V <sub>out</sub> < V <sub>CC</sub> )                | $I_{O(L)}$ | - 10                 | 10                   | μA   |      |



### AC Characteristics <sup>5)6)</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 3.3$  V  $\pm$  0.3V,  $t_T = 2$  ns

16E

| Parameter | Symbol | Limit Values |      | Unit | Note |
|-----------|--------|--------------|------|------|------|
|           |        | -60          |      |      |      |
|           |        | min.         | max. |      |      |

#### **common parameters**

|                                                     |           |     |     |    |   |
|-----------------------------------------------------|-----------|-----|-----|----|---|
| Random read or write cycle time                     | $t_{RC}$  | 104 | –   | ns |   |
| $\overline{RAS}$ precharge time                     | $t_{RP}$  | 40  | –   | ns |   |
| $\overline{RAS}$ pulse width                        | $t_{RAS}$ | 60  | 10k | ns |   |
| $\overline{CAS}$ pulse width                        | $t_{CAS}$ | 10  | 10k | ns |   |
| Row address setup time                              | $t_{ASR}$ | 0   | –   | ns |   |
| Row address hold time                               | $t_{RAH}$ | 10  | –   | ns |   |
| Column address setup time                           | $t_{ASC}$ | 0   | –   | ns |   |
| Column address hold time                            | $t_{CAH}$ | 10  | –   | ns |   |
| $\overline{RAS}$ to $\overline{CAS}$ delay time     | $t_{RCD}$ | 14  | 45  | ns |   |
| $\overline{RAS}$ to column address delay            | $t_{RAD}$ | 12  | 30  | ns |   |
| $\overline{RAS}$ hold time                          | $t_{RSH}$ | 15  | –   | ns |   |
| $\overline{CAS}$ hold time                          | $t_{CSH}$ | 50  | –   | ns |   |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | $t_{CRP}$ | 5   | –   | ns |   |
| Transition time (rise and fall)                     | $t_T$     | 1   | 50  | ns | 7 |

#### **Read Cycle**

|                                                       |           |    |    |    |       |
|-------------------------------------------------------|-----------|----|----|----|-------|
| Access time from $\overline{RAS}$                     | $t_{RAC}$ | –  | 60 | ns | 8, 9  |
| Access time from $\overline{CAS}$                     | $t_{CAC}$ | –  | 15 | ns | 8, 9  |
| Access time from column address                       | $t_{AA}$  | –  | 30 | ns | 8, 10 |
| $\overline{OE}$ access time                           | $t_{OEA}$ | –  | 15 | ns |       |
| Column address to $\overline{RAS}$ lead time          | $t_{RAL}$ | 30 | –  | ns |       |
| Read command setup time                               | $t_{RCS}$ | 0  | –  | ns |       |
| Read command hold time                                | $t_{RCH}$ | 0  | –  | ns | 11    |
| Read command hold time referenced to $\overline{RAS}$ | $t_{RRH}$ | 0  | –  | ns | 11    |
| $\overline{CAS}$ to output in low-Z                   | $t_{CLZ}$ | 0  | –  | ns | 8     |
| Output buffer turn-off delay                          | $t_{OFF}$ | 0  | 15 | ns | 12    |
| Output turn-off delay from $\overline{OE}$            | $t_{OEZ}$ | 0  | 15 | ns | 12    |
| Data to $\overline{CAS}$ low delay                    | $t_{DZC}$ | 0  | –  | ns | 13    |

### AC Characteristics (cont'd) <sup>5)6)</sup>

$T_A = 0$  to  $70$  °C,  $V_{CC} = 3.3$  V  $\pm$  0.3V,  $t_T = 2$  ns

16E

| Parameter                           | Symbol    | Limit Values |      | Unit | Note |
|-------------------------------------|-----------|--------------|------|------|------|
|                                     |           | -60          |      |      |      |
|                                     |           | min.         | max. |      |      |
| Data to $\overline{OE}$ low delay   | $t_{DZO}$ | 0            | –    | ns   | 13   |
| $\overline{CAS}$ high to data delay | $t_{CDD}$ | 13           | –    | ns   | 14   |
| $\overline{OE}$ high to data delay  | $t_{ODD}$ | 13           | –    | ns   | 14   |

### Write Cycle

|                                             |           |    |   |    |    |
|---------------------------------------------|-----------|----|---|----|----|
| Write command hold time                     | $t_{WCH}$ | 10 | – | ns |    |
| Write command pulse width                   | $t_{WCP}$ | 10 | – | ns |    |
| Write command setup time                    | $t_{WCS}$ | 0  | – | ns | 15 |
| Write command to $\overline{RAS}$ lead time | $t_{RWL}$ | 15 | – | ns |    |
| Write command to $\overline{CAS}$ lead time | $t_{CWL}$ | 15 | – | ns |    |
| Data setup time                             | $t_{DS}$  | 0  | – | ns | 16 |
| Data hold time                              | $t_{DH}$  | 10 | – | ns | 16 |

### Read-modify-Write Cycle

|                                                |            |     |   |    |    |
|------------------------------------------------|------------|-----|---|----|----|
| Read-write cycle time                          | $t_{RWC}$  | 138 | – | ns |    |
| $\overline{RAS}$ to $\overline{WE}$ delay time | $t_{RWD}$  | 77  | – | ns | 15 |
| $\overline{CAS}$ to $\overline{WE}$ delay time | $t_{CWD}$  | 32  | – | ns | 15 |
| Column address to $\overline{WE}$ delay time   | $t_{AWD}$  | 47  | – | ns | 15 |
| $\overline{OE}$ command hold time              | $t_{OEHL}$ | 13  | – | ns |    |

### Hyper Page Mode (EDO) Cycle

|                                                      |            |    |      |    |   |
|------------------------------------------------------|------------|----|------|----|---|
| Hyper page mode (EDO) cycle time                     | $t_{HPC}$  | 25 | –    | ns |   |
| $\overline{CAS}$ precharge time                      | $t_{CP}$   | 10 | –    | ns |   |
| Access time from $\overline{CAS}$ precharge          | $t_{CPA}$  | –  | 32   | ns | 7 |
| Output data hold time                                | $t_{COH}$  | 3  | –    | ns |   |
| $\overline{RAS}$ pulse width in EDO mode             | $t_{RAS}$  | 60 | 200k | ns |   |
| $\overline{CAS}$ precharge to $\overline{RAS}$ Delay | $t_{RHCP}$ | 32 | –    | ns |   |
| $\overline{OE}$ setup time prior to $\overline{CAS}$ | $t_{OES}$  | 5  | –    | 5  | – |

### AC Characteristics (cont'd) <sup>5)6)</sup>

16E

$T_A = 0$  to  $70$  °C,  $V_{CC} = 3.3$  V  $\pm$  0.3V,  $t_T = 2$  ns

| Parameter | Symbol | Limit Values |      | Unit | Note |
|-----------|--------|--------------|------|------|------|
|           |        | -60          |      |      |      |
|           |        | min.         | max. |      |      |

### **Hyper Page Mode (EDO) Read-modify-Write Cycle**

|                                               |            |    |   |    |  |
|-----------------------------------------------|------------|----|---|----|--|
| Hyper page mode (EDO) read-write cycle time   | $t_{PRWC}$ | 68 | – | ns |  |
| $\overline{CAS}$ precharge to $\overline{WE}$ | $t_{CPWD}$ | 49 | – | ns |  |

### **$\overline{CAS}$ -before- $\overline{RAS}$ refresh cycle**

|                                                     |           |    |   |    |  |
|-----------------------------------------------------|-----------|----|---|----|--|
| $\overline{CAS}$ setup time                         | $t_{CSR}$ | 10 | – | ns |  |
| $\overline{CAS}$ hold time                          | $t_{CHR}$ | 10 | – | ns |  |
| $\overline{RAS}$ to $\overline{CAS}$ precharge time | $t_{RPC}$ | 5  | – | ns |  |
| Write to $\overline{RAS}$ precharge time            | $t_{WRP}$ | 10 | – | ns |  |
| Write hold time referenced to $\overline{RAS}$      | $t_{WRH}$ | 10 | – | ns |  |

### **$\overline{CAS}$ -before- $\overline{RAS}$ counter test cycle**

|                                 |           |    |   |    |  |
|---------------------------------|-----------|----|---|----|--|
| $\overline{CAS}$ precharge time | $t_{CPT}$ | 40 | – | ns |  |
|---------------------------------|-----------|----|---|----|--|

### **Self Refresh Cycle (L-versions only)**

|                              |            |      |   |    |    |
|------------------------------|------------|------|---|----|----|
| $\overline{RAS}$ pulse width | $t_{RASS}$ | 100k | – | ns | 17 |
| $\overline{RAS}$ precharge   | $t_{RPS}$  | 110  | – | ns | 17 |
| $\overline{CAS}$ hold time   | $t_{CHS}$  | -50  | – | ns | 17 |

**Notes:**

- 1) All voltages are referenced to  $V_{SS}$ .
- 2)  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC6}$  depend on cycle rate.
- 3)  $I_{CC1}$  and  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
- 4) Address can be changed once or less while  $RAS = Vil$ . In case of  $ICC4$  it can be changed once or less during a hyper page mode (EDO) cycle
- 5) An initial pause of 200  $\mu s$  is required after power-up followed by 8  $\overline{RAS}$  cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8  $\overline{CAS}$ -before- $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
- 6) AC measurements assume  $t_T = 2$  ns.
- 7)  $V_{IH (min.)}$  and  $V_{IL (max.)}$  are reference levels for measuring timing of input signals. Transition times are also measured between  $V_{IH}$  and  $V_{IL}$ .
- 8) Measured with a load equivalent to 1 TTL loads and 100 pF, ( $V_{ol} = 0.8$  V and  $V_{oh} = 2.0$  V).
- 9) Operation within the  $t_{RCD (max.)}$  limit ensures that  $t_{RAC (max.)}$  can be met.  $t_{RCD (max.)}$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD (max.)}$  limit, then access time is controlled by  $t_{CAC}$ .
- 10) Operation within the  $t_{RAD (max.)}$  limit ensures that  $t_{RAC (max.)}$  can be met.  $t_{RAD (max.)}$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD (max.)}$  limit, then access time is controlled by  $t_{AA}$ .
- 11) Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
- 12)  $t_{OFF (max.)}$ ,  $t_{OEZ (max.)}$  define the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels.  $t_{OFF}$  is referenced from the rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ , whichever occurs last.
- 13) Either  $t_{DZC}$  or  $t_{DZO}$  must be satisfied.
- 14) Either  $t_{CDD}$  or  $t_{ODD}$  must be satisfied.
- 15)  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} > t_{WCS (min.)}$ , the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if  $t_{RWD} > t_{RWD (min.)}$ ,  $t_{CWD} > t_{CWD (min.)}$  and  $t_{AWD} > t_{AWD (min.)}$ , the cycle is a read-write cycle and I/O will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of I/O (at access time) is indeterminate.
- 16) These parameters are referenced to the  $\overline{CAS}$  leading edge in early write cycles and to the  $\overline{WE}$  leading edge in read-write cycles.
- 17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:  
If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.  
If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh

### Serial Presence Detects:

A serial presence detect storage device -- E<sup>2</sup>PROM is assembled on to the module. Information about the modul confuguration, speed, etc. is written into the EEPROM device during module production using a serial presence detect protocol ( I<sup>2</sup>C synchronous 2-wire bus).

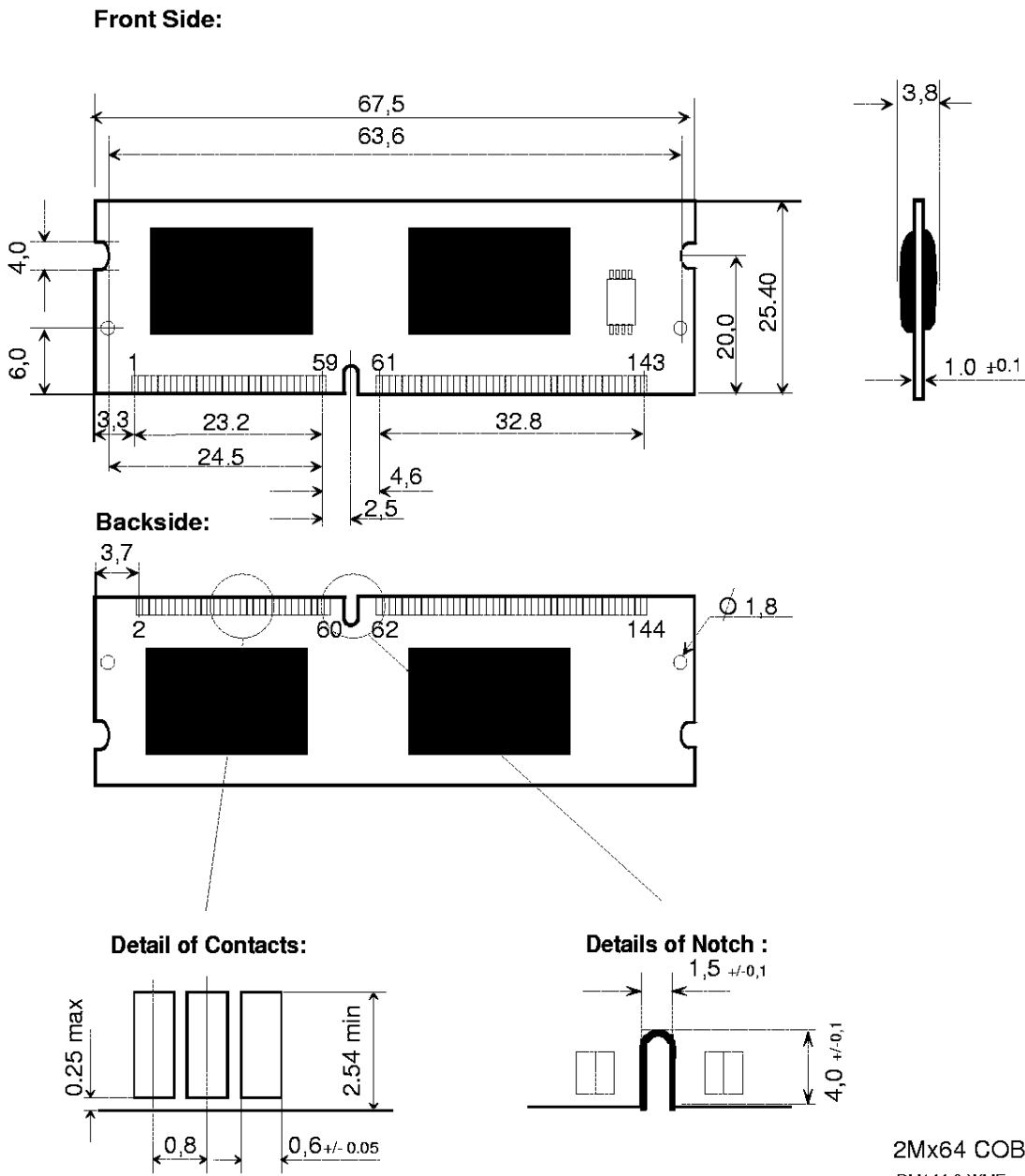
### Standard Version (without Self Refresh & Low Power)

| Byte#   | Description<br>SPD Entry Value               | Hex<br>HYM           |                      |                      |                      |    |
|---------|----------------------------------------------|----------------------|----------------------|----------------------|----------------------|----|
|         |                                              | 64<br>V1005<br>GC-60 | 64<br>V2005<br>GC-60 | 64<br>V4005<br>GC-60 | 64<br>V8005<br>GC-60 |    |
| 0       | Number of SPD bytes                          | 128                  | 80                   | 80                   | 80                   | 80 |
| 1       | Total bytes in Serial PD                     | 256                  | 08                   | 08                   | 08                   | 08 |
| 2       | Memory Type                                  | EDO                  | 02                   | 02                   | 02                   | 02 |
| 3       | Number of Row Addresses                      |                      | 0A                   | 0B                   | 0C                   | 0C |
| 4       | Number of Column Addresses                   |                      | 0A                   | 0A                   | 0A                   | 0B |
| 5       | Number of DIMM Banks                         | 1                    | 01                   | 01                   | 01                   | 01 |
| 6       | Module Data Width                            | x64                  | 40                   | 40                   | 40                   | 40 |
| 7       | Module Data Width (cont'd)                   | 0                    | 00                   | 00                   | 00                   | 00 |
| 8       | Module Interface Levels                      | LVTTL                | 01                   | 01                   | 01                   | 01 |
| 9       | RAS access time                              | 60 ns                | 3C                   | 3C                   | 3C                   | 3C |
| 10      | CAS access time                              | 15 ns                | 0F                   | 0F                   | 0F                   | 0F |
| 11      | Dimm Config (Error Det/Corr.)                | none                 | 00                   | 00                   | 02                   | 02 |
| 12      | Refresh Rate/Type                            | normal<br>15.6µs     | 00                   | 00                   | 00                   | 00 |
| 13      | Primary DRAM data width                      |                      | 10                   | 08                   | 10                   | 08 |
| 14      | Error checking DRAM data width               | none                 | 00                   | 00                   | 00                   | 00 |
| 15-31   | reserved for future offerings                |                      | FF                   | FF                   | FF                   | FF |
| 32      | Superset Memory Type                         | NA                   | FF                   | FF                   | FF                   | FF |
| 33-61   | Superset information (may be used in future) | NA                   | FF                   | FF                   | FF                   | FF |
| 62      | SPD Revision Designator                      | Rev. 1.0             | 01                   | 01                   | 01                   | 01 |
| 63      | Checksum for bytes 0-62                      |                      |                      | 06                   | 0F                   |    |
| 64-127  | Manufacturer Information (optional)          |                      | FF                   | FF                   | FF                   | FF |
| 128-255 | Unused Storage Locations                     |                      | FF                   | FF                   | FF                   | FF |

### Low Power Version with Self Refresh:

| Byte#<br>Description<br>SPD Entry Value |                                              |              | Hex<br>HYM            |                       |                       |                       |
|-----------------------------------------|----------------------------------------------|--------------|-----------------------|-----------------------|-----------------------|-----------------------|
|                                         |                                              |              | 64<br>V1005<br>GCL-60 | 64<br>V2005<br>GCL-60 | 64<br>V4005<br>GCL-60 | 64<br>V8005<br>GCL-60 |
| 0                                       | Number of SPD bytes                          | 128          | 80                    | 80                    | 80                    | 80                    |
| 1                                       | Total bytes in Serial PD                     | 256          | 08                    | 08                    | 08                    | 08                    |
| 2                                       | Memory Type                                  | EDO          | 02                    | 02                    | 02                    | 02                    |
| 3                                       | Number of Row Addresses                      |              | 0A                    | 0B                    | 0C                    | 0C                    |
| 4                                       | Number of Column Addresses                   |              | 0A                    | 0A                    | 0A                    | 0B                    |
| 5                                       | Number of DIMM Banks                         | 1            | 01                    | 01                    | 01                    | 01                    |
| 6                                       | Module Data Width                            | x64          | 40                    | 40                    | 40                    | 40                    |
| 7                                       | Module Data Width (cont'd)                   | 0            | 00                    | 00                    | 00                    | 00                    |
| 8                                       | Module Interface Levels                      | LVTTL        | 01                    | 01                    | 01                    | 01                    |
| 9                                       | RAS access time                              | 60 ns        | 3C                    | 3C                    | 3C                    | 3C                    |
| 10                                      | CAS access time                              | 15 ns        | 0F                    | 0F                    | 0F                    | 0F                    |
| 11                                      | Dimm Config (Error Det/Corr.)                | none         | 00                    | 00                    | 02                    | 02                    |
| 12                                      | Refresh Rate/Type                            | self refresh | 85                    | 84                    | 83                    | 83                    |
| 13                                      | Primary DRAM data width                      |              | 10                    | 08                    | 10                    | 08                    |
| 14                                      | Error checking DRAM data width               | none         | 00                    | 00                    | 00                    | 00                    |
| 15-31                                   | reserved for future offerings                |              | FF                    | FF                    | FF                    | FF                    |
| 32                                      | Superset Memory Type                         | NA           | FF                    | FF                    | FF                    | FF                    |
| 33-61                                   | Superset information (may be used in future) | NA           | FF                    | FF                    | FF                    | FF                    |
| 62                                      | SPD Revision Designator                      | Rev. 1.0     | 01                    | 01                    | 01                    | 01                    |
| 63                                      | Checksum for bytes 0-62                      |              |                       |                       |                       |                       |
| 64-127                                  | Manufacturer Information (optional)          |              | FF                    | FF                    | FF                    | FF                    |
| 128-255                                 | Unused Storage Locations                     |              | FF                    | FF                    | FF                    | FF                    |

**L-DIM-144-C1 to L-DIM-144-C4  
SO-DIMM Module package  
(144 pin, dual read-out, single in-line COB memory module)**



preliminary drawing