Intel StrataFlash® Cellular Memory (M18)

Datasheet

Product Features

- **High Performance Read, Program and Erase**
  - 96 ns initial access for reads
  - 512-Mbit device: 108 MHz with zero wait-state synchronous burst reads: 7 ns clock-to-data output
  - 256-Mbit device: 133 MHz with zero wait-state synchronous burst reads: 5.5 ns clock-to-data output
  - 8-, 16-, and continuous-word synchronous-burst
  - Programmable WAIT configuration
  - Customer-configurable output driver impedance
  - Buffered Enhanced Factory Programming (BEFP): 2.1 µs/byte (typ)
  - 1.8 V low-power buffered programming: 2.1 µs/byte (typ)
  - Block Erase: 0.9 s per block (typ)
- **Architecture**
  - 16-bit wide data bus
  - Multi-Level Cell Technology
  - Symmetrically Blocked Array Architecture
  - 256-Kbyte Erase Blocks
  - 512-Mb device: Eight 64-Mbit partitions
  - 256-Mb device: Eight 32-Mbit partitions
  - Four additional 8-Kbyte Extended Flash Array (EFA) Blocks
  - Read-While-Program and Read-While-Erase
  - Status register for partition and device status
  - Blank Check feature
- **Quality and Reliability**
  - Expanded temperature: –30° C to +85° C
  - Minimum 100,000 erase cycles per block
  - ETOX™ IX Process Technology (90 nm)
- **Power**
  - Core voltage: 1.7 V - 2.0 V
  - I/O voltage: 1.7 V - 2.0 V
  - Standby current: 50 µA (typ)
  - Deep Power-Down mode: 2 µA (typ)
  - Automatic Power Savings mode
  - 16-word synchronous-burst read current: 23 mA (typ)
- **Software**
  - 20 µs (typ) program suspend
  - 20 µs (typ) erase suspend
  - Intel® Flash Data Integrator optimized
  - Basic Command Set (BCS) and Extended Command Set (ECS) compatible
  - Common Flash Interface (CFI)
- **Security**
  - OTP Registers:
    - 64 unique pre-programmed bits
    - 64 user-programmable bits
    - Additional 2048 user-programmable bits
  - Absolute write protection with V_{PP} = GND
  - Power-transition erase/program lockout
  - Individual zero-latency block locking
  - Individual block lock-down
- **Density and Packaging**
  - Density: 512 Mbit, 256 Mbit
  - Address-data multiplexed and non-multiplexed
  - x16D (105-ball) Flash SCSP package
  - x16C (107-ball) Flash SCSP package
  - 0.8 mm solder-ball pitch lead-free

The Intel StrataFlash® Cellular Memory (M18) is the 5th generation Intel StrataFlash® memory with multi-level cell (MLC) technology. It provides high performance, low-power synchronous-burst read mode and asynchronous read mode at 1.8 V. It features flexible, multi-partition read-while-program and read-while-erase capability, enabling background programming or erasing in one partition simultaneously with code execution or data reads in another partition. This dual operation architecture also allows two processors to interleave code operations while program and erase operations take place in the background. The eight partitions allow flexibility for system designers to choose the size of the code and data segments. The Intel StrataFlash® Cellular Memory (M18) is manufactured using Intel 90 nm ETOX™ IX process technology and is available in industry-standard chip-scale packaging.

Order Number: 309823, Revision: 003
23-Feb-2006

Contents

Revision History

Revision Date	Revision	Description
October 05	001	Initial Release
28-Dec-05	002	Made the following specifcations changes: Initial read access speed changed to 96 ns as shown in "High Performance Read, Program and Erase" on page 1. Revised I_{CCS} test conditions in Table 7 "DC Current Specifications" on page 31. Latency count for 66 MHz changed to 7 in Table 7 "DC Current Specifications" on page 31 and in Table 24 "CLK Frequencies for LC Settings" on page 73. Latency count for 108 MHz changed to 10 in Table 7 "DC Current Specifications" on page 31. Latency count for 133 MHz changed to 13 in Table 7 "DC Current Specifications" on page 31 and in Table 24 "CLK Frequencies for LC Settings" on page 73. Revised V_{PP} Program and Erase specifications and test conditions in Table 7 "DC Current Specifications" on page 31. R201 t_{CLK} changed to 9.26 in Table 12 "AC Read, 512 Mbit, 108 MHz, VCCQ = 1.7 V to 2.0 V" on page 36. R317 t_{VHCH} min changed to 2 in Table 13 "AC Read, 256 Mbit, 133 MHz, VCCQ = 1.7 V to 2.0 V" on page 38. Added data and adress valid information to Table 3 "Signal Descriptions for x16D / x16D AD-Mux Ballout" on page 19. Updated the description for the ADV# signal to include 108 MHz in Table 4 "Signal Descriptions for x16C / x16C AD-Mux Ballout" on page 25. Updated the data value in the comments column of the BEFP Confirm operation in Figure 60 "Buffered EFP Flowchart" on page 101. Updated the address signal names to Address [Max:4] [A] and A[3:0] in Figure 14 "Asynchronous Single-Word Read with ADV# Latch" on page 40.
23-Feb-06	003	Made the following specification updates: Corrected two typographical errors as follows: 512 KB changed to 512 bytes and 1 KB changed to 512 bytes in Section 9.6.1, "Control Mode" on page 79. Corrected one typographical error as follows: Max value for R17 changed from 14 to 9 in Table 12 "AC Read, 512 Mbit, 108 MHz, VCCQ = 1.7 V to 2.0 V" on page 36. Updated the package in Figure 3 "Mechanical Specifications for x16D (105-ball) package (8x10x1.4 mm)" on page 13. Changed wording from "power transitions" to "signal transitions" in notes for Table 5 "Absolute Maximum Ratings" on page 29. Changed value for T_C in notes for Table 7 "DC Current Specifications" on page 31. Changed wording from "power transitions" to "signal transitions" in notes for Table 8 "DC Voltage Specifications" on page 33. Changed value for T_C in notes for Table 9 "Capacitance" on page 33. Revised Table 11 "Test configuration component value for worst case speed conditions" on page 35. Revised symbol in the symbol column for R17 in Table 12 "AC Read, 512 Mbit, 108 MHz, VCCQ = 1.7 V to 2.0 V" on page 36. Changed value for T_C in notes for Table 15 "Program and Erase Characteristics" on page 59. Revised the Table 63 "Package Ordering Information" on page 125 as follows: Changed the package of the non-mux x16D 105-ball 512 + 512 flash device to 8 x 10 x 1.4. Also added the following new line item: Mux x16D 105-ball 512 + 512 flash device 8 x 10 x 1.4 package.

§§

1.0 Introduction

1.1 Document Purpose

This document describes the device interface, operations, and specifications of the Intel StrataFlash® Cellular Memory (M18) device.

1.2 Nomenclature

1.8 V	Refers to V_{cc} and V_{ccq} voltage range of 1.7 V to 2.0 V
Block	A group of bits that erase with one erase command
Main Array	A group of 256-KB blocks used for storing code or data
Extended Flash Array	A group of four 8-KB blocks outside of the main array
Partition	A group of blocks that share common program and erase circuitry and command status register
Programming Region	An aligned 1-KB section of the main array
Segment	A 32-byte section of the programming region
Byte	8 bits
Word	2 bytes = 16 bits
Kb	1024 bits
KB	1024 bytes
KW	1024 words
Mb	1,048,576 bits
MB	1,048,576 bytes

1.3 Acronyms

BCS	Basic Command Set
CFI	Common Flash Interface
CUI	Command User Interface
DU	Don't Use
ECR	Enhanced Configuration Register (Flash)
EFA	Extended Flash Array
ETOX	EPROM Tunnel Oxide

FDI	Flash Data Integrator
RCR	Read Configuration Register (Flash)
RFU	Reserved for Future Use
SCSP	Stacked Chip Scale Package
SR	Status Register

1.4 Conventions

Group Membership Brackets	Square brackets are used to designate group membership or to define a group of signals with a similar function, such as A[21:1].
VCC vs. V_{CC}	When referring to a signal or package-connection name, the notation used is VCC. When referring to a timing or electrical level, the notation used is subscripted such as V_{CC}.
Device	This term is used interchangeably throughout this document to denote either a particular die, or all die in the package.
F[3:1]-CE#, F[2:1]-OE#	This is the method used to refer to more than one chip-enable or output enable. When each is referred to individually, the reference is F1-CE# and F1-OE# (for die #1), and F2-CE# and F2-OE# (for die #2).
F-VCC	When referencing flash memory signals or timings, the notation used is F-VCC or F-$V_{CC,}$ respectively.
00FFh	Denotes 16-bit hexadecimal numbers
00FF 00FFh	Denotes 32-bit hexadecimal numbers

2.0 Functional Overview

This section provides an overview of the device features and a detailed description of the device memory architecture.

2.1 Product Description

The Intel StrataFlash® Cellular Memory (M18) device provides high read and write performance at low voltage on a 16-bit data bus.

The flash memory device has a multi-partition architecture with read-while-program and read-while-erase capability. It supports synchronous burst reads of up to 108 MHz on 512-Mb and devices and 133 MHz on 256-Mbit devices. In continuous-burst mode, data can be read from the bottom to the top of memory across partition boundaries.

Upon initial power up or return from reset, the device defaults to asynchronous array-read mode. Synchronous burst-mode reads are enabled by setting the Read Configuration Register. In synchronous burst mode, output data is synchronized with a user-supplied clock signal. A WAIT signal provides easy CPU-to-flash memory synchronization.

Designed for low-voltage applications, the device supports read operations with V_{CC} at 1.8 V, and erase and program operations with V_{PP} at 1.8 V or 9.0 V. VCC and VPP can be tied together for a simple, ultra-low power design. In addition to voltage flexibility, a dedicated VPP connection provides complete data protection when V_{PP} is less than V_{PPLK}.

A Status Register provides status and error conditions of erase and program operations.

One-Time-Programmable registers allows unique flash device identification that can be used to increase flash content security. Also, the individual block-lock feature provides zero-latency block locking and unlocking to protect against unwanted program or erase of the array.

The flash memory device offers three power savings features: Automatic Power Savings (APS) mode, standby mode, and Deep Power-Down (DPD) mode. The device automatically enters APS following read-cycle completion. Standby is initiated when the system deselects the device by deasserting CE#. The DPD mode provides the lowest power consumption; it is enabled by setting a bit in the Enhanced Configuration Register and entered by asserting the DPD pin.

2.2 Configuration and Memory Map

The Intel StrataFlash® Cellular Memory device features a symmetrical block architecture. The device main array is divided as follows:

- The 256-Mb device has a main array of 128 blocks. There are eight 32-Mb partitions, each containing 16 blocks of 256 KB.
- The 512-Mb device has a main array of 256 blocks. There are eight 64-Mb partitions, each containing 32 blocks of 256 KB.

Flash cells within a block are organized by regions and segments.

- A block contains 256 regions of 1024 bytes that are called “programming regions”.
- Each programming region has 32 “segments” of 32 bytes each.
- The 32 segments within the programming region are divided into two halves, “A-half” and “B-half”. The A-half has A3 = 0 addresses, and the B-half has A3 = 1 addresses.

See Table 1 for main array memory map, Figure 1 for main array architecture, and Figure 2 for programming region architecture for details.

Table 1. Main Array Memory Map

		256-Mbit Device			512-Mbit Device	
		Blk #	Address Range		Blk #	Address Range
Partition 7	32Mbit	127	0FE0000-0FFFFFF	64Mbit	255	1FE0000-1FFFFFF
		⋮	⋮		⋮	⋮
		112	0E00000-0E1FFFF		224	1C00000-1C1FFFF
Partition 6	32Mbit	111	0DE0000-0DFFFFF	64Mbit	223	1BE0000-1BFFFFF
		⋮	⋮		⋮	⋮
		96	0C00000-0C1FFFF		192	1800000-181FFFF
Partition 5	32Mbit	95	0BE0000-0BFFFFF	64Mbit	191	17E0000-17FFFFF
		⋮	⋮		⋮	⋮
		80	0A00000-0A1FFFF		160	1400000-141FFFF
Partition 4	32Mbit	79	09E0000-09FFFFF	64Mbit	159	13E0000-13FFFFF
		⋮	⋮		⋮	⋮
		64	0800000-081FFFF		128	1000000-101FFFF
Partition 3	32Mbit	63	07E0000-07FFFFF	64Mbit	127	0FE0000-0FFFFFF
		⋮	⋮		⋮	⋮
		48	0600000-061FFFF		96	0C00000-0C1FFFF
Partition 2	32Mbit	47	05E0000-05FFFFF	64Mbit	95	0BE0000-0BFFFFF
		⋮	⋮		⋮	⋮
		32	0400000-041FFFF		64	0800000-081FFFF
Partition 1	32Mbit	31	03E0000-03FFFFF	64Mbit	63	07E0000-07FFFFF
		⋮	⋮		⋮	⋮
		16	0200000-021FFFF		32	0400000-041FFFF
Partition 0	32Mbit	15	01E0000-01FFFFF	64Mbit	31	03E0000-03FFFFF
		⋮	⋮		⋮	⋮
		0	0000000-001FFFF		0	0000000-001FFFF

Figure 1. Main Array Architecture

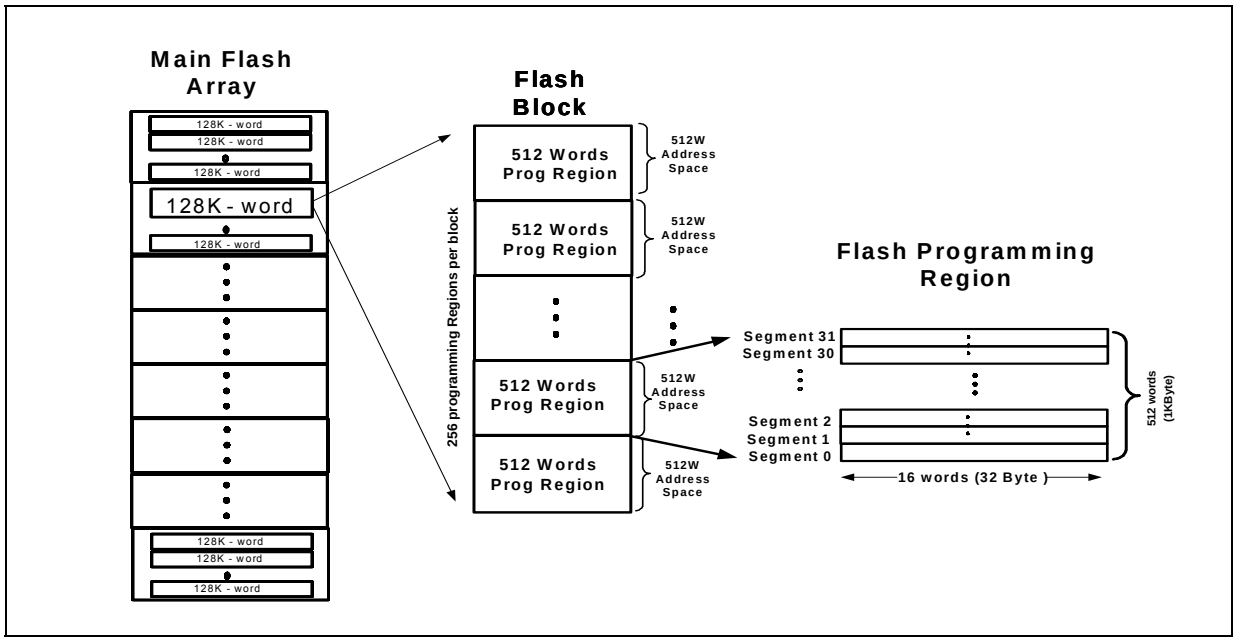
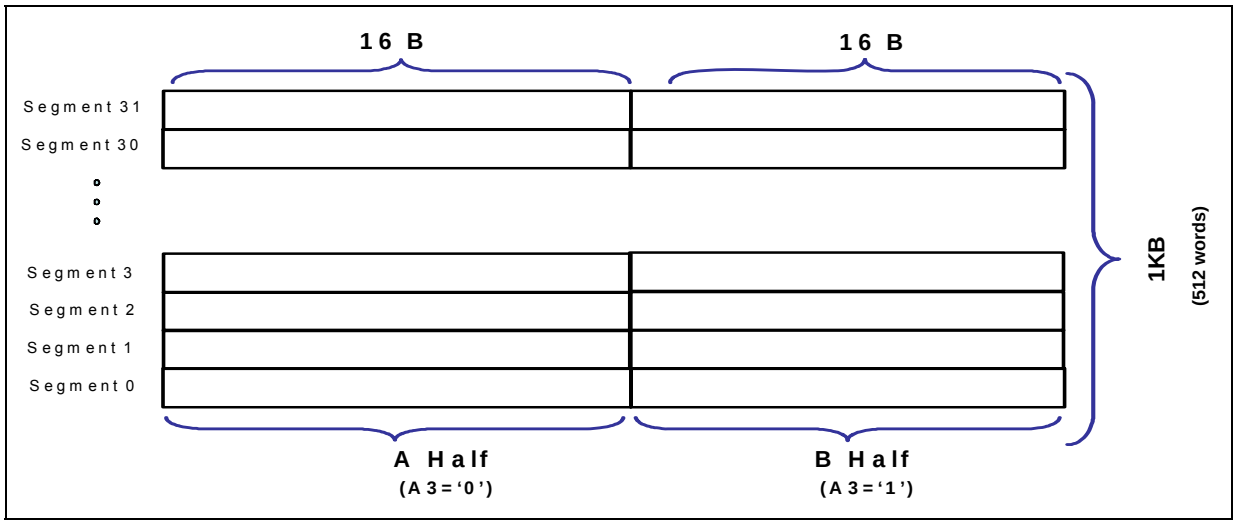


Figure 2. Programming Region Architecture



2.2.1 Extended Flash Array

In additional to the main array, the flash device features four 8-KB Extended Flash Array (EFA) blocks. The EFA block plane is not part of the main array, however it maps to a main array partition during a read, program or erase operation. See Table 2 for EFA block addresses.

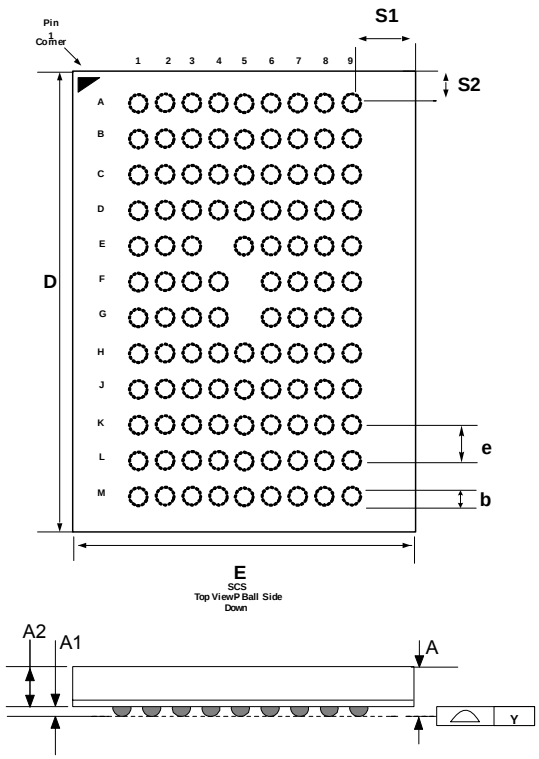
Table 2. Extended Flash Array (EFA) Blocks Memory Map

	Blk #	Address Range
256Kbit	3	0003000-0003FFF
	2	0002000-0002FFF
	1	0001000-0001FFF
	0	0000000-0000FFF

3.0 Package Information

The following figures show the ballout package information for the M18 device in x16C and x16D SCSP ballouts. Figure 3 and Figure 4 shows the x16D 105-ball package, and Figure 5 and Figure 6 show a x16C 107-ball package.

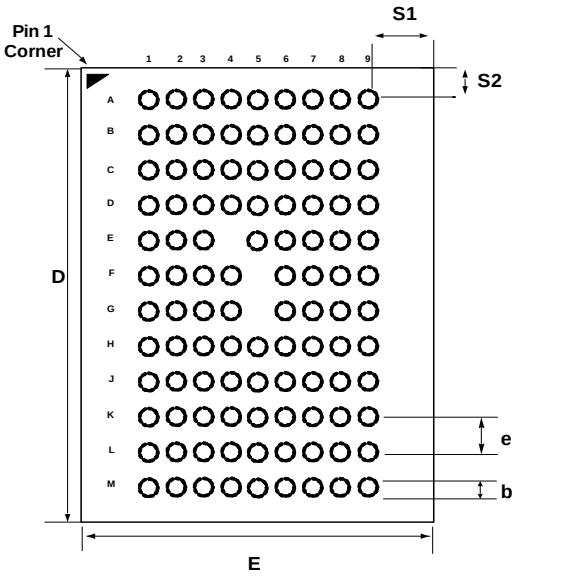
Figure 3. Mechanical Specifications for x16D (105-ball) package (8x10x1.4 mm)



Note: Drawing not to scale.

Dimensions	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.4				0.0551
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		1.070				0.0421	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	9.90	10.00	10.10		0.3898	0.3937	0.3976
Package Body Width	E	7.90	8.00	8.10		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		105				105	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball Distance Along E	S1	0.700	0.800	0.900		0.0276	0.0315	0.0354
Corner to Ball Distance Along D	S2	0.500	0.600	0.700		0.0197	0.0236	0.0276

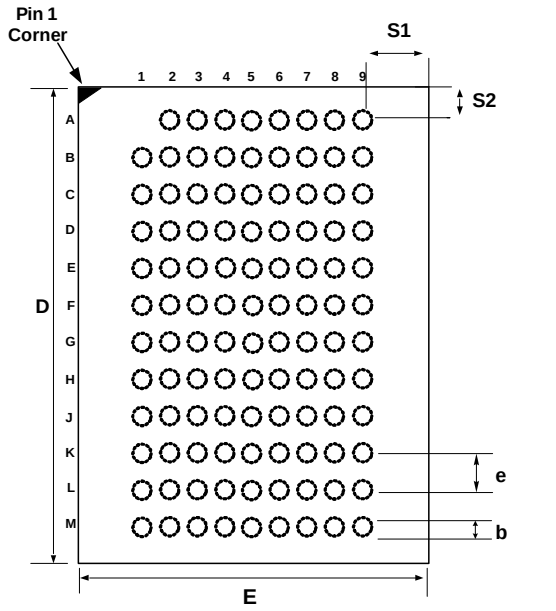
Figure 4. Mechanical Specifications for x16D (105-ball) package (9x11x1.2 mm)



Note: Drawing not to scale.

Dimensions	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.2				0.0472
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		0.860				0.0339	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	10.90	11.00	11.10		0.4291	0.4331	0.4370
Package Body Width	E	8.90	9.00	9.10		0.3504	0.3543	0.3583
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		105				105	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball Distance Along E	S1	1.200	1.300	1.400		0.0472	0.0512	0.0551
Corner to Ball Distance Along D	S2	1.000	1.100	1.200		0.0394	0.0433	0.0472

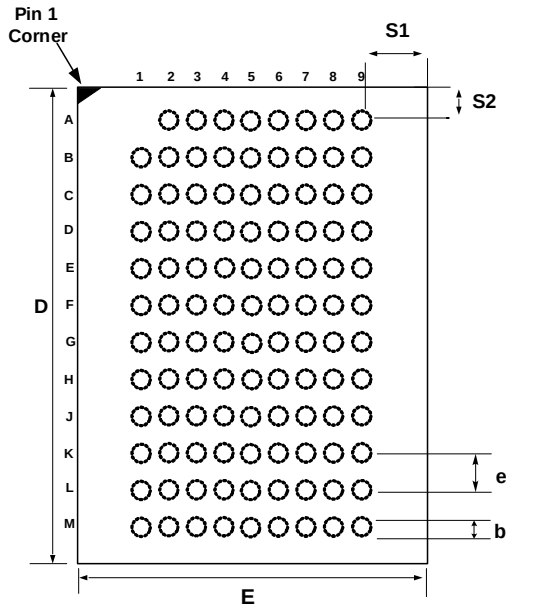
Figure 5. Mechanical Specifications for x16C (107-ball) package (8x11x1.2 mm)



Note: Drawing not to scale.

		Millimeters				Inches		
Dimensions	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.2				0.0472
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		0.860				0.0339	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	10.90	11.00	11.10		0.4291	0.4331	0.4370
Package Body Width	E	7.90	8.00	8.10		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		107				107	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball Distance Along E	S1	0.700	0.800	0.900		0.0276	0.0315	0.0354
Corner to Ball Distance Along D	S2	1.000	1.100	1.200		0.0394	0.0433	0.0472

Figure 6. Mechanical Specifications for x16C (107-ball) package (8x11x1.4 mm)



Note: Drawing not to scale.

		Millimeters				Inches		
Dimensions	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.4				0.0551
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		1.070				0.0421	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	10.90	11.00	11.10		0.4291	0.4331	0.4370
Package Body Width	E	7.90	8.00	8.10		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		107				107	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball Distance Along E	S1	0.700	0.800	0.900		0.0276	0.0315	0.0354
Corner to Ball Distance Along D	S2	1.000	1.100	1.200		0.0394	0.0433	0.0472

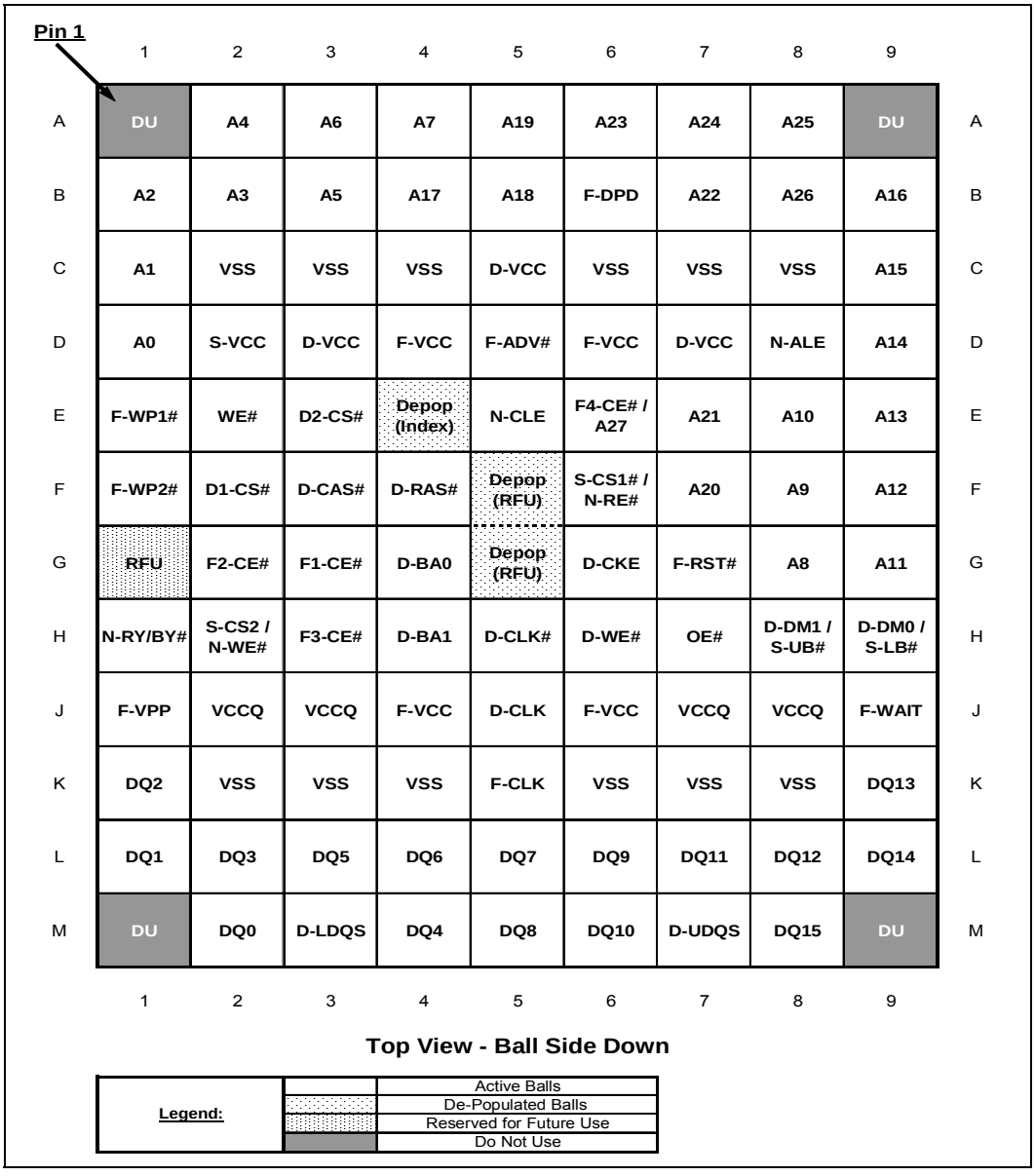
4.0 Ballout and Signal Descriptions

This section provides ballout and signal description information for x16D (105-ball) and x16C (107-ball) packages, Non-Mux and AD-Mux.

4.1 Signal Ballouts x16D

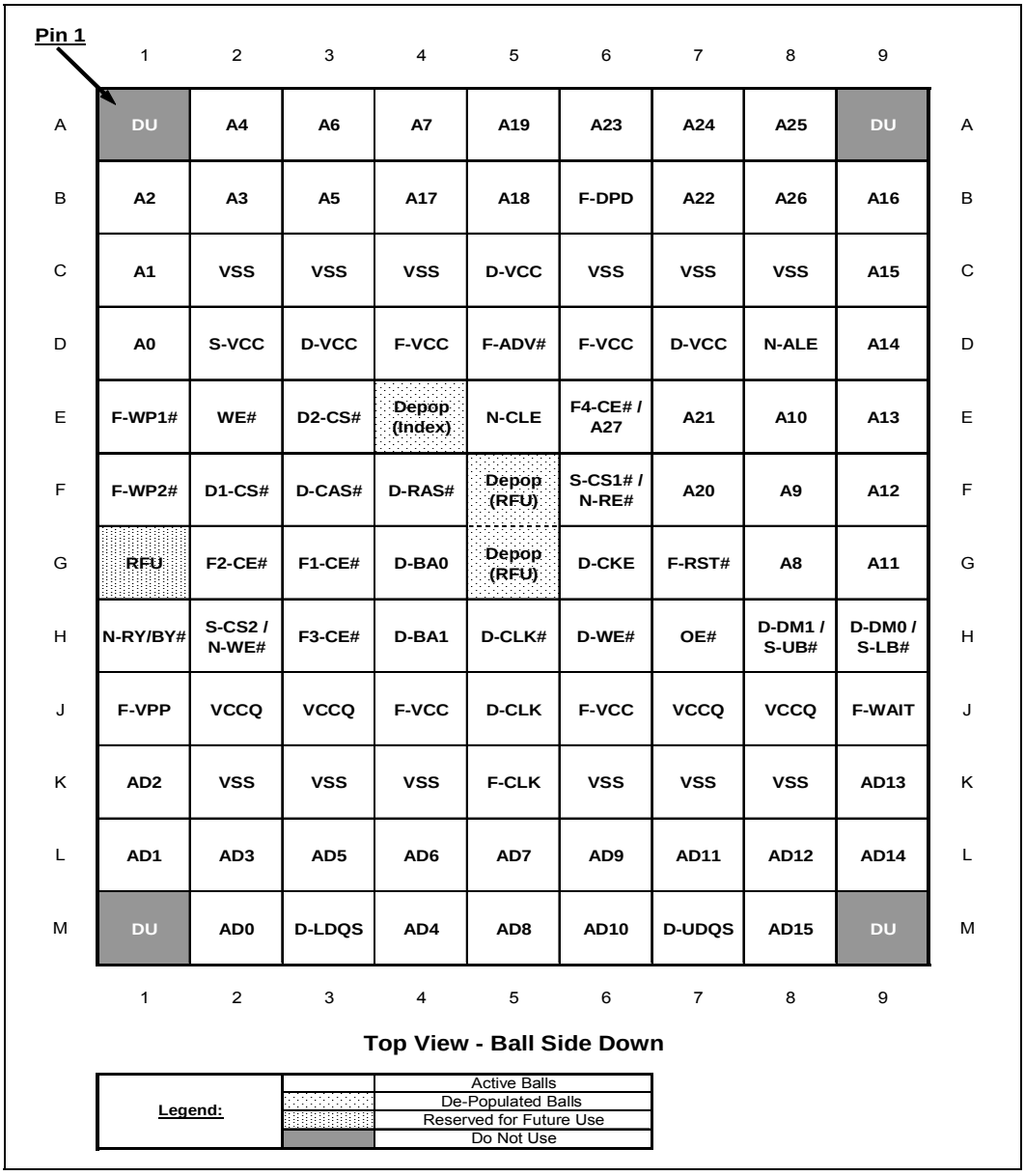
4.1.1 x16D (105-Ball) Ballout, Non-Mux

Figure 7. x16D (105-Ball) Electrical Ballout, Non-Mux



4.1.2 x16D AD-Mux (105-Ball) Ballout

Figure 8. x16D AD-Mux (105-Ball) Electrical Ballout



4.2 Signal Descriptions x16D

Table 3. Signal Descriptions for x16D / x16D AD-Mux Ballout (Sheet 1 of 4)

Symbol	Type	Signal Descriptions	Notes
Address and Data Signals, Non-Mux			
A[MAX: 0]	Input	**ADDRESS:** Global device signals. Shared address inputs for all memory die during Read and Write operations. • 4-Gbit: AMAX = A27 • 2-Gbit: AMAX = A26 • 1-Gbit: AMAX = A25 • 512-Mbit: AMAX = A24 • 256-Mbit: AMAX = A23 • 128-Mbit: AMAX = A22 • A[12:0] are the row and A[9:0] are the column addresses for 512-Mbit LPSDRAM. • A[12:0] are the row and A[8:0] are the column addresses for 256-Mbit LPSDRAM. • A[11:0] are the row and A[8:0] are the column addresses for 128-Mbit LPSDRAM. Unused address inputs should be treated as RFU.	1
DQ[15:0]	Input/ Output	**DATA INPUT/OUTPUTS:** Global device signals. DQ[15:0] are used to input commands and write-data during Write cycles, and to output read-data during Read cycles. During NAND accesses, DQ[7:0] are used to input commands, address-data, and write-data, and to output read-data. Data signals are High-Z when the device is deselected or its output is disabled.	
F-ADV#	Input	**FLASH ADDRESS VALID:** Flash-specific signal; low-true input. During synchronous flash Read operations, the address is latched on the rising edge of F-ADV#, or on the first rising edge of F-CLK after F-ADV# goes low for devices that support up to 108 MHz, or on the last rising edge of F-CLK after F-ADV# goes low for devices that support up to 133 MHz. In an asynchronous flash Read operation, the address is latched on the rising edge of F-ADV# or continuously flows through while F-ADV# is low.	
Address and Data Signals, AD-Mux			
A[MAX:16]	Input	**ADDRESS:** Global device signals. Shared address inputs for all Flash and SRAM memory die during Read and Write operations. • 4-Gbit: AMAX = A27 • ‘2-Gbit: AMAX = A26 • 1-Gbit: AMAX = A25 • 512-Mbit: AMAX = A24 • 256-Mbit: AMAX = A23 • 128-Mbit: AMAX = A22 Unused address inputs should be treated as RFU.	1

Table 3. Signal Descriptions for x16D / x16D AD-Mux Ballout (Sheet 2 of 4)

Symbol	Type	Signal Descriptions	Notes
AD[15:0]	Input / Output	**ADDRESS-DATA MULTIPLEXED INPUTS/ OUTPUTS:** AD-Mux flash and SRAM lower address and data signals; LPSDRAM data signals. During AD-Mux flash and SRAM Write cycles, AD[15:0] are used to input the lower address followed by commands or write-data. During AD-Mux flash Read cycles, AD[15:0] are used to input the lower address followed by read-data output. During LPSDRAM accesses, AD[15:0] are used to input commands and write-data during Write cycles or to output read-data during Read cycles. During NAND accesses, AD[7:0] are used to input commands, address, or write-data, and to output read-data. AD[15:0] are High-Z when the flash or SRAM is deselected or its output is disabled.	
F-ADV#	Input	**FLASH ADDRESS VALID:** Flash-specific signal; low-true input. During synchronous flash Read operations, the address is latched on the rising edge of F-ADV#, or on the first rising edge of F-CLK after F-ADV# goes low for devices that support up to 108 MHz, or on the last rising edge of F-CLK after F-ADV# goes low for devices that support up to 133 MHz. In an asynchronous flash Read operation, the address is latched on the rising edge of F-ADV#.	
Control Signals			
F[4:1]-CE#	Input	**FLASH CHIP ENABLE:** Flash-specific signal; low-true input. When low, F-CE# selects the associated flash memory die. When high, F-CE# deselects the associated flash die. Flash die power is reduced to standby levels, and its data and F-WAIT outputs are placed in a High-Z state. • F1-CE# is dedicated to flash die #1. • F[4:2]-CE# are dedicated to flash die #4 through #2, respectively, if present. Otherwise, any unused flash chip enable should be treated as RFU. • For NOR/NAND stacked device, F1-CE# selects NOR die #1, F2-CE# selects NOR die #2 while F4-CE# selects NAND die #1 and NAND die #2 using virtual chip-select scheme, F3-CE# selects NAND die #3 if present.	1
F-CLK	Input	**FLASH CLOCK:** Flash-specific signal; rising active-edge input. F-CLK synchronizes the flash with the system clock during synchronous operations.	
D-CLK	Input	**LPSDRAM CLOCK:** LPSDRAM-specific signal; rising active-edge input. D-CLK synchronizes the LPSDRAM and DDR LPSDRAM with the system clock.	2
D-CLK#	Input	**DDR LPSDRAM CLOCK:** DDR LPSDRAM-specific signal; falling active-edge input. D-CLK# synchronizes the DDR LPSDRAM with the system clock.	2
OE#	Input	**OUTPUT ENABLE:** Flash- and SRAM-specific signal; low-true input. When low, OE# enables the output drivers of the selected flash or SRAM die. When high, OE# disables the output drivers of the selected flash or SRAM die and places the output drivers in High-Z.	
F-RST#	Input	**FLASH RESET:** Flash-specific signal; low-true input. When low, F-RST# resets internal operations and inhibits writes. When high, F-RST# enables normal operation.	
F-WAIT	Output	**FLASH WAIT:** Flash -specific signal; configurable-true output. When asserted, F-WAIT indicates invalid output data. F-WAIT is driven whenever F-CE# and OE# are low. F-WAIT is High-Z whenever F-CE# or OE# is high.	
WE#	Input	**WRITE ENABLE:** Flash- and SRAM-specific signal; low-true input. When low, WE# enables Write operations for the enabled flash or SRAM die.	4
D-WE#	Input	**LPSDRAM WRITE ENABLE:** LPSDRAM-specific signal; low-true input. D-WE#, together with A[MAX:0], D-BA[1:0], D-CKE, D-CS#, D-CAS#, and D-RAS#, define the LPSDRAM command or operation. D-WE# is sampled on the rising edge of D-CLK.	2

Table 3. Signal Descriptions for x16D / x16D AD-Mux Ballout (Sheet 3 of 4)

Symbol	Type	Signal Descriptions	Notes
F-WP[2:1]#	Input	**FLASH WRITE PROTECT:** Flash-specific signals; low-true inputs. When low, F-WP# enables the Lock-Down mechanism. When high, F-WP# overrides the Lock-Down function, enabling locked-down blocks to be unlocked with the Unlock command. • F-WP1# is dedicated to flash die #1. • F-WP2# is common to all other flash dies, if present. Otherwise it is RFU. • For NOR/NAND stacked device, F-WP1# selects all NOR dies, while F-WP2# selects all NAND dies.	
F-DPD	Input	**FLASH DEEP POWER-DOWN:** Flash-specific signal; configurable-true input. When enabled in the ECR, F-DPD is used to enter and exit Deep Power-Down mode.	
N-CLE	Input	**NAND COMMAND LATCH ENABLE:** NAND-specific signal; high-true input. When high, N-CLE enables commands to be latched on the rising edge of N-WE#.	2
N-ALE	Input	**NAND ADDRESS LATCH ENABLE:** NAND-specific signal; high-true input. When high, N-ALE enables addresses to be latched on the rising edge of N-WE#.	2
N-RE#	Input	**NAND READ ENABLE:** NAND-specific signal; low-true input. When low, N-RE# enables the output drivers of the selected NAND die. When high, N-RE# disables the output drivers of the selected NAND die and places the output drivers in High-Z.	2,5
N-RY/BY#	Output	**NAND READY/BUSY:** NAND-specific signal; low-true output. When low, N-RY/BY# indicates the NAND is busy performing a read, program, or erase operation. When high, N-RY/BY# indicates the NAND device is ready.	2
N-WE#	Input	**NAND WRITE ENABLE:** NAND-specific signal; low-true input. When low, N-WE# enables Write operations for the enabled NAND die.	2,6
D-CKE	Input	**LPSDRAM CLOCK ENABLE:** LPSDRAM-specific signal; high-true input. When high, D-CKE indicates that the next D-CLK edge is valid. When low, D-CKE indicates that the next D-CLK edge is invalid and the selected LPSDRAM die is suspended.	2
D-BA[1:0]	Input	**LPSDRAM BANK SELECT:** LPSDRAM-specific input signals. D-BA[1:0] selects one of four banks in the LPSDRAM die.	2
D-RAS#	Input	**LPSDRAM ROW ADDRESS STROBE:** LPSDRAM-specific signal; low-true input. D-RAS#, together with A[MAX:0], D-BA[1:0], D-CKE, D-CS#, D-CAS#, and D-WE#, define the LPSDRAM command or operation. D-RAS# is sampled on the rising edge of D-CLK.	2
D-CAS#	Input	**LPSDRAM COLUMN ADDRESS STROBE:** LPSDRAM-specific signal; low-true input. D-CAS#, together with A[MAX:0], D-BA[1:0], D-CKE, D-CS#, D-RAS#, and D-WE#, define the LPSDRAM command or operation. D-CAS# is sampled on the rising edge of D-CLK.	2
D[2:1]-CS#	Input	**LPSDRAM CHIP SELECT:** LPSDRAM-specific signal; low-true input. When low, D-CS# selects the associated LPSDRAM memory die and starts the command input cycle. When D-CS# is high, commands are ignored but operations continue. • D-CS#, together with A[MAX:0], D-BA[1:0], D-CKE, D-RAS#, D-CAS#, and D-WE#, define the LPSDRAM command or operation. D-CS# is sampled on the rising edge of D-CLK. • D[2:1]-CS# are dedicated to LPSDRAM die #2 and die #1, respectively, if present. Otherwise, any unused LPSDRAM chip selects should be treated as RFU.	2
D-DM[1:0]	Input	**LPSDRAM DATA MASK:** LPSDRAM-specific signal; high-true input. When high, D-DM[1:0] controls masking of input data during writes and output data during reads. • D-DM1 corresponds to the data on DQ[15:8]. • D-DM0 corresponds to the data on DQ[7:0].	2,3

Table 3. Signal Descriptions for x16D / x16D AD-Mux Ballout (Sheet 4 of 4)

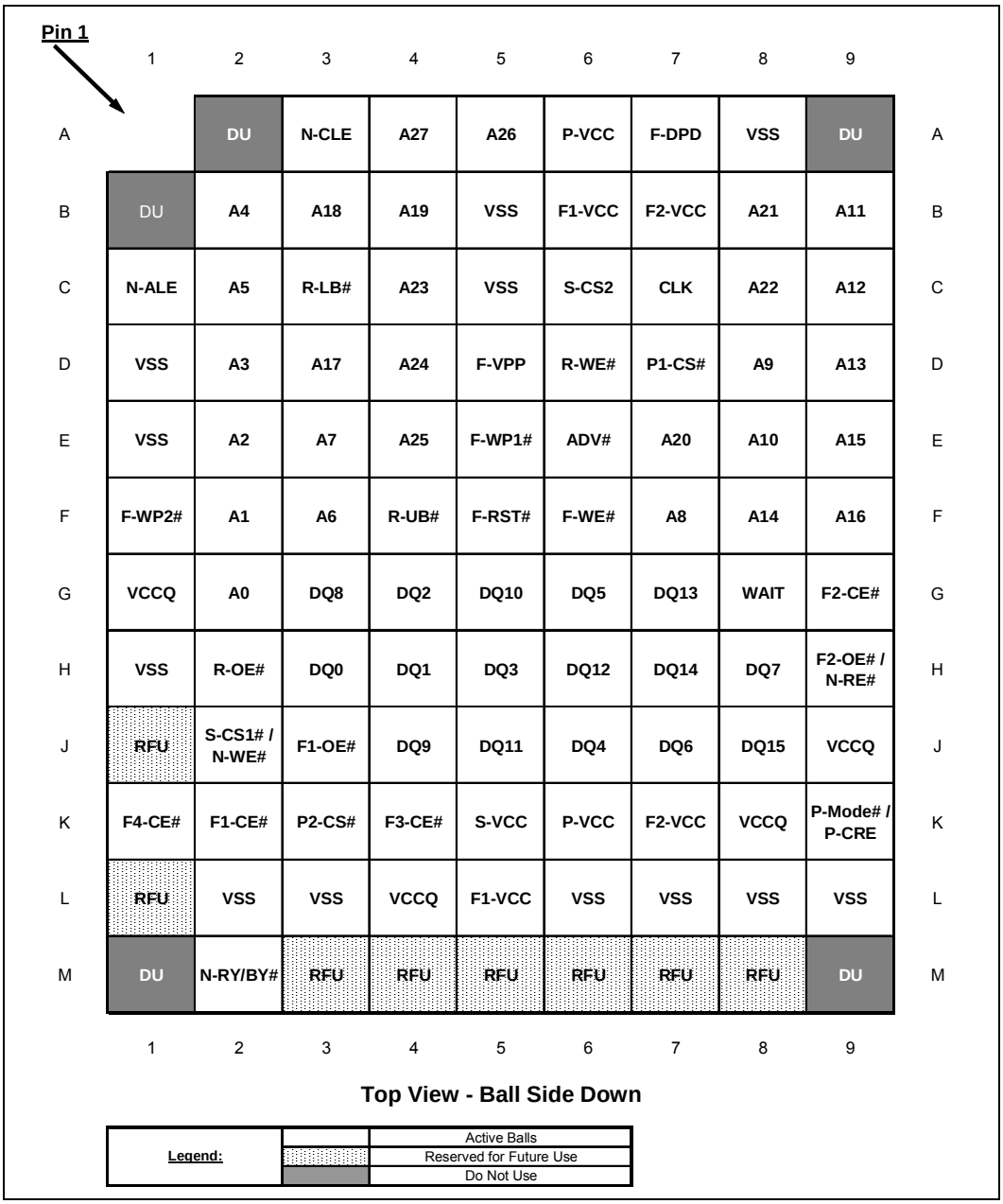
Symbol	Type	Signal Descriptions	Notes
D-UDQS D-LDQS	Input / Output	**LPSDRAM UPPER/LOWER DATA STROBE:** DDR LPSDRAM-specific input/output signals. D-UDQS and D-LDQS provide as output the read-data strobes, and as input the write-data strobes. • D-UDQS corresponds to the data on DQ[15:8]. • D-LDQS corresponds to the data on DQ[7:0].	2
S-CS1# S-CS2	Input	**SRAM CHIP SELECTS:** SRAM-specific signals; S-CS1# low-true input, S-CS2 high-true input. When both are asserted, S-CS1# and S-CS2 select the SRAM die. When either is deasserted, the SRAM die is deselected and its power is reduced to standby levels.	2,5,6
S-UB# S-LB#	Input	**SRAM UPPER/LOWER BYTE ENABLES:** SRAM-specific signals; low-true inputs. When low, S-UB# enables DQ[15:8] and S-LB# enables DQ[7:0] during SRAM Read and Write cycles. When high, S-UB# masks DQ[15:8] and S-LB# masks DQ[7:0].	2,3
Power Signals			
F-VPP	Power	**FLASH PROGRAM/ERASE VOLTAGE:** Flash specific. F-VPP supplies program or erase power to the flash die.	
F-VCC	Power	**FLASH CORE POWER SUPPLY:** Flash specific. F-VCC supplies the core power to the flash die.	
VCCQ	Power	**I/O POWER SUPPLY:** Global device I/O power. VCCQ supplies the device input/output driver voltage.	
D-VCC	Power	**LPSDRAM CORE POWER SUPPLY:** LPSDRAM specific. D-VCC supplies the core power to the LPSDRAM die.	2
S-VCC	Power	**SRAM POWER SUPPLY:** SRAM specific. S-VCC supplies the core power to the SRAM die.	2
VSS	Ground	**DEVICE GROUND:** Global ground reference for all signals and power supplies. Connect all VSS balls to system ground. Do not float any VSS connections.	
DU	—	**DO NOT USE:** This ball should not be connected to any power supplies, signals, or other balls. This ball can be left floating.	
RFU	—	**RESERVED for FUTURE USE:** Reserved by Intel for future device functionality and enhancement. This ball must be left floating.	

Notes:
1. F4-CE# and A27 share the same package ball at location E6. Only one signal function is available, depending on the stacked device combination.
2. Only available on stacked device combinations with NAND, SRAM, and/or LPSDRAM die; otherwise, treated as RFU.
3. D-DM[1:0] and S-UB#/S-LB# share the same package balls at locations H8 and H9, respectively. Only one signal function for each ball location is available, depending on the stacked device combination.
4. S-CS1# and N-RE# share the same package ball at location F6. Only one signal function is available, depending on the stacked device combination.
5. S-CS2 and N-WE# share the same package ball at location H2. Only one signal function is available, depending on the stacked device combination.

4.3 Signal Ballouts x16C

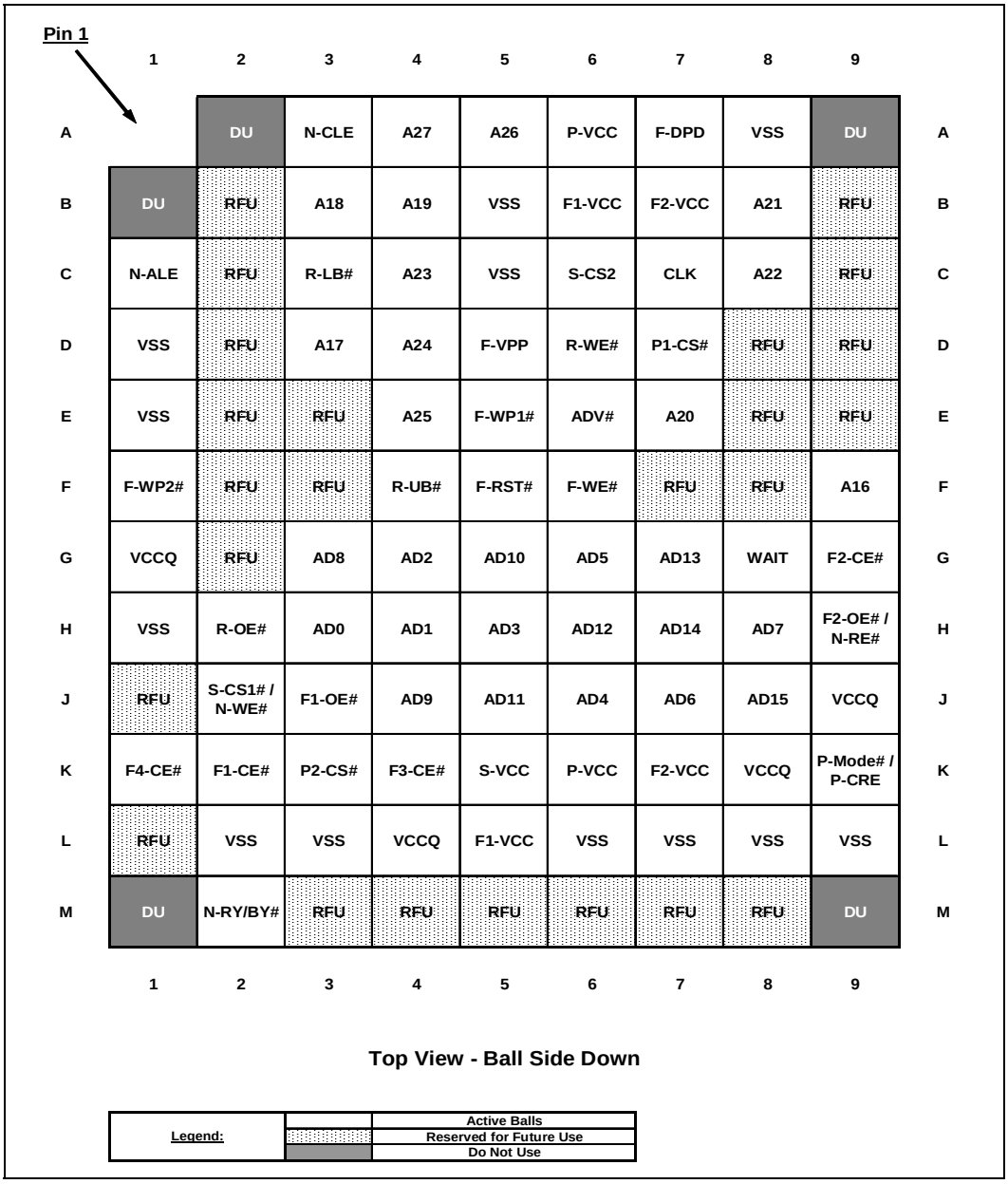
4.3.1 x16C (107-Ball) Ballout, Non-Mux

Figure 9. x16C (107-Ball) Electrical Ballout, Non-Mux



4.3.2 x16C AD-Mux (107-Ball) Ballout

Figure 10. x16C AD-Mux (107-Ball) Electrical Ballout



4.4 Signal Descriptions x16C

Table 4. Signal Descriptions for x16C / x16C AD-Mux Ballout (Sheet 1 of 4)

Symbol	Type	Signal Descriptions	Notes
Address and Data Signals, Non-Mux			
A[MAX:0]	Input	**ADDRESS:** Global device signals. Shared address inputs for all memory die during Read and Write operations. • 4-Gbit: AMAX = A27• 128-Mbit: AMAX = A22 • 2-Gbit: AMAX = A26• 64-Mbit: AMAX = A21 • 1-Gbit: AMAX = A25• 32-Mbit: AMAX = A20 • 512-Mbit: AMAX = A24• 16-Mbit: AMAX = A19 • 256-Mbit: AMAX = A23• 8-Mbit: AMAX = A18 Unused address inputs should be treated as RFU.	
DQ[15:0]	Input / Output	**DATA INPUT/OUTPUTS:** Global device signals. Inputs data and commands during Write cycles, outputs data during Read cycles. Data signals are High-Z when the device is deselected or its output is disabled.	
ADV#	Input	**ADDRESS VALID:** Flash- and Synchronous PSRAM-specific signal; low-true input. During synchronous flash Read operations, the address is latched on the rising edge of F-ADV#, or on the first rising edge of F-CLK after F-ADV# goes low for devices that support up to 108 MHz, or on the last rising edge of F-CLK after F-ADV# goes low for devices that support up to 133 MHz. In an asynchronous flash Read operation, the address is latched on the rising edge of ADV# or continuously flows through while ADV# is low.	
Address and Data Signals, AD-Mux			
A[MAX:16]	Input	**ADDRESS:** Global device signals. Shared address inputs for all memory die during Read and Write operations. • 4-Gbit: AMAX = A27• 128-Mbit: AMAX = A22 • 2-Gbit: AMAX = A26• 64-Mbit: AMAX = A21 • 1-Gbit: AMAX = A25• 32-Mbit: AMAX = A20 • 512-Mbit: AMAX = A24• 16-Mbit: AMAX = A19 • 256-Mbit: AMAX = A23• 8-Mbit: AMAX = A18 Unused address inputs should be treated as RFU.	
AD[15:0]	Input / Output	**ADDRESS-DATA MULTIPLEXED INPUTS/ OUTPUTS:** Global device signals. During AD-Mux Write cycles, AD[15:0] are used to input the lower address followed by commands or data. During AD-Mux Read cycles, AD[15:0] are used to input the lower address followed by read-data output. During NAND accesses, AD[7:0] is used to input commands, address-data, or write-data, and output read-data. AD[15:0] are High-Z when the device is deselected or its output is disabled.	
ADV#	Input	**ADDRESS VALID:** Flash- and Synchronous PSRAM-specific signal; low-true input. During synchronous flash Read operations, the address is latched on the rising edge of F-ADV#, or on the first rising edge of F-CLK after F-ADV# goes low for devices that support up to 108 MHz, or on the last rising edge of F-CLK after F-ADV# goes low for devices that support up to 133 MHz. In an asynchronous flash Read operation, the address is latched on the rising edge of ADV#.	
Control Signals			

Table 4. Signal Descriptions for x16C / x16C AD-Mux Ballout (Sheet 2 of 4)

Symbol	Type	Signal Descriptions	Notes
F[4:1]-CE#	Input	**FLASH CHIP ENABLE:** Flash-specific signal; low-true input. When low, F-CE# selects the associated flash memory die. When high, F-CE# deselects the associated flash die. Flash die power is reduced to standby levels, and its data and F-WAIT outputs are placed in a High-Z state. • F1-CE# is dedicated to flash die #1. • F[4:2]-CE# are dedicated to flash die #4 through #2, respectively, if present. Otherwise, any unused flash chip enable should be treated as RFU. • For NOR/NAND stacked device, F1-CE# selects NOR die #1, F2-CE# selects NOR die #2 while F4-CE# selects NAND die #1 and NAND die #2 using virtual chip-select scheme, F3-CE# selects NAND die #3 if present.	
CLK	Input	**CLOCK:** Flash- and Synchronous PSRAM-specific input signal. CLK synchronizes the flash and/or synchronous PSRAM with the system clock during synchronous operations.	
F[2:1]-OE#	Input	**FLASH OUTPUT ENABLE:** Flash-specific signal; low-true input. When low, F-OE# enables the output drivers of the selected flash die. When high, F-OE# disables the output drivers of the selected flash die and places the output drivers in High-Z. • For NOR only stacked device, F[2:1]-OE# are common to all NOR dies in the device. • For NOR/NAND stacked device, F1-OE# enables all NOR dies, F2-OE# selects all NAND dies if present.	2
R-OE#	Input	**RAM OUTPUT ENABLE:** PSRAM- and SRAM-specific signal; low-true input. When low, R-OE# enables the output drivers of the selected memory die. When high, R-OE# disables the output drivers of the selected memory die and places the output drivers in High-Z.	1
F-RST#	Input	**FLASH RESET:** Flash-specific signal; low-true input. When low, F-RST# resets internal operations and inhibits writes. When high, F-RST# enables normal operation.	
WAIT	Output	**WAIT:** Flash -and Synchronous PSRAM-specific signal; configurable true-level output. When asserted, WAIT indicates invalid output data. When deasserted, WAIT indicates valid output data. • WAIT is driven whenever the flash or the synchronous PSRAM is selected and its output enable is low. • WAIT is High-Z whenever flash or the synchronous PSRAM is deselected, or its output enable is high.	
F-WE#	Input	**FLASH WRITE ENABLE:** Flash-specific signal; low-true input. When low, F-WE# enables Write operations for the enabled flash die. Address and data are latched on the rising edge of F-WE#.	
R-WE#	Input	**RAM WRITE ENABLE:** PSRAM- and SRAM-specific signal; low-true input. When low, R-WE# enables Write operations for the selected memory die. Data is latched on the rising edge of R-WE#.	1
F-WP[2:1]#	Input	**FLASH WRITE PROTECT:** Flash-specific signals; low-true inputs. When low, F-WP# enables the Lock-Down mechanism. When high, F-WP# overrides the Lock-Down function, enabling locked-down blocks to be unlocked with the Unlock command. • F-WP1# is dedicated to flash die #1. • F-WP2# is common to all other flash dies, if present. Otherwise it is RFU. • For NOR/NAND stacked device, F-WP1# selects all NOR dies, while F-WP2# selects all NAND dies.	
F-DPD	Input	**FLASH DEEP POWER-DOWN:** Flash-specific signal; configurable-true input. When enabled in the ECR, F-DPD is used to enter and exit Deep Power-Down mode.	
N-CLE	Input	**NAND COMMAND LATCH ENABLE:** NAND-specific signal; high-true input. When high, N-CLE enables commands to be latched on the rising edge of N-WE#.	1

Table 4. Signal Descriptions for x16C / x16C AD-Mux Ballout (Sheet 3 of 4)

Symbol	Type	Signal Descriptions	Notes
N-ALE	Input	**NAND ADDRESS LATCH ENABLE:** NAND-specific signal; high-true input. When high, N-ALE enables addresses to be latched on the rising edge of N-WE#.	1
N-RE#	Input	**NAND READ ENABLE:** NAND-specific signal; low-true input. When low, N-RE# enables the output drivers of the selected NAND die. When high, N-RE# disables the output drivers of the selected NAND die and places the output drivers in High-Z.	1,2
N-RY/BY#	Output	**NAND READY/BUSY:** NAND-specific signal; low-true output. When low, N-RY/BY# indicates the NAND is busy performing a Read, Program, or Erase operation. When high, N-RY/BY# indicates the NAND device is ready.	1
N-WE#	Input	**NAND WRITE ENABLE:** NAND-specific signal; low-true input. When low, N-WE# enables Write operations for the enabled NAND die.	1,4
P-CRE	Input	**PSRAM CONTROL REGISTER ENABLE:** Synchronous PSRAM-specific signal; high-true input. When high, P-CRE enables access to the Refresh Control Register (P-RCR) or Bus Control Register (P-BCR). When low, P-CRE enables normal Read or Write operations.	1,3
P-MODE#	Input	**PSRAM MODE#:** Asynchronous only PSRAM-specific signal; low-true input. When low, P-MODE# enables access to the configuration register, and to enter or exit Low-Power mode. When high, P-MODE# enables normal Read or Write operations.	1,3
P[2:1]-CS#	Input	**PSRAM CHIP SELECT:** PSRAM-specific signal; low-true input. When low, P-CS# selects the associated PSRAM memory die. When high, P-CS# deselects the associated PSRAM die. PSRAM die power is reduced to standby levels, and its data and WAIT outputs are placed in a High-Z state. • P1-CS# is dedicated to PSRAM die #1. • P2-CS# IS dedicated to PSRAM die #2. Otherwise, any unused PSRAM chip select should be treated as RFU.	1
S-CS1# S-CS2	Input	**SRAM CHIP SELECTS:** SRAM-specific signals; S-CS1# low-true input, S-CS2 high-true input. When both S-CS1# and S-CS2 are asserted, the SRAM die is selected. When either S-CS1# or S-CS2 is deasserted, the SRAM die is deselected.	1,4
R-UB# R-LB#	Input	**RAM UPPER/LOWER BYTE ENABLES:** PSRAM- and SRAM-specific signals; low-true inputs. When low, R-UB# enables DQ[15:8] and R-LB# enables DQ[7:0] during PSRAM or SRAM Read and Write cycles. When high, R-UB# masks DQ[15:8] and R-LB# masks DQ[7:0].	1
Power Signals			
F-VPP	Power	**FLASH PROGRAM/ERASE VOLTAGE:** Flash specific. F-VPP supplies program or erase power to the flash die.	
F[2:1]-VCC	Power	**FLASH CORE POWER SUPPLY:** Flash specific. F[2:1]-VCC supplies the core power to the flash die. • For NOR/NAND stacked device, F1-VCC is dedicated for all NOR dies, F2-VCC is dedicated for all NAND dies.	
VCCQ	Power	**I/O POWER SUPPLY:** Global device I/O power. VCCQ supplies the device input/output driver voltage.	
P-VCC	Power	**PSRAM CORE POWER SUPPLY:** PSRAM specific. P-VCC supplies the core power to the PSRAM die.	1
S-VCC	Power	**SRAM POWER SUPPLY:** SRAM specific. S-VCC supplies the core power to the SRAM die.	1

Table 4. Signal Descriptions for x16C / x16C AD-Mux Ballout (Sheet 4 of 4)

Symbol	Type	Signal Descriptions	Notes
VSS	Ground	**DEVICE GROUND:** Global ground reference for all signals and power supplies. Connect all VSS balls to system ground. Do not float any VSS connections.	
DU	—	**DO NOT USE:** This ball should not be connected to any power supplies, signals, or other balls. This ball can be left floating.	
RFU	—	**RESERVED for FUTURE USE:** Reserved by Intel for future device functionality and enhancement. This ball must be left floating.	

Notes:
1. Only available on stacked device combinations with NAND, SRAM, and/or LPSDRAM die. Otherwise treated as RFU.
2. F2-OE# and N-RE# share the same package ball at location H9. Only one signal function is available, depending on the stacked device combination.
3. P-CRE and P-MODE# share the same package ball at location K9. Only one signal function is available, depending on the stacked device combination.
4. S-CS1# and N-WE# share the same package ball at location J2. Only one signal function is available, depending on the stacked device combination.

5.0 Maximum Ratings and Operating Conditions

5.1 Absolute Maximum Ratings

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only.

NOTICE: This document contains information available at the time of its release. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

Table 5. Absolute Maximum Ratings

Parameter	Min	Max	Unit	Conditions	Notes
Temperature under Bias Expanded	–30	+85	°C	—	—
Storage Temperature	–65	+125	°C	—	—
F-VCC Voltage	–2.0	V_{CCQ} (max) + 2.0	V	—	1,2
VCCQ	–2.0	V_{CCQ} (max) + 2.0	V	—	1,3
Voltage on any input/output signal (except VCC, VCCQ, and VPP)	–2.0	V_{CCQ} (max) + 2.0	V	—	1,3
F-VPP Voltage	–2.0	+11.5	V	—	1,3
I_{SH} Output Short Circuit Current	—	100	mA	—	4
V_{PPH} Time	—	80	Hours		5
Block Program/Erase Cycles: Main and EFA Blocks	100,000	—	Cycles	F-VPP = V_{CC} or F-VPP = V_{PPH}	5

Notes:
1. Voltage is referenced to V_{SS}.
2. During signal transitions, minimum DC voltage may undershoot to –2.0 V for periods < 20 ns; maximum DC voltage may overshoot to V_{CC} (max) + 2.0 V for periods < 20 ns.
3. During signal transitions, minimum DC voltage may undershoot to –1.0 V for periods < 20 ns; maximum DC voltage may overshoot to V_{CCQ} (max) + 1.0 V for periods < 20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. Operation beyond this limit may degrade performance.

5.2 Operating Conditions

Warning: Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Table 6. Operating Conditions

Symbol	Description	Min	Max	Unit	Conditions
T_C	Operating Temperature (Case Temperature)	–30	+85	°C	—
V_{CC}	VCC Supply Voltage	+1.7	+2.0	V	—
V_{CCQ}	I/O Supply Voltage	+1.7	+2.0	V	—
V_{PPL}	Programming Voltage (Logic Level)	+0.9	+2.0	V	—
V_{PPH}	Factory Programming Voltage (High Level)	+8.5	+9.5	V	—

6.0 Electrical Characteristics

6.1 DC Current Specifications

Table 7. DC Current Specifications (Sheet 1 of 2)

Sym	Parameter		Density	1.7 V – 2.0 V		Unit	Test Conditions	Notes
				Typ	Max			
I_{LI}	Input Load Current			—	±1	µA	$V_{CC} = V_{CC}$ Max $V_{CCQ} = V_{CCQ}$ Max $V_{IN} = V_{CCQ}$ or V_{SS}	1
I_{LO}	Output Leakage Current			—	±1	µA	$V_{CC} = V_{CC}$ Max $V_{CCQ} = V_{CCQ}$ Max $V_{IN} = V_{CCQ}$ or V_{SS}	
I_{CCS}	V_{CC} Standby		256-Mb 512-Mb	35 50	95 120	µA	$V_{CC} = V_{CC}$Max $V_{CCQ} = V_{CCQ}$Max CE# = V_{CCQ} RST# = V_{CCQ} or GND (for I_{CCS}) WP# = V_{IH}	1,2
I_{CCAPS}	APS		256-Mb 512-Mb	35 50	95 120	µA	$V_{CC} = V_{CC}$ Max $V_{CCQ} = V_{CCQ}$ Max CE# = V_{SSQ} RST# = V_{CCQ} All inputs are at rail to rail (V_{CCQ} or V_{SSQ}).	—
I_{DPD}	DPD		256 Mbit 512 Mbit	2	30	µA	$V_{CC} = V_{CC}$ Max $V_{CCQ} = V_{CCQ}$ Max CE# = V_{CCQ} RST# = V_{CCQ} ECR[15] = V_{CCQ} DPD = V_{CCQ} or V_{SSQ} All inputs are at rail to rail (V_{CCQ} or V_{SSQ}).	8
I_{CCR}	Average V_{CC} Read: Asynchronous Single Word Read f = 5 MHz, (1 CLK)	—	256 Mbit 512 Mbit	25	30	mA	$V_{CC} = V_{CC}$MAX CE# = V_{IL} OE# = V_{IH} Inputs: V_{IL} or V_{IH}	1,3, 4,5
I_{CCR}	Average V_{CC} Read: Page Mode Read f = 13 MHz, (17 CLK)	16 Word	256 Mbit 512 Mbit	11	15	mA	$V_{CC} = V_{CC}$MAX CE# = V_{IL} OE# = V_{IH} Inputs: V_{IL} or V_{IH}	1,3, 4,5
I_{CCR}	Average V_{CC} Read: Synchronous Burst Read f = 66 MHz, LC = 7	Burst = 8 Word	256 Mbit 512 Mbit	22	32	mA	$V_{CC} = V_{CC}$MAX CE# = V_{IL} OE# = V_{IH} Inputs: V_{IL} or V_{IH}	1,3, 4,5
		Burst = 16 Word	256 Mbit 512 Mbit	19	26	mA		
		Continuous	256 Mbit 512 Mbit	25	34	mA		

Table 7. DC Current Specifications (Sheet 2 of 2)

Sym	Parameter		Density	1.7 V – 2.0 V		Unit	Test Conditions	Notes
				Typ	Max			
I_{CCR}	Average V_{CC} Read: Synchronous Burst Read f = 108 MHz, LC = 10	Burst = 8 Word	256 Mbit 512 Mbit	26	36	mA	$V_{CC} = V_{CC}MAX$ CE# = V_{IL} OE# = V_{IH} Inputs: V_{IL} or V_{IH}	1,3, 4,5
		Burst = 16 Word	256 Mbit 512 Mbit	23	30	mA		
		Continuous	256 Mbit 512 Mbit	30	42	mA		
I_{CCR}	Average V_{CC} Read: Synchronous Burst Read f = 133 MHz, LC = 13	Burst = 8 Word	256 Mbit 512 Mbit	26	35	mA	$V_{CC} = V_{CC}MAX$ CE# = V_{IL} OE# = V_{IH} Inputs: V_{IL} or V_{IH}	1,3, 4,5
		Burst = 16 Word	256 Mbit 512 Mbit	24	33	mA		
		Continuous	256 Mbit 512 Mbit	33	46	mA		
I_{CCW}, I_{CCE} I_{CCBC}	V_{CC} Program V_{CC} Erase V_{CC} Blank Check			35	50	mA	$V_{PP} = V_{PPL}$ or $V_{PP} = V_{PPH}$, program/erase in progress	1,3,4, 5,7
I_{CCWS}, I_{CCES}	V_{CC} Program Suspend V_{CC} Erase Suspend		256-Mb 512-Mb	35 50	95 120	µA	CE# = V_{CCQ}; suspend in progress	1,3,6
I_{PPS}, I_{PPWS}, I_{PPES}	V_{PP} Standby V_{PP} Program Suspend V_{PP} Erase Suspend			0.2	5	µA	$V_{PP} = V_{PPL}$; suspend in progress	3
I_{PPR}	V_{PP} Read			2	15	µA	$V_{PP} \leq V_{CC}$	3
I_{PPW}	V_{PP} Program			0.05	0.1	mA	$V_{PP} = V_{PPL} = V_{PPH}$, program in progress	3
I_{PPE}	V_{PP} Erase			0.05	0.1	mA	$V_{PP} = V_{PPL} = V_{PPH}$, erase in progress	3
I_{PPBC}	V_{PP} Blank Check			0.05	0.1	mA	$V_{PP} = V_{PPL} = V_{PPH}$, blank check in progress	3

NOTES:

1. All currents are RMS unless noted. Typical values at typical V_{CC}, T_C = +25°C.
2. I_{CCS} is the average current measured over any 5 ms time interval 5 µs after CE# is deasserted.
3. Sampled, not 100% tested.
4. V_{CC} read + program current is the sum of V_{CC} read and V_{CC} program currents.
5. V_{CC} read + erase current is the sum of V_{CC} read and V_{CC} erase currents.
6. I_{CCES} is specified with the device deselected. If device is read while in erase suspend, current is I_{CCES} plus I_{CCR}
7. I_{CCW}, I_{CCE} measured over typical or max times specified in Section 7.4, “Program and Erase Characteristics” on page 59
8. I_{DPD} is the current measured 40 µs after entering DPD state by asserting DPD.

6.2 DC Voltage Specifications

Table 8. DC Voltage Specifications

Sym	Parameter	V_{CCQ}	1.7 V – 2.0 V		Unit	Test Condition	Notes
			Min	Max			
V_{IL}	Input Low Voltage		0	0.4	V	—	1
V_{IH}	Input High Voltage		V_{CCQ} –0.4	V_{CCQ}		—	—
V_{OL}	Output Low Voltage		—	0.1		V_{CC} = V_{CC}MIN V_{CCQ} = V_{CCQ}MIN I_{OL} = 100 µA	—
V_{OH}	Output High Voltage		V_{CCQ} –0.1	—		V_{CC} = V_{CC}MIN V_{CCQ} = V_{CCQ}MIN I_{OH} = –100 µA	—
V_{PPLK}	V_{PP} Lock-Out Voltage		—	0.4		—	2
V_{LKO}	V_{CC} Lock Voltage		1.0	—		—	—
V_{LKOQ}	V_{CCQ} Lock Voltage		0.9	—		—	—

Notes:
1. During signal transitions, voltage can undershoot to –1.0 V and overshoot to maximum V_{CCQ}+1.0V for durations of <2 ns.
2. $V_{PP} \leq V_{PPLK}$ inhibits erase and program operations. Do not use V_{PPL} and V_{PPH} outside their valid ranges.

6.3 Capacitance

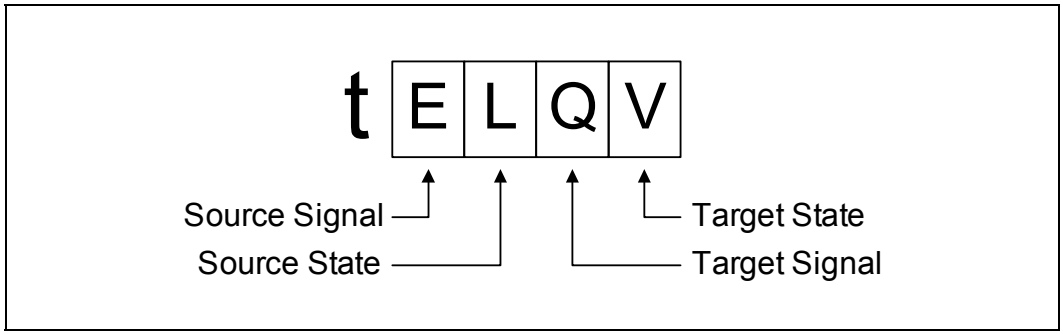
Table 9. Capacitance

Symbol	Parameter	Min	Typ	Max	Unit	Condition	Note
C_{IN}	Input Capacitance (Address, CLK, CE#, OE#, ADV#, WE#, WP#, DPD and RST#)	2	4	6	pF	V_{IN} = 0.0 - 2.0 V	1,2
C_{OUT}	Output Capacitance (Data and WAIT)	2	5	6		V_{OUT} = 0.0 - 2.0 V	

NOTES:
1. T_C = +25°C, f = 1 MHz.
2. Sampled, not 100% tested.

7.0 NOR Flash AC Characteristics

Timing symbols used in the timing diagrams within this document conform to the following convention:

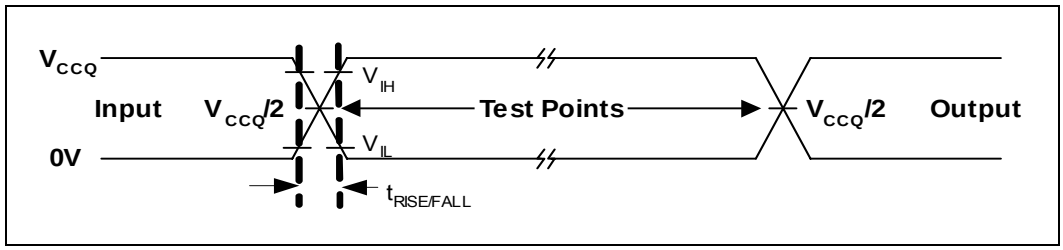


Signal	Code	State	Code
Address	A	High	H
Data - Read	Q	Low	L
Data - Write	D	High-Z	Z
Chip Enable (CE#)	E	Low-Z	X
Output Enable (OE#)	G	Valid	V
Write Enable (WE#)	W	Invalid	I
Address Valid (ADV#)	V		
Reset (RST#)	P		
Clock (CLK)	C		
WAIT	T		

Note: Exceptions to this convention include tACC and tAPA. tACC is a generic timing symbol that refers to the aggregate initial-access delay as determined by tAVQV, tELQV, and tGLQV (whichever is satisfied last) of the flash device. tAPA is specified in the flash device's data sheet, and is the address-to-data delay for subsequent page-mode reads.

7.1 AC Test Conditions

Figure 11. AC Input/Output Reference Waveform

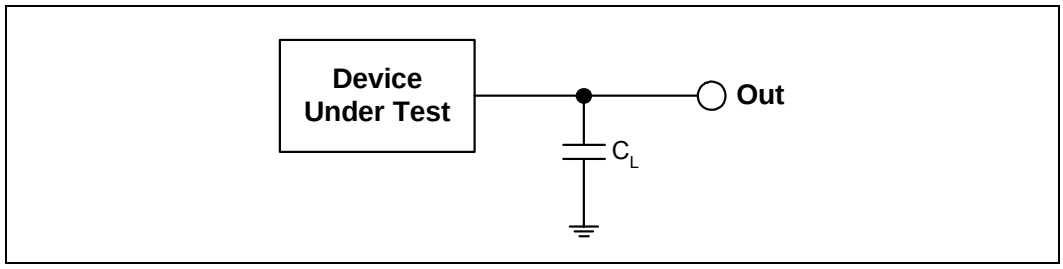


Note: AC test inputs are driven at V_{CCQ} for Logic '1' and 0.0 V for Logic '0'. Input/output timing begins/ends at $V_{CCQ}/2$.

Table 10. AC Input Requirements

Symbol	Parameter	Frequency	Min	Max	Unit	Condition
$t_{RISE/FALL}$	Inputs rise/fall time (Address, CLK, CE#, OE#, ADV#, WE#, WP#)	133MHz, 108MHz	0.3	1.2	ns	V_{IL} to V_{IH} or V_{IH} to V_{IL}
		@66MHz	0	3		
t_{ASKW}	Address-Address skew		0	3		At $V_{CCQ}/2$

Figure 12. Transient Equivalent Testing Load Circuit

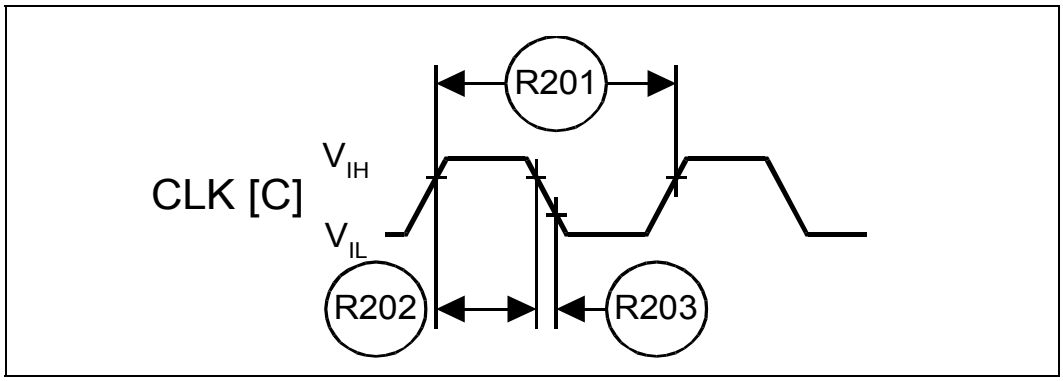


NOTES:
1. See the following table for component values.
2. Test configuration component value for worst case speed conditions.
3. C_L includes jig capacitance.

Table 11. Test configuration component value for worst case speed conditions

Test Configuration	C_L (pF)
1.7 V Standard Test	30
2.0 V Standard Test	30

Figure 13. Clock Input AC Waveform



7.2 Read Specifications

The M18 device includes read specifications for the following speeds and voltage levels:

- 512-Mbit device: 108 MHz, V_{CCQ} = 1.7 V to 2.0 V
- 256-Mbit device: 133 MHz, V_{CCQ} = 1.7 V to 2.0 V

Devices which support frequencies up to 133 MHz must meet additional timing specifications for synchronous reads (for address latching with CLK) as listed in Table 13.

Table 12. AC Read, 512 Mbit, 108 MHz, V_{CCQ} = 1.7 V to 2.0 V (Sheet 1 of 2)

Nbr.	Symbol	Parameter[1]	–96		Units	Notes
			Min	Max		
Asynchronous Specifications						
R1	t_{AVAV}	Read cycle time	96	—	ns	—
R2	t_{AVQV}	Address to output valid	—	96	ns	—
R3	t_{ELQV}	CE# low to output valid	—	96	ns	—
R4	t_{GLQV}	OE# low to output valid	—	20	ns	2
R5	t_{PHQV}	RST# high to output valid	—	150	ns	—
R6	t_{ELQX}	CE# low to output in low-Z	0	—	ns	3
R7	t_{GLQX}	OE# low to output in low-Z	0	—	ns	2,3
R8	t_{EHQZ}	CE# high to output in high-Z	—	9	ns	3
R9	t_{GHQZ}	OE# high to output in high-Z	—	9	ns	
R10	t_{OH}	Output hold from first occurring address, CE#, or OE# change	0	—	ns	
R11	t_{EHEL}	CE# pulse width high	9	—	ns	—
R12	t_{ELTV}	CE# low to WAIT valid	—	11	ns	—
R13	t_{EHTZ}	CE# high to WAIT high Z	—	9	ns	3
R14	t_{GHTV}	OE# high to WAIT valid (AD-Mux only)	—	7	ns	—

Table 12. AC Read, 512 Mbit, 108 MHz, V_{CCQ} = 1.7 V to 2.0 V (Sheet 2 of 2)

Nbr.	Symbol	Parameter[1]	–96		Units	Notes
			Min	Max		
R15	t_{GLTV}	OE# low to WAIT valid	—	7	ns	—
R16	t_{GLTX}	OE# low to WAIT in low-Z	0	—	ns	3
R17	t_{GHTZ}	OE# low to WAIT in high-Z (non-mux only)	0	9	ns	3
Latching Specifications						
R101	t_{AVVH}	Address setup to ADV# high	5	—	ns	—
R102	t_{ELVH}	CE# low to ADV# high	9	—	ns	
R103	t_{VLQV}	ADV# low to output valid		96	ns	
R104	t_{VLVH}	ADV# pulse width low	7	—	ns	
R105	t_{VHVL}	ADV# pulse width high	7	—	ns	
R106	t_{VHAX}	Address hold from ADV# high	5	—	ns	4
R107	t_{VHGL}	ADV# high to OE# low (AD-Mux only)	7	—	ns	—
R108	t_{APA}	Page address access (non-mux only)	—	15	ns	
R111	t_{PHVH}	RST# high to ADV# high	30	—	ns	
Clock Specifications						
R200	f_{CLK}	CLK frequency	—	108	MHz	—
R201	t_{CLK}	CLK period	9.26	—	ns	
R202	$t_{CH/CL}$	CLK high/low time	3.5	—	ns	
R203	$t_{FCLK/RCLK}$	CLK fall/rise time	0.3	1.2	ns	
Synchronous Specifications						
R301	t_{AVCH}	Address setup to CLK high	5	—	ns	—
R302	t_{VLCH}	ADV# low setup to CLK high	5	—	ns	
R303	t_{ELCH}	CE# low setup to CLK high	5	—	ns	
R304	t_{CHQV}	CLK to output valid	—	7	ns	
R305	t_{CHQX}	Output hold from CLK high	2	—	ns	—
R306	t_{CHAX}	Address hold from CLK high	5	—	ns	4
R307	t_{CHTV}	CLK high to WAIT valid	—	7	ns	—
R311	t_{CHVL}	CLK high to ADV# Setup	0	—	ns	—
R312	t_{CHTX}	WAIT hold from CLK	2	—	ns	—

NOTES:

1. See Figure 11, "AC Input/Output Reference Waveform" on page 35 for timing measurements and maximum allowable input slew rate.
2. OE# may be delayed by up to $t_{ELQV} - t_{GLQV}$ after CE#'s falling edge without impact to t_{ELQV}.
3. Sampled, not 100% tested.
4. Address hold in synchronous burst mode is t_{CHAX} or t_{VHAX}, whichever timing specification is satisfied first.

Table 13. AC Read, 256 Mbit, 133 MHz, V_{CCQ} = 1.7 V to 2.0 V (Sheet 1 of 2)

Nbr.	Symbol	Parameter[1]	–96		Units	Notes
			Min	Max		
Asynchronous Specifications						
R1	t_{AVAV}	Read cycle time	96	—	ns	—
R2	t_{AVQV}	Address to output valid	—	96	ns	—
R3	t_{ELQV}	CE# low to output valid	—	96	ns	—
R4	t_{GLQV}	OE# low to output valid	—	7	ns	2
R5	t_{PHQV}	RST# high to output valid	—	150	ns	—
R6	t_{ELQX}	CE# low to output in low-Z	0	—	ns	3
R7	t_{GLQX}	OE# low to output in low-Z	0	—	ns	2,3
R8	t_{EHQZ}	CE# high to output in high-Z	—	7	ns	3
R9	t_{GHQZ}	OE# high to output in high-Z	—	7	ns	
R10	t_{OH}	Output hold from first occurring address, CE#, or OE# change	0	—	ns	
R11	t_{EHEL}	CE# pulse width high	7	—	ns	—
R12	t_{ELTV}	CE# low to WAIT valid	—	8	ns	—
R13	t_{EHTZ}	CE# high to WAIT high Z	—	7	ns	3
R14	t_{GHTV}	OE# high to WAIT valid (AD-Mux only)	—	5.5	ns	—
R15	t_{GLTV}	OE# low to WAIT valid	—	5.5	ns	—
R16	t_{GLTX}	OE# low to WAIT in low-Z	0	—	ns	3
R17	t_{GHTZ}	OE# high to WAIT in high-Z (non-mux only)	0	7	ns	3
Latching Specifications						
R101	t_{AVVH}	Address setup to ADV# high	5	—	ns	—
R102	t_{ELVH}	CE# low to ADV# high	7	—	ns	
R103	t_{VLQV}	ADV# low to output valid		96	ns	
R104	t_{VLVH}	ADV# pulse width low	7	—	ns	
R105	t_{VHVL}	ADV# pulse width high	7	—	ns	
R106	t_{VHAX}	Address hold from ADV# high	5	—	ns	
R107	t_{VHGL}	ADV# high to OE# low (AD-Mux only)	2	—	ns	
R108	t_{APA}	Page address access (non-mux only)	—	15	ns	
R111	t_{PHVH}	RST# high to ADV# high	30	—	ns	
Clock Specifications						
R200	f_{CLK}	CLK frequency	—	133	MHz	—
R201	t_{CLK}	CLK period	7.5	—	ns	
R202	$t_{CH/CL}$	CLK high/low time	3.2	—	ns	
R203	$t_{FCLK/RCLK}$	CLK fall/rise time	0.3	1.2	ns	
Synchronous Specifications						

Table 13. AC Read, 256 Mbit, 133 MHz, V_{CCQ} = 1.7 V to 2.0 V (Sheet 2 of 2)

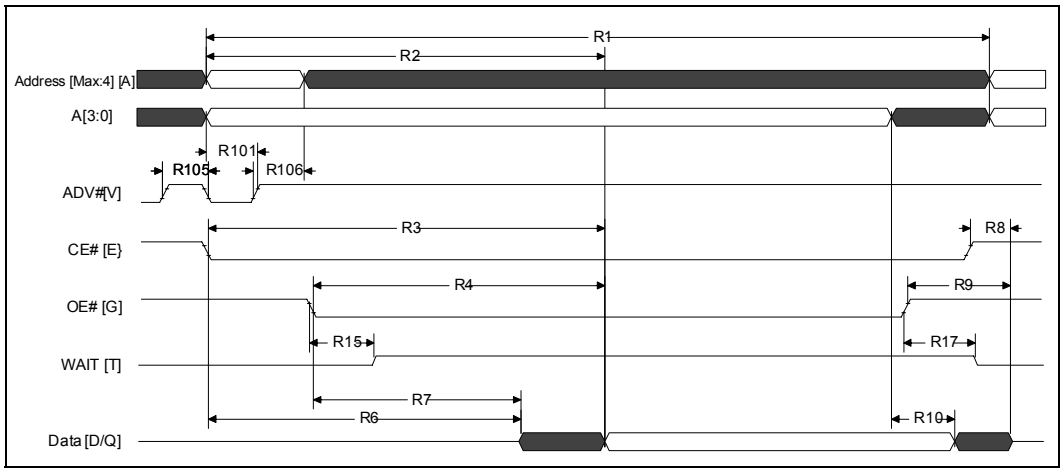
Nbr.	Symbol	Parameter[1]	–96		Units	Notes
			Min	Max		
R301	t_{AVCH}	Address setup to CLK high	2	—	ns	—
R302	t_{VLCH}	ADV# low setup to CLK high	2	—	ns	
R303	t_{ELCH}	CE# low setup to CLK high	2.5	—	ns	
R304	t_{CHQV}	CLK to output valid	—	5.5	ns	
R305	t_{CHQX}	Output hold from CLK high	2	—	ns	
R306	t_{CHAX}	Address hold from CLK high	2	—	ns	
R307	t_{CHTV}	CLK high to WAIT valid	—	5.5	ns	
R311	t_{CHVL}	CLK high to ADV# Setup	0	—	ns	
R312	t_{CHTX}	WAIT hold from CLK high	2	—	ns	
R313	t_{CHVH}	ADV# hold from CLK high	2	—	ns	
R314	t_{CHGL}	CLK to OE# low (AD-Mux only)	2	—	ns	
R315	t_{ACC}	Read access time from address latching clock	96	—	ns	
R316	t_{VLVH}	ADV# pulse width low for sync reads	1	2	clks	
R317	t_{VHCH}	ADV# high to CLK high	2	—	ns	

NOTES:

1. See Figure 11, “AC Input/Output Reference Waveform” on page 35 for timing measurements and maximum allowable input slew rate.
2. OE# may be delayed by up to $t_{ELQV} - t_{GLQV}$ after CE#’s falling edge without impact to t_{ELQV}.
3. Sampled, not 100% tested.

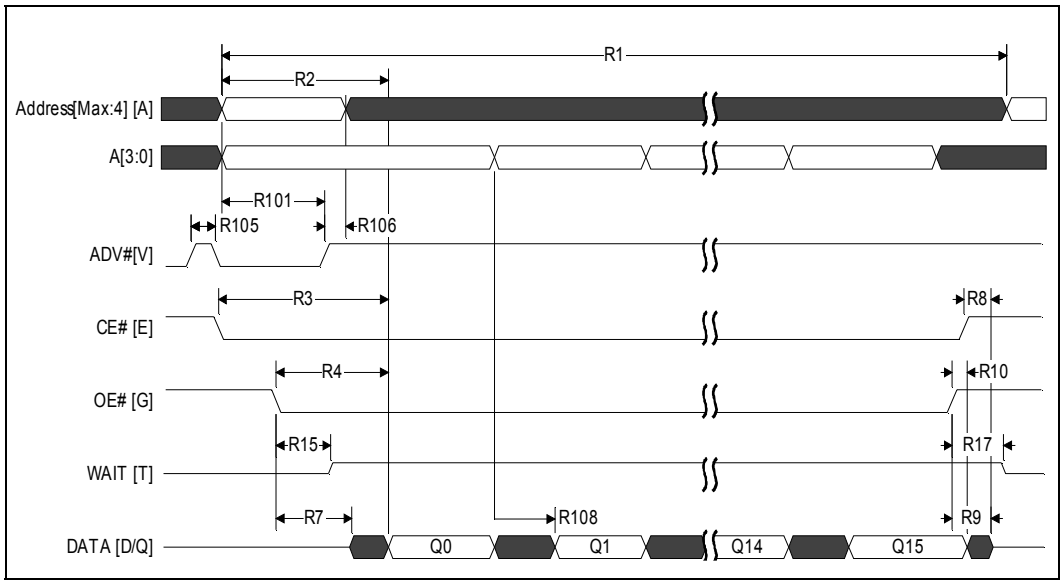
7.2.1 Timings: Non Mux Device, Asynchronous Read

Figure 14. Asynchronous Single-Word Read with ADV# Latch



Note: WAIT polarity in figure is low-true (RCR10 = 0, default). WAIT deasserted during asynchronous reads.

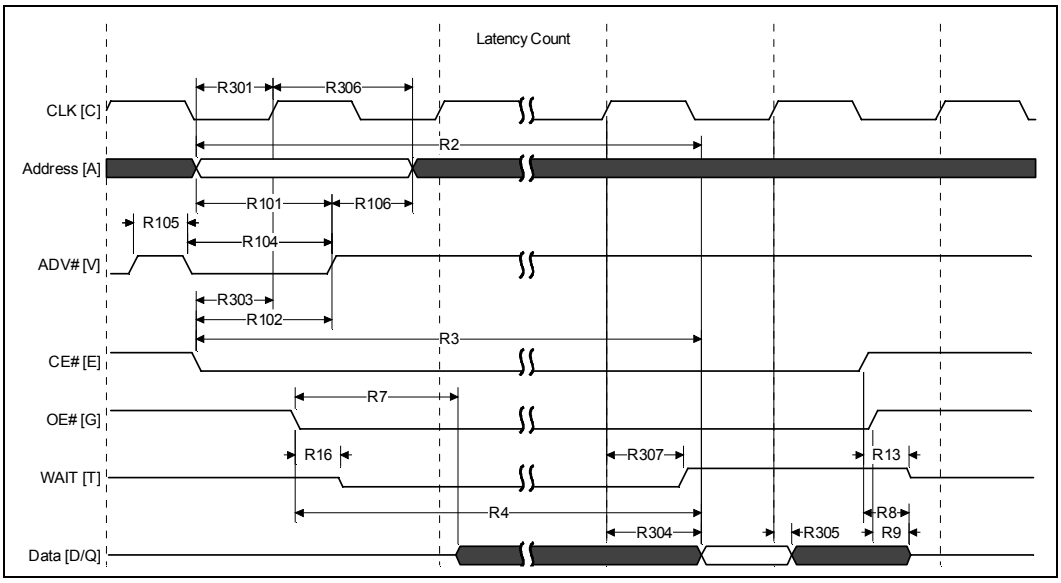
Figure 15. Asynchronous Page-Mode Read Timing



Note: WAIT polarity in figure is low-true (RCR10 = 0, default). WAIT deasserted during asynchronous reads.

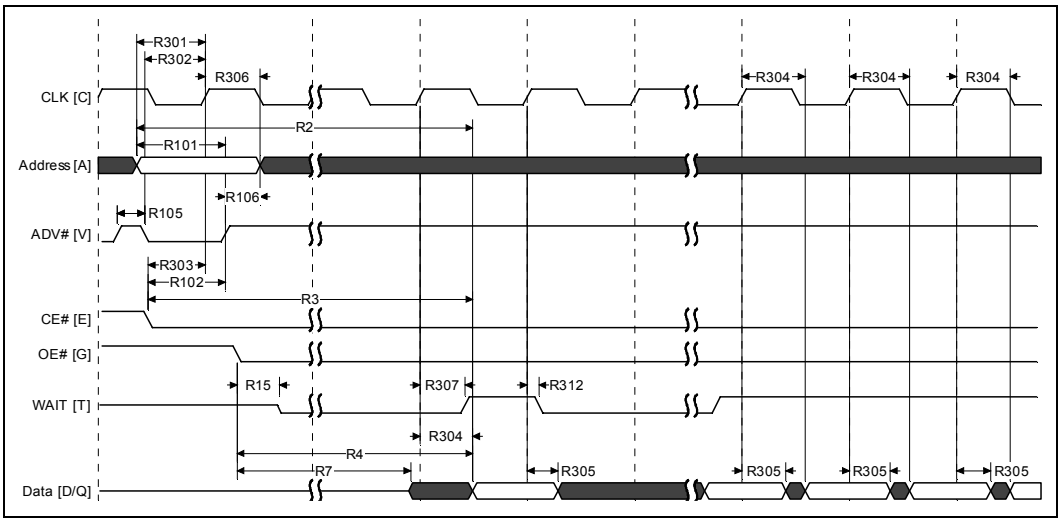
7.2.2 Timings: Non Mux Device, Synchronous Read 108 MHz, 512 Mb

Figure 16. Synchronous Single-Word Array or Non-array Read 108 MHz, 512 Mbit



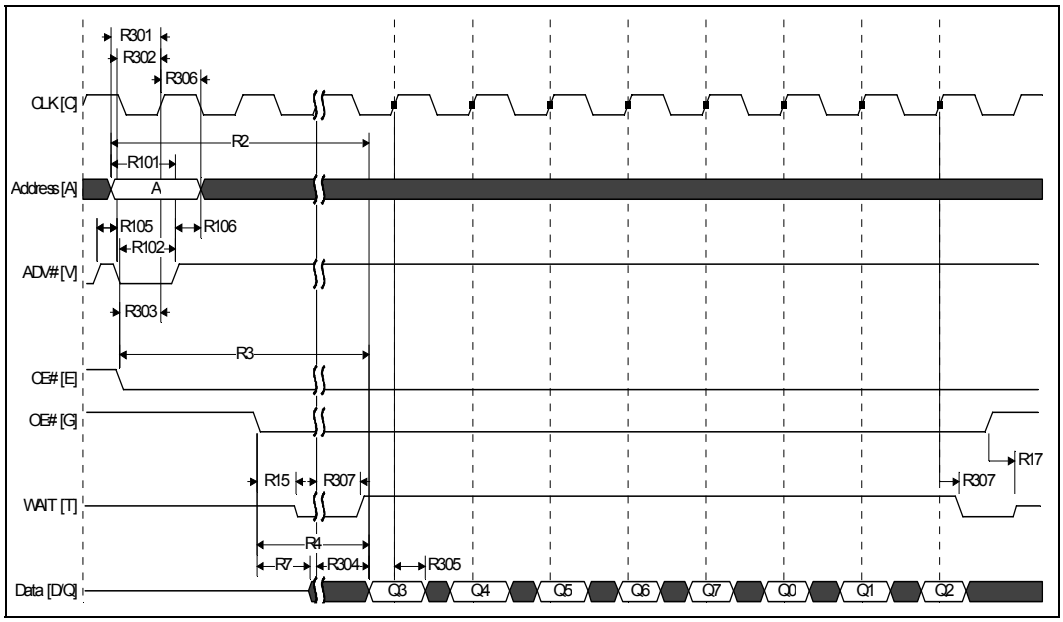
NOTES:
1. WAIT polarity in figure is low-true (RCR10 = 0, default)
2. This figure illustrates the case in which an n-word burst is initiated to the flash memory array and it is terminated by OE# and CE# deassertion after the first word in the burst.
3. Address latched on rising CLK edge after ADV# low.

Figure 17. Continuous Burst Read, showing an Output Delay at EOWL 108 MHz, 512 Mbit



Notes:
1. At the End of Word Line (EOWL); the delay incurred when a burst access crosses a 16-word boundary and the starting address is not 16-word boundary aligned.
2. WAIT polarity in figure is low-true (RCR10 = 0, default)
3. Address latched on rising CLK edge after ADV# low.

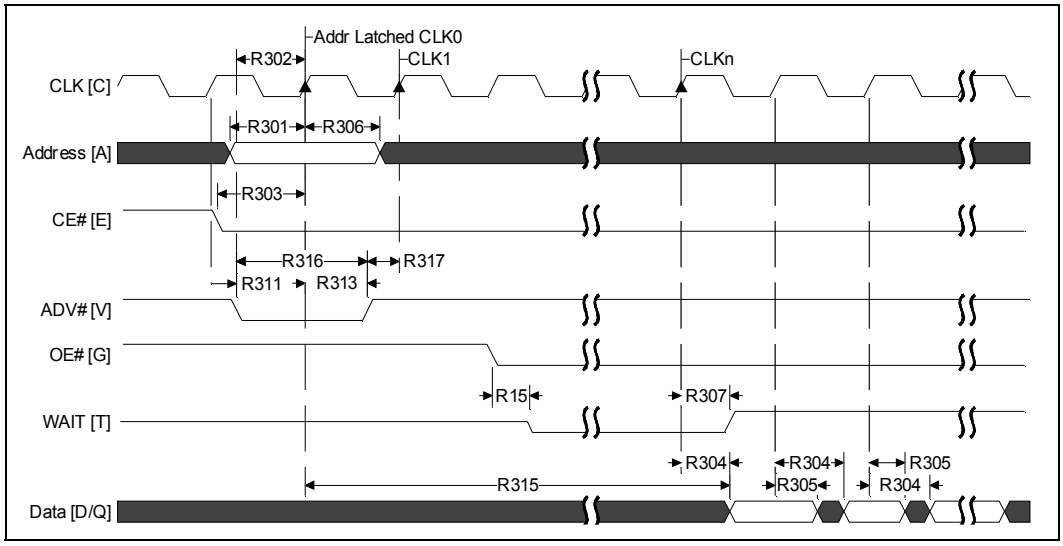
Figure 18. Synchronous Burst-Mode Unaligned Eight-Word Burst Read 108 MHz, 512 Mbit



NOTES:
1. WAIT polarity in figure is low-true (RCR10 = 0, default).
2. 8-word and 16-word burst are always wrap-only.
3. Address latched on rising CLK edge after ADV# low.

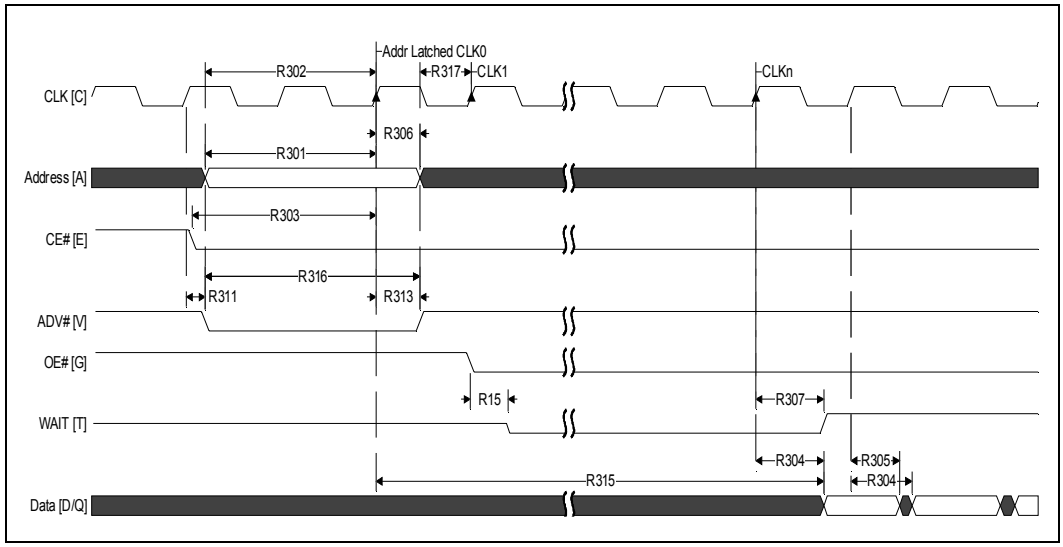
7.2.3 Timings: Non Mux Device, Synchronous Read 133 MHz, 256 Mb

Figure 19. Synchronous Array or Non-array Read 133 MHz, 256 Mb



NOTES:
1. Address is latched on first CLK edge after ADV# assertion, associated setup and hold timings shown.
2. WAIT polarity in figure is low-true (RCR10 = 0, default).

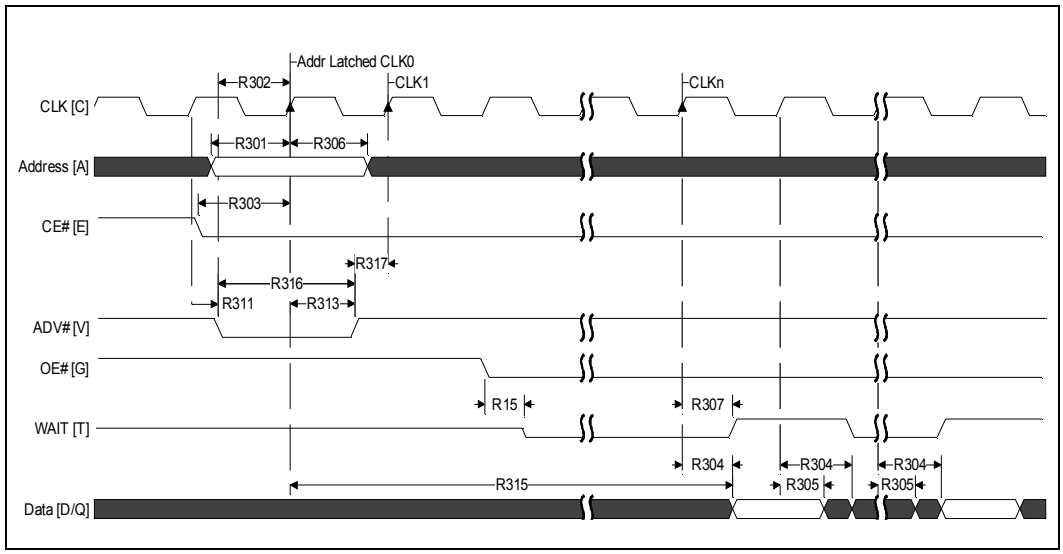
Figure 20. Synchronous Array or Non-array Read with ADV# Maximum Low Pulse Width 133 MHz, 256 Mb



NOTES:

1. Address is latched on the second rising CLK edge after ADV# assertion, associated setup and hold timing shown.
2. WAIT polarity in figure is low-true (RCR10 = 0, default).

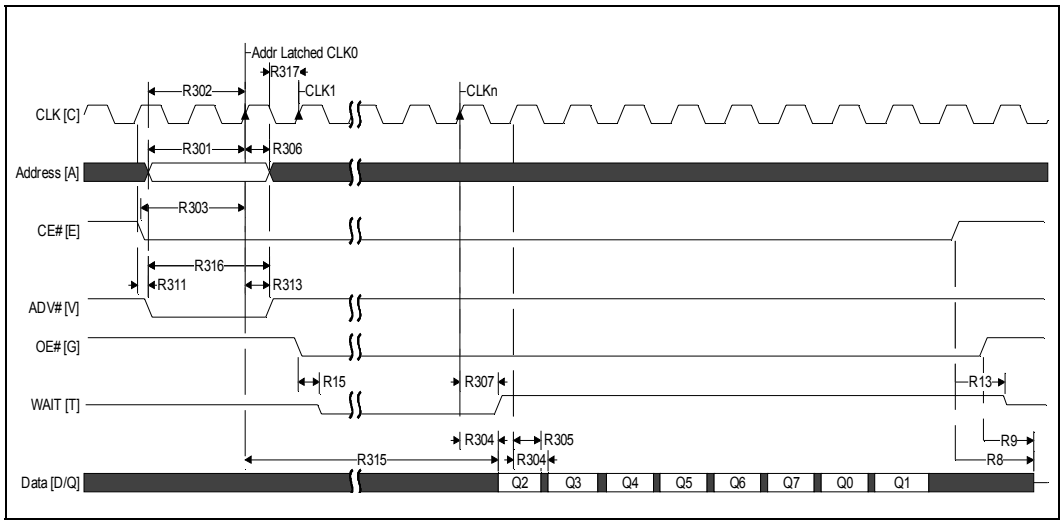
Figure 21. Continuous Burst Read, showing Output Delay at EOWL 133 MHz, 256 Mb



Notes:

1. At the End of Word Line (EOWL); the delay incurred when a burst access crosses a 16-word boundary and the starting address is not 16-word boundary aligned.
2. WAIT polarity in figure is low-true (RCR10 = 0, default).
3. Address is latched on the first rising CLK edge after ADV# assertion, associated setup and hold timing shown.

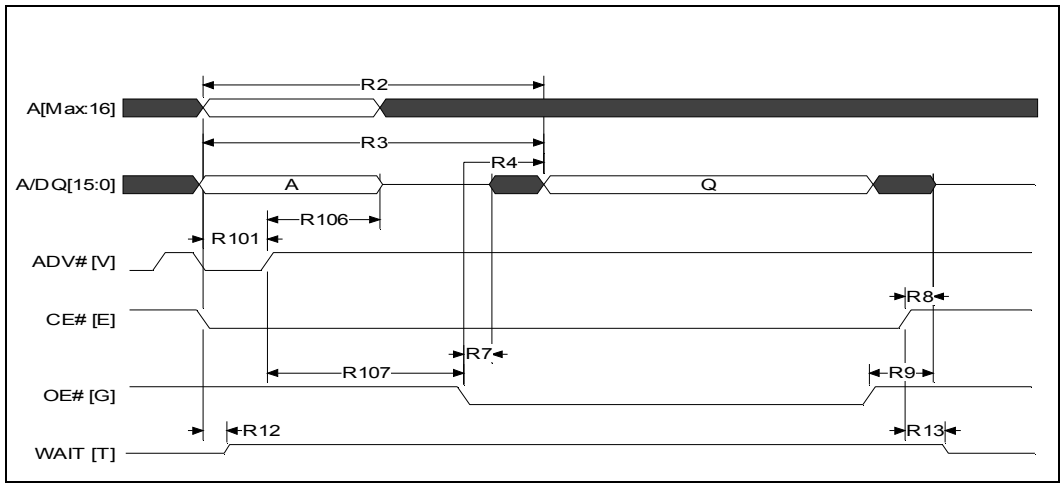
Figure 22. Synchronous Burst-Mode Unaligned Eight-Word Burst Read 133 MHz, 256 Mb



NOTES:
1. WAIT polarity in figure is low-true (RCR10 = 0, default).
2. 8-word and 16-word burst reads are always wrapped.
3. Address is latched on the second rising CLK edge after ADV# assertion, associated setup and hold timing shown.

7.2.4 Timings: AD-Mux Device, Asynchronous Read

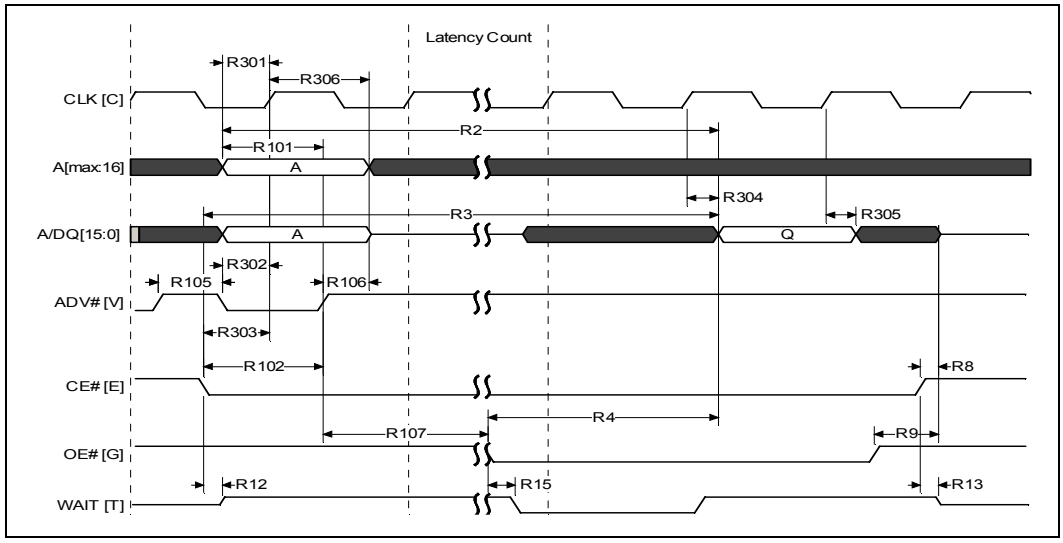
Figure 23. Asynchronous Word Read



Note: WAIT polarity in figure is low-true (RCR10 = 0, default). WAIT is deasserted during asynchronous reads.

7.2.5 Timings: AD-Mux Device, Synchronous Read 108 MHz, 512 Mb

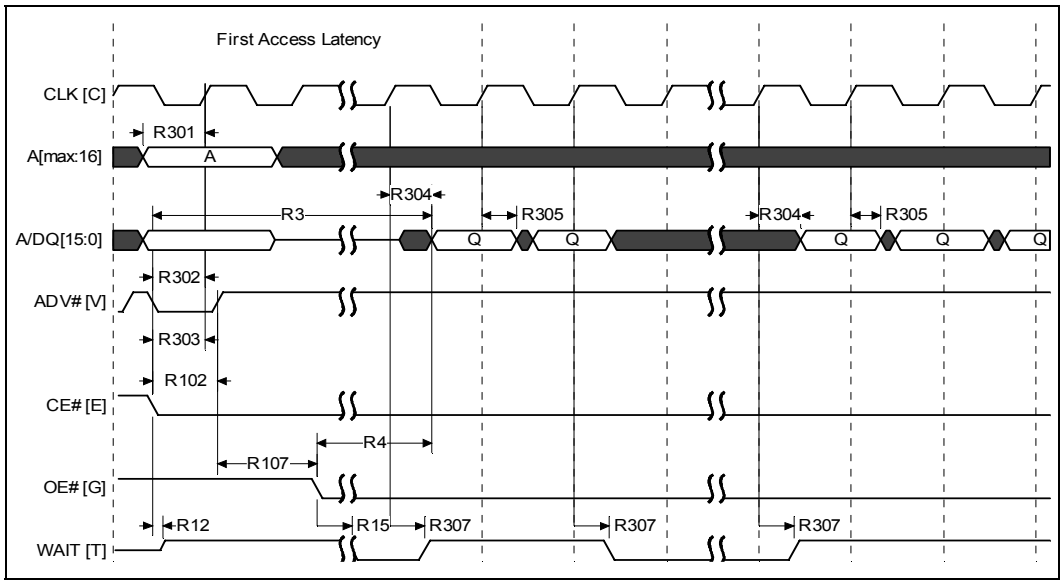
Figure 24. Synchronous Single-Word Array or Non-array Read 108 MHz, 512 Mbit



NOTES:

1. WAIT polarity in figure is low-true (RCR10 = 0, default)..
2. This figure illustrates the case in which an n-word burst is initiated to the flash memory array and it is terminated by OE# and CE# deassertion after the first word in the burst.
3. Address latched on first CLK edge after ADV# low.

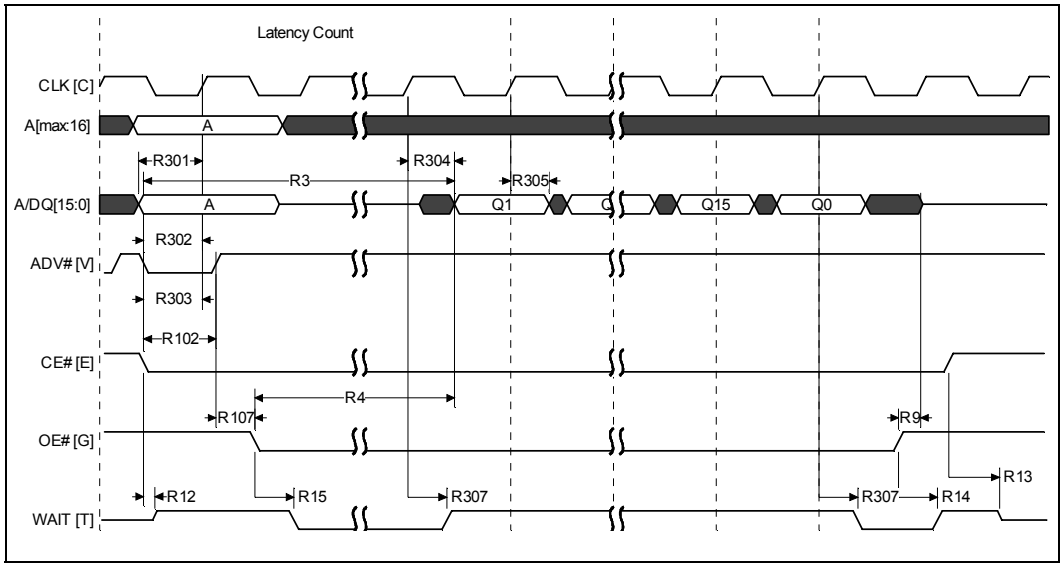
Figure 25. Continuous Burst Read, showing an Output Delay at EOWL 108 MHz, 512 Mbit



Notes:

1. At the End of Word Line (EOWL); the delay incurred when a burst access crosses a 16-word boundary and the starting address is not 16-word boundary aligned.
2. WAIT polarity in figure is low-true (RCR10 = 0, default).
3. Address latched on first CLK edge after ADV# low.

Figure 26. Synchronous Burst-Mode Unaligned 16-Word Burst Read 108 MHz, 512 Mbit

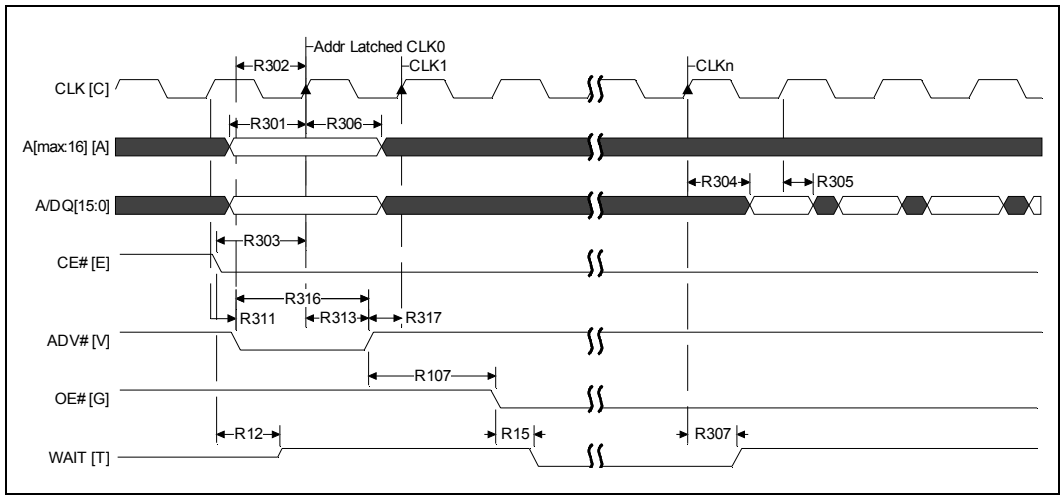


Notes:

1. WAIT polarity in figure is low-true (RCR10 = 0, default).
2. Address latched on first CLK edge after ADV# low.

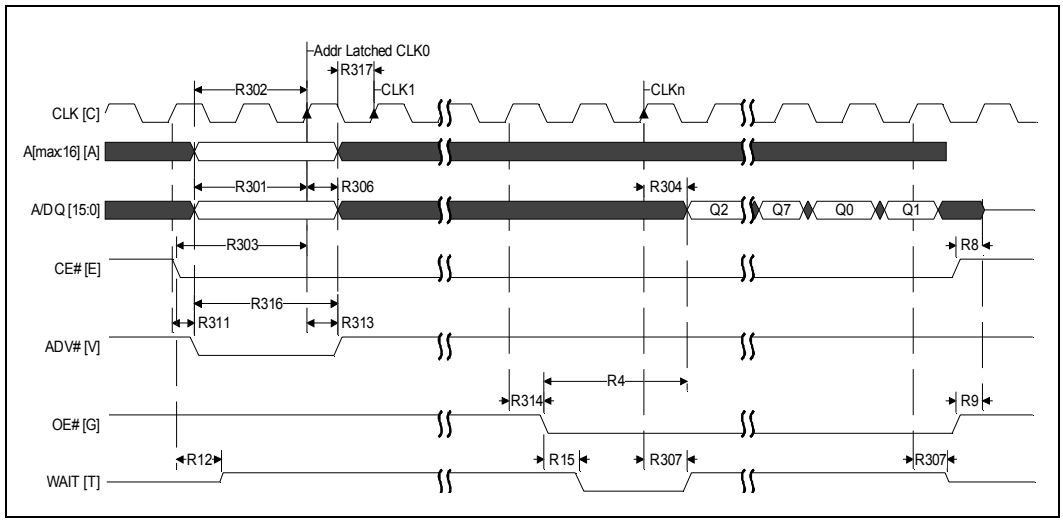
7.2.6 Timings: AD-Mux Device, Synchronous Read 133 MHz, 256 Mb

Figure 27. Synchronous Array or Non-array Read 133 MHz, 256 Mb



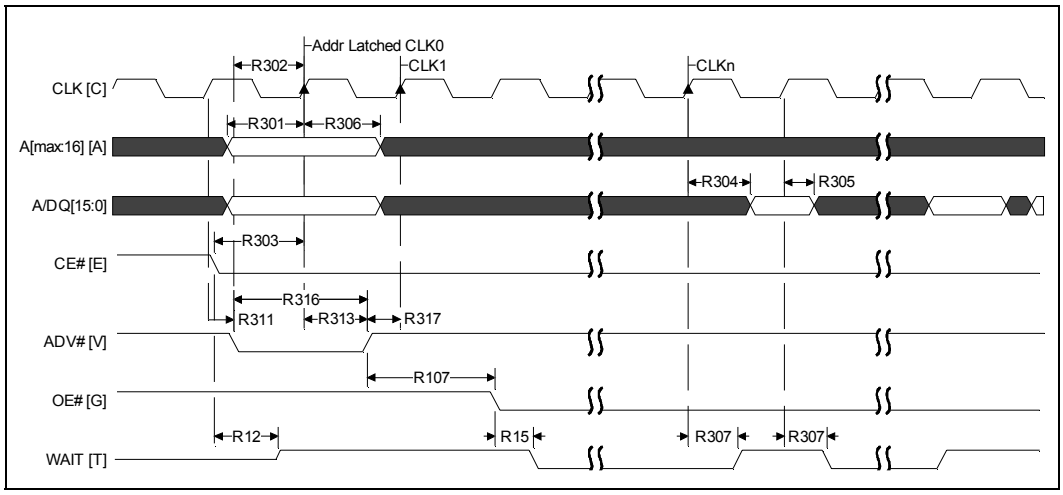
NOTES:
1. Address is latched on the first rising CLK edge after ADV# assertion, associated setup and hold timing shown.
2. WAIT polarity in figure is low-true (RCR10 = 0, default).

Figure 28. Synchronous Unaligned Eight-Word Burst Read with ADV# Maximum Low Pulse Width 133 MHz, 256 Mb



NOTES:
1. Address is latched on the second rising CLK edge after ADV# assertion, associated setup and hold timing shown.
2. WAIT polarity in figure is low-true (RCR10 = 0, default).
3. 8-word and 16-word burst reads are always wrapped.

Figure 29. Continuous Burst Read, showing an Output Delay at EOWL 133 MHz, 256 Mb



Notes:

1. At the End of Word Line (EOWL); the delay incurred when a burst access crosses a 16-word boundary and the starting address is not 16-word boundary aligned
2. WAIT polarity in figure is low-true (RCR10 = 0, default).
3. Address is latched on the first rising CLK edge after ADV# assertion, associated setup and hold timing shown.

7.3 Write Specifications

Table 14. AC Write Specifications

Nbr.	Symbol	Parameter (1, 2)	Min	Max	Units	Notes
W1	t_{PHWL}	RST# high recovery to WE# low	150	—	ns	1,2,3
W2	t_{ELWL}	CE# setup to WE# low	0	—	ns	1,2
W3	t_{WLWH}	WE# write pulse width low	40	—	ns	1,2,4
W4	t_{DVWH}	Data setup to WE# high	40	—	ns	1,2
W5	t_{AVWH}	Address setup to WE# high	40	—	ns	
W6	t_{WHEH}	CE# hold from WE# high	0	—	ns	
W7	t_{WHDX}	Data hold from WE# high	0	—	ns	
W8	t_{WHAX}	Address hold from WE# high (non-mux only)	0	—	ns	
W9	t_{WHWL}	WE# pulse width high	20	—	ns	1,2,5
W10	t_{VPWH}	VPP setup to WE# high	200	—	ns	1,2,3,7
W11	t_{QVVL}	VPP hold from Status read	0	—	ns	
W12	t_{QVBL}	WP# hold from Status read	0	—	ns	
W13	t_{BHWH}	WP# setup to WE# high	200	—	ns	
W14	t_{WHGL}	WE# high to OE# low	0	—	ns	1,2,8
W15	t_{VLWH}	ADV# low to WE# high (AD-Mux only)	55	—	ns	1,2
W16	t_{WHQV}	WE# high to read valid	t_{AVQV}+30	—	ns	1,2,3,9
Write to Synchronous Read Specifications						
W19	t_{WHCH}	WE# high to Clock high	15	—	ns	1,2,3,6
Bus Write with Active Clock Specifications						
W21	t_{VHWL}	ADV# high to WE# low	—	27	ns	1,2,10,11
W22	t_{CHWL}	Clock high to WE# low	—	27	ns	

NOTES:

1. Write timing characteristics during erase suspend are the same as write-only operations.
2. A write operation can be terminated with either CE# or WE#.
3. Sampled, not 100% tested.
4. Write pulse width low (t_{WLWH} or t_{ELEH}) is defined from CE# or WE# low (whichever occurs last) to CE# or WE# high (whichever occurs first). Hence, $t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$.
5. Write pulse width high (t_{WHWL} or t_{EHEL}) is defined from CE# or WE# high (whichever occurs first) to CE# or WE# low (whichever occurs last). Hence, $t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$).
6. t_{WHCH} must be met when transitioning from a write cycle to a synchronous burst read. In addition there must be a CE# toggle after WE# goes high.
7. VPP and WP# should be at a valid level until erase or program success is determined.
8. When doing a Read Status operation following any command that alters the Status Register data, W14 is 20ns.
9. Add 10ns if the write operations results in a RCR or block lock status change, for the subsequent read operation to reflect this change.
10. This specification is applicable only if the part is configured in synchronous mode and an active clock is running. Either t_{VHWL} or t_{CHWL} must be met depending on the whether the address is latched on ADV# or CLK.
11. These specifications are not applicable to 133 MHz devices.

7.3.1 Timings: Non Mux Device, Asynchronous Write

Figure 30. Write to Write

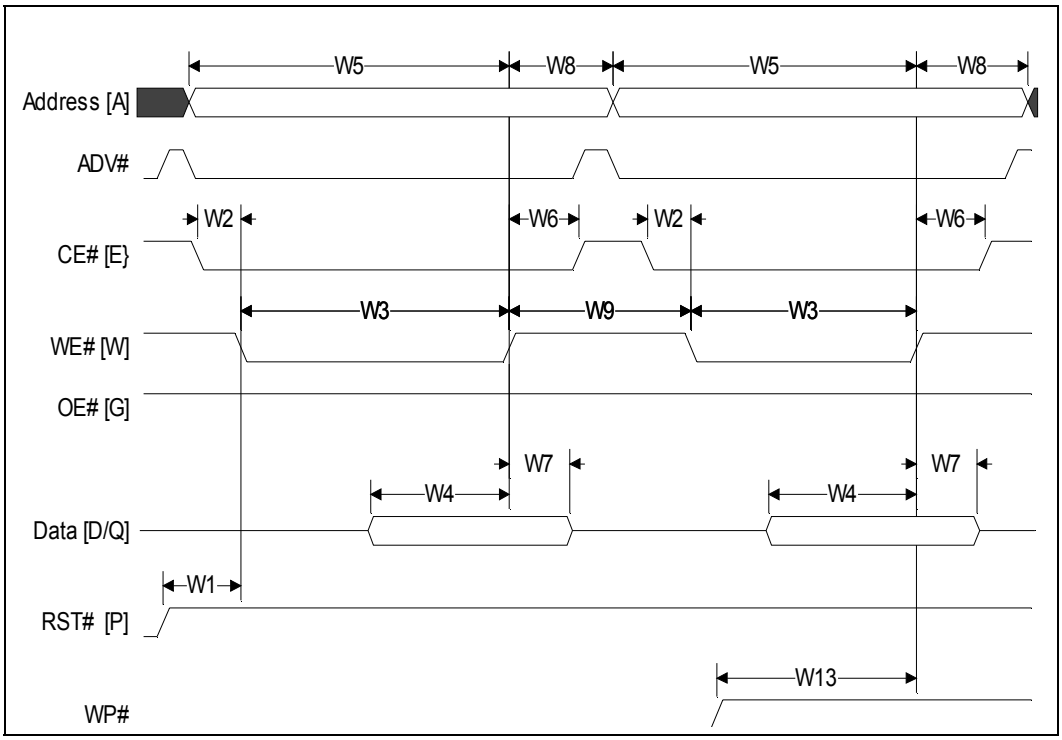
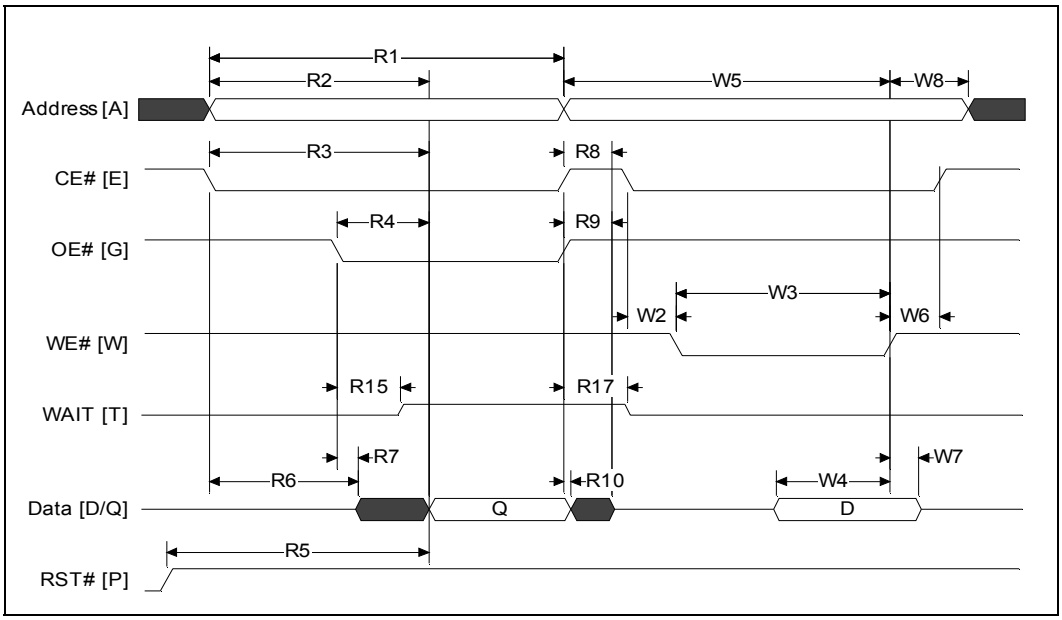
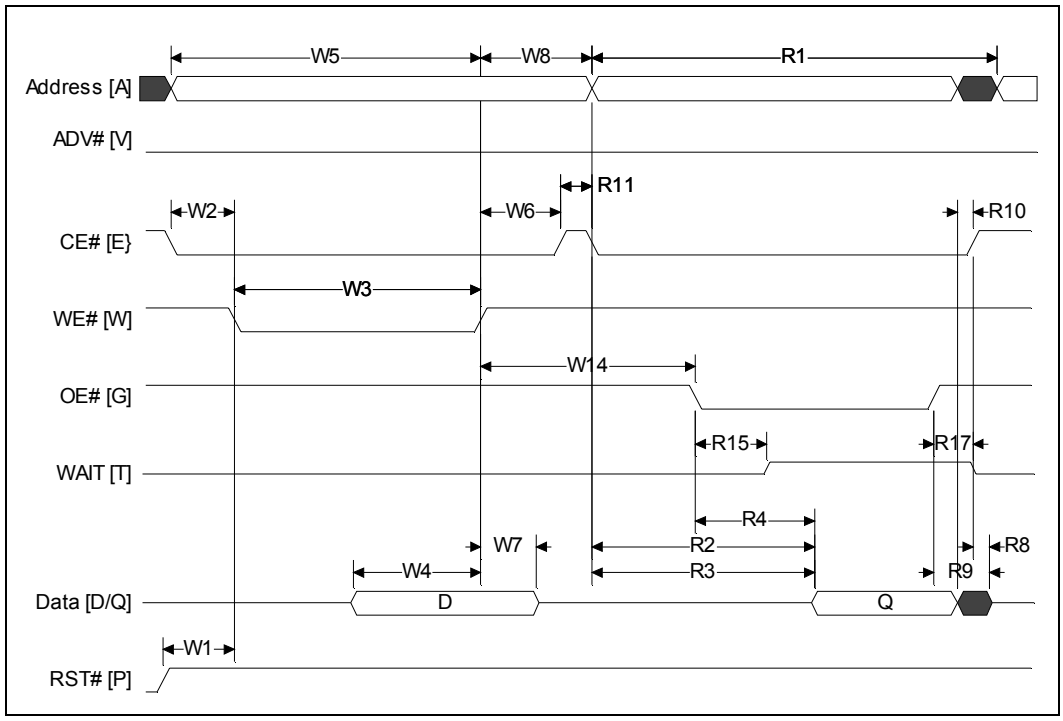


Figure 31. Asynchronous Read to Write



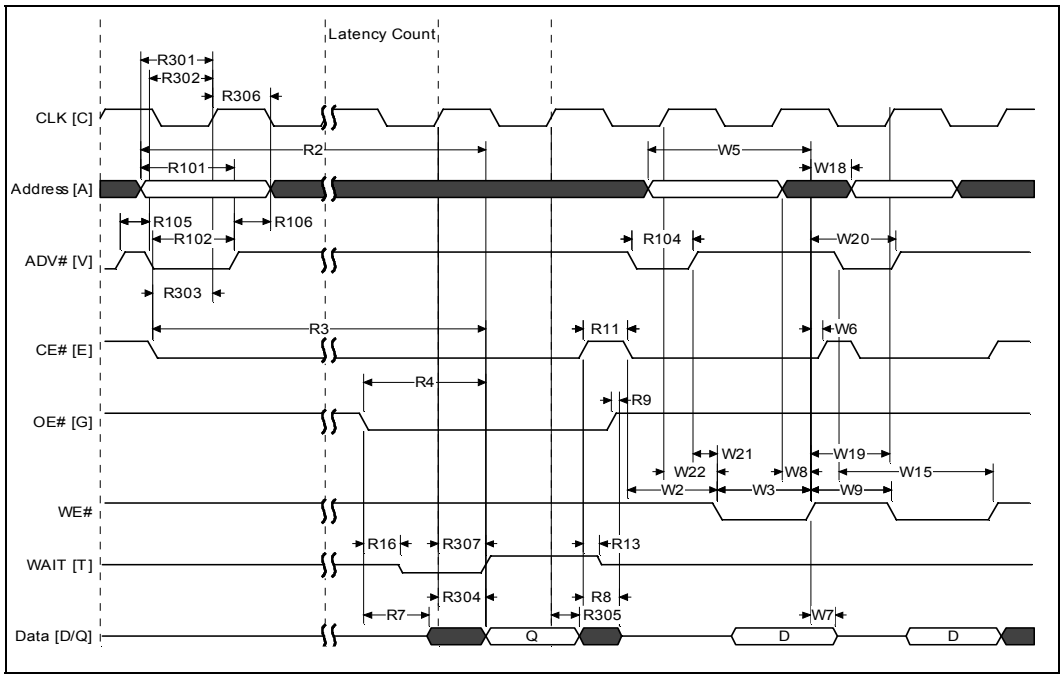
Note: WAIT polarity in figure is low-true (RCR10 = 0, default). WAIT deasserted during asynchronous reads and High-Z during writes.

Figure 32. Write to Asynchronous Read



7.3.2 Timings: Non Mux Device, Synchronous Write 108 MHz, 512 Mb

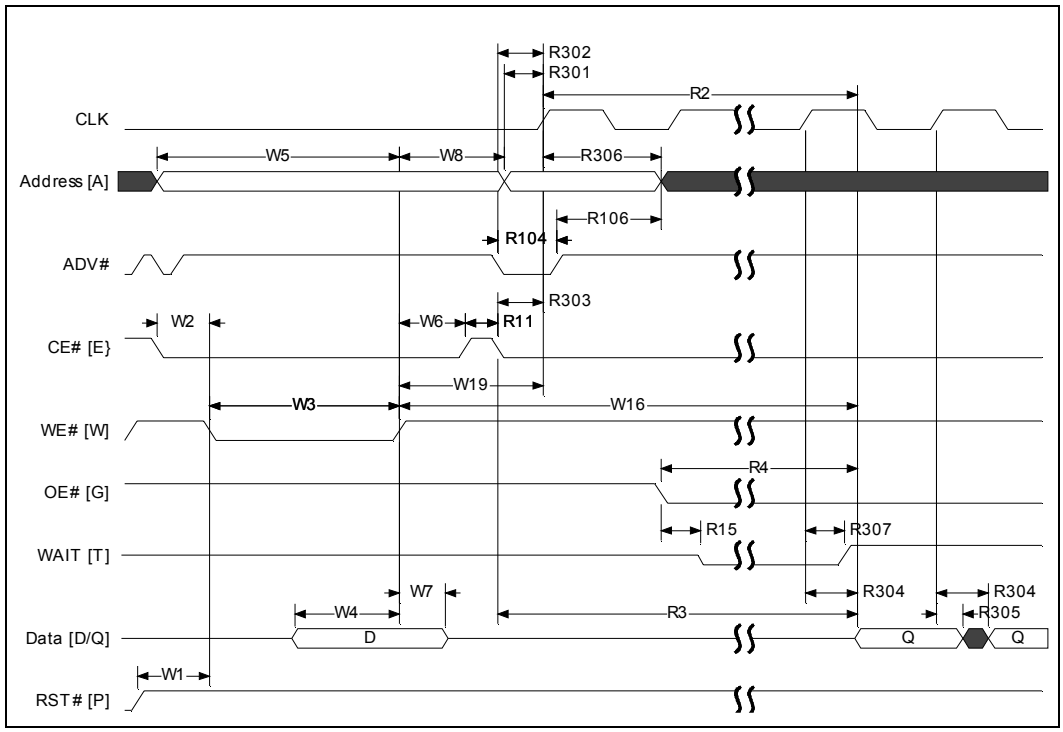
Figure 33. Synchronous Read to Write 108 MHz, 512 Mbit



Notes:

1. WAIT polarity in figure is low-true (RCR10 = 0, default). WAIT is high-Z during write operations.
2. Clock is ignored during write operation.

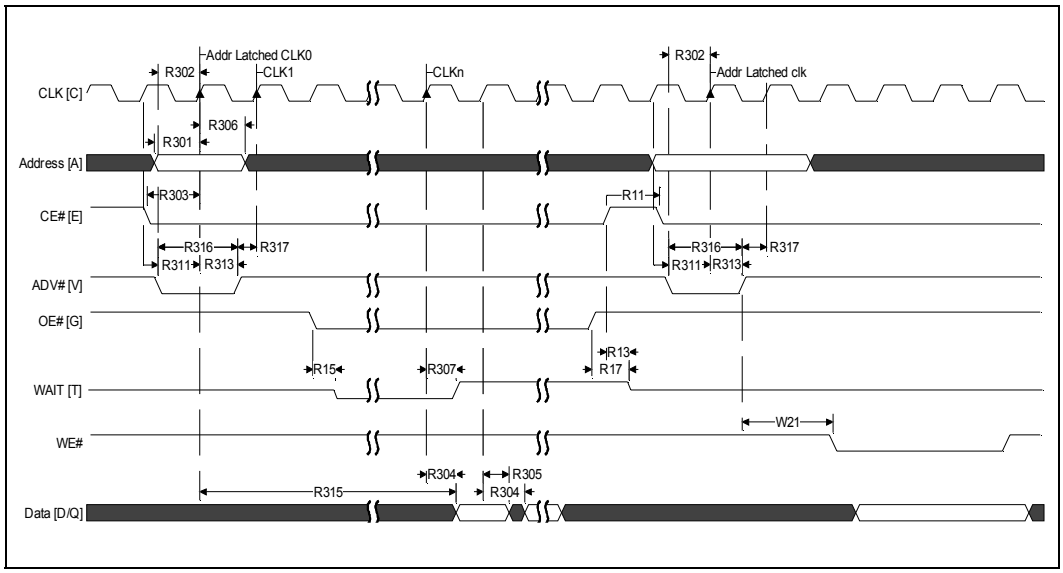
Figure 34. Write to Synchronous Read 108 MHz, 512 Mbit



Note: WAIT polarity in figure is low-true (RCR10 = 0, default).

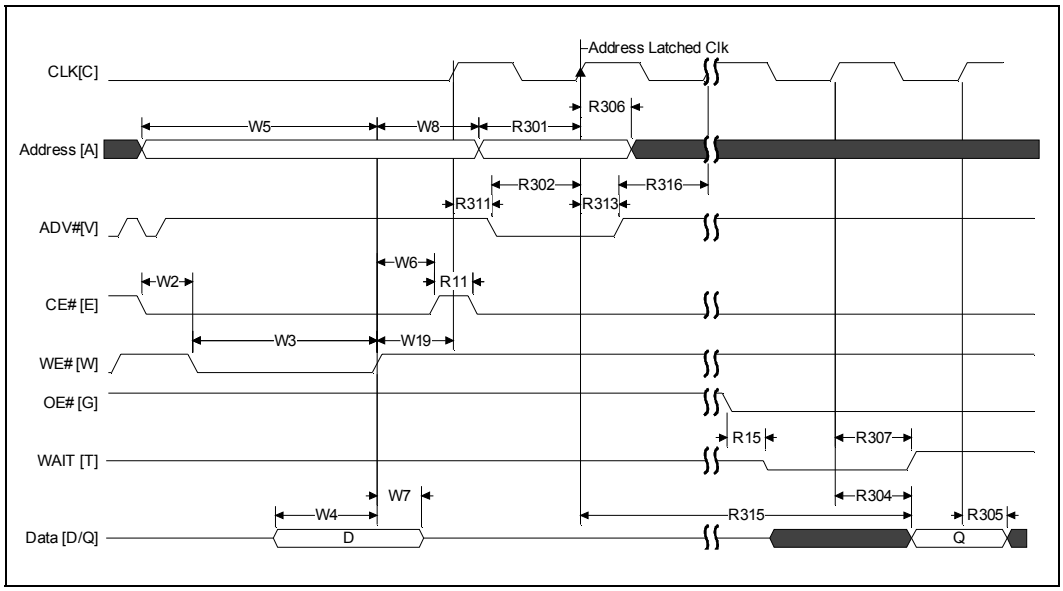
7.3.3 Timings: Non Mux Device, Synchronous Write 133 MHz, 256 Mb

Figure 35. Synchronous Read to Write 133 MHz, 256 Mb



NOTE: WAIT polarity in figure is low-true (RCR10 = 0, default).

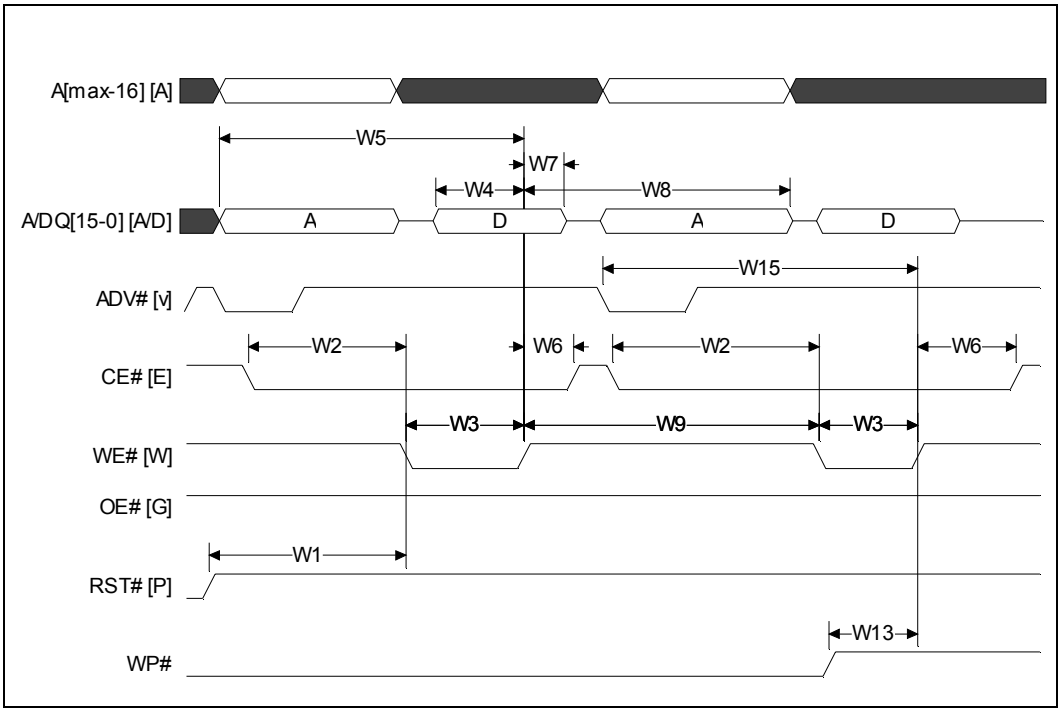
Figure 36. Write to Synchronous Read 133 MHz, 256 Mb



NOTE: WAIT polarity in figure is low-true (RCR10 = 0, default).

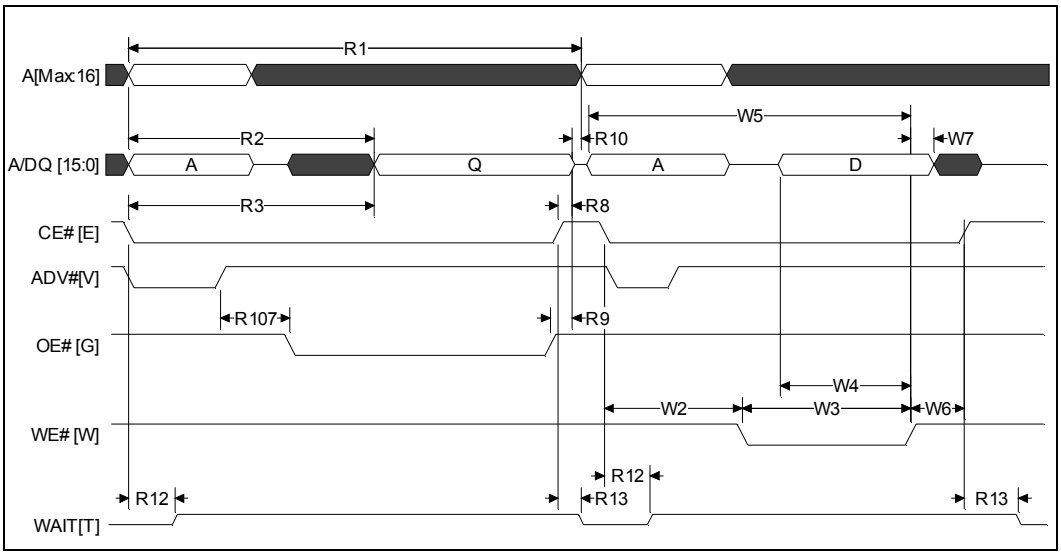
7.3.4 Timings: AD-Mux Device, Asynchronous Write

Figure 37. Write to Write



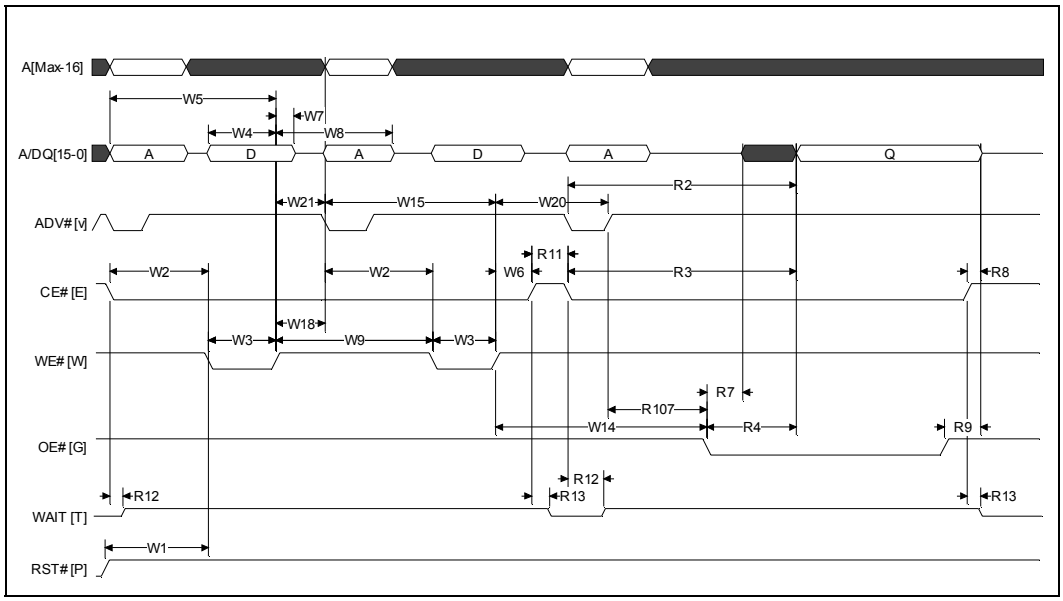
Note: WAIT polarity in figure is low-true (RCR10 = 0, default).

Figure 38. Asynchronous Read to Write



Note: WAIT polarity in figure is low-true (RCR10 = 0, default).

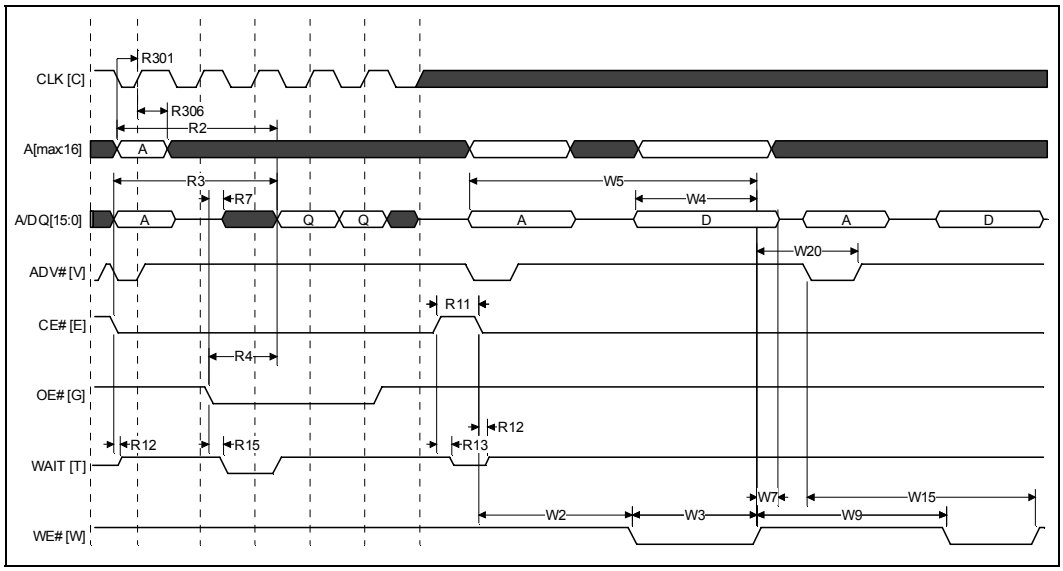
Figure 39. Write to Asynchronous Read



Note: WAIT polarity in figure is low-true (RCR10 = 0, default).

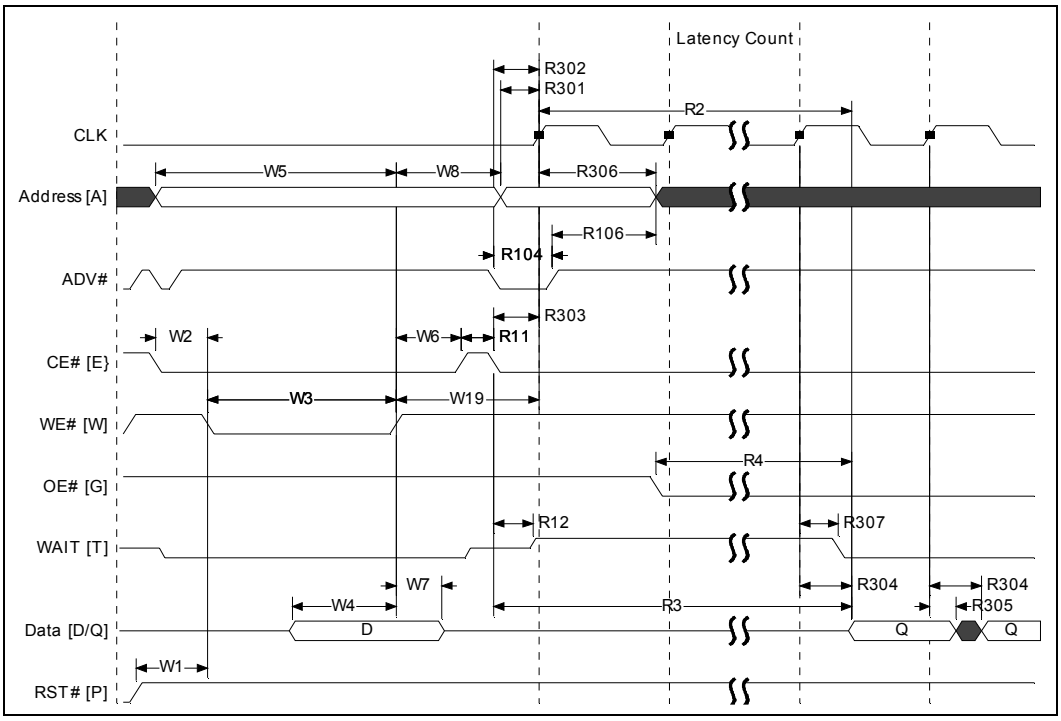
7.3.5 Timings: AD-Mux Device, Synchronous Write 108 MHz, 512 Mb

Figure 40. Synchronous Read to Write 108 MHz, 512 Mbit



Note: WAIT polarity in figure is low-true (RCR10 = 0, default).

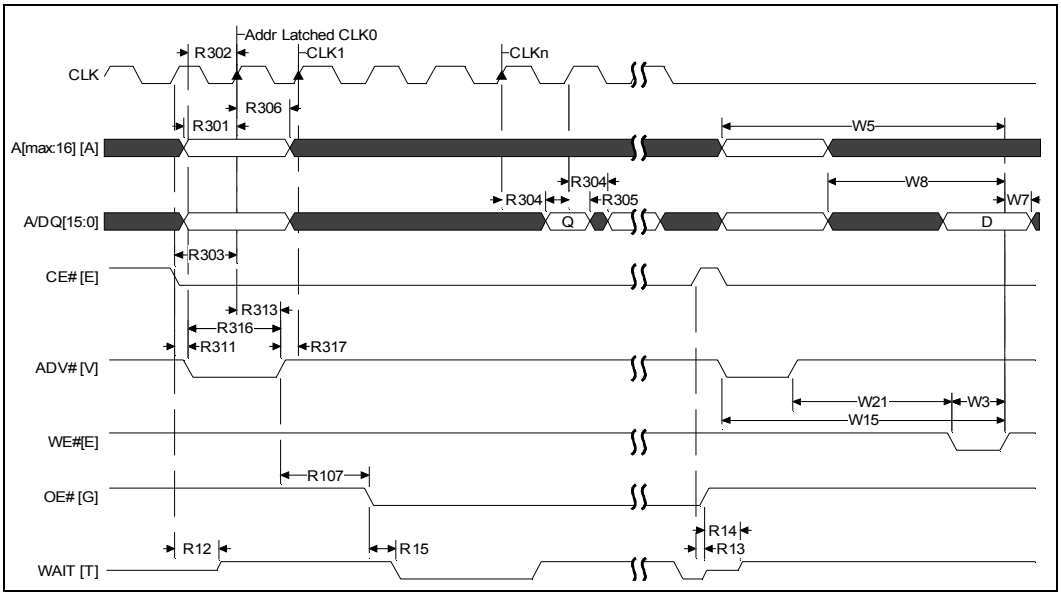
Figure 41. Write to Synchronous Read 108 MHz, 512 Mbit



Note: WAIT polarity in figure is low-true (RCR10 = 0, default).

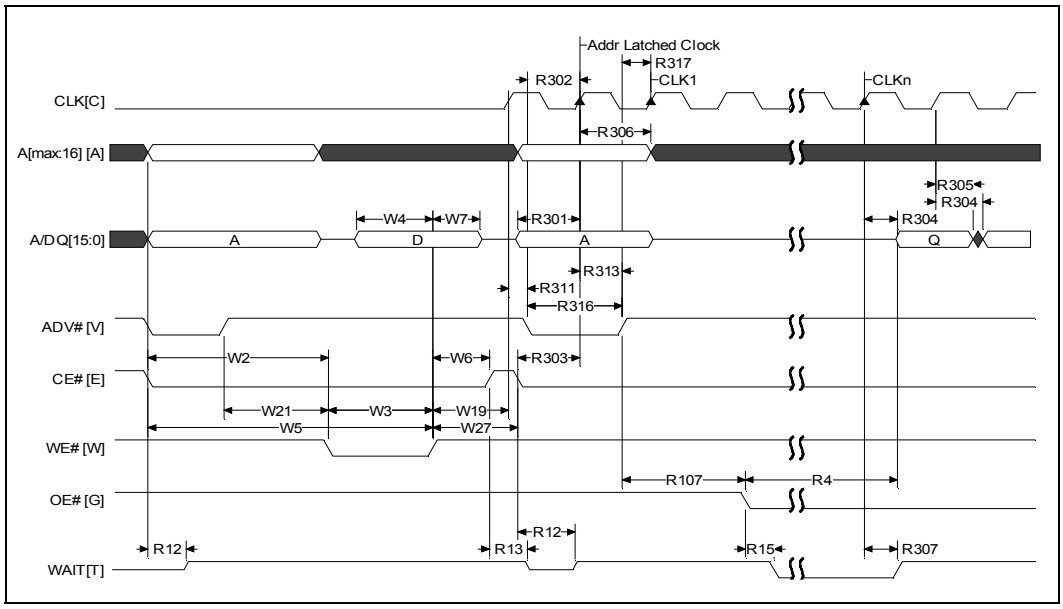
7.3.6 Timings: AD-Mux Device, Synchronous Write 133 MHz, 256 Mb

Figure 42. Synchronous Read to Write 133 MHz, 256 Mb



Note: WAIT polarity in figure is low-true (RCR10 = 0, default).

Figure 43. Write to Synchronous Read 133 MHz, 256 Mb



Note: WAIT polarity in figure is low-true (RCR10 = 0, default).

7.4 Program and Erase Characteristics

Table 15. Program and Erase Characteristics

Nbr.	Symbol	Parameter		V_{PPL}/V_{PPH}			Units	Notes
				Min	Typ	Max		
Conventional Word Programming								
W200	$t_{PROG/W}$	Program Time	Single word (first word)	—	115	230	µs	1,2
			Single word (subsequent word)	—	50	230		
			Single word (EFA)	—	50	230		1
Buffered Programming								
W200	$t_{PROG/W}$	Program Time	Single word	—	250	500	µs	1
W250	$t_{PROG/PB}$		One Buffer (512 words)	—	2.15	4.3	ms	
Buffered Enhanced Factory Programming								
W451	$t_{BEFP/W}$	Program	Single word	—	4.2	—	µs	1,3,4
W452	$t_{BEFP/Setup}$		Buffered EFP Setup	5	—	—		1
Erasing and Suspending								
W500	$t_{ERS/EFA\ B}$	Erase Time	4-Kword EFA Block	—	0.4	2.5	s	1
W501	$t_{ERS/MAB}$		128-Kword Main Array Block	—	0.9	4		
W600	$t_{SUSP/P}$	Suspend Latency	Program suspend	—	20	25	µs	
W601	$t_{SUSP/E}$		Erase suspend	—	20	25		
Blank Check								
W702	$t_{BC/MB}$	Blank Check	Main array block	—	3.2	—	ms	1

NOTES:
1. Typical values measured at TC = +25 °C and nominal voltages. Performance numbers are valid for all speed versions. Sampled, but not 100% tested.
2. First and subsequent words refer to first word and subsequent words in Control Mode programming region.
3. Averaged over entire device.
4. BEFP not validated at V_{PPL}.

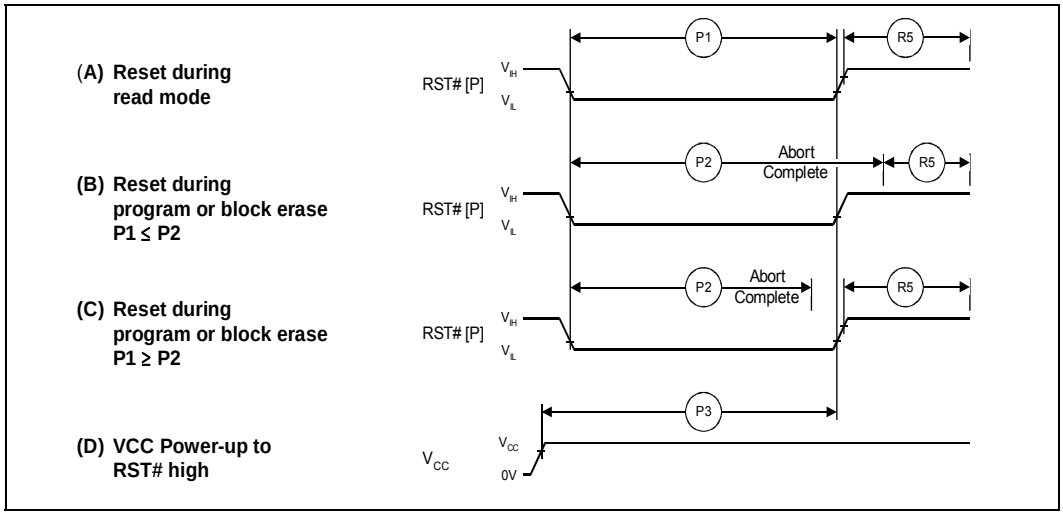
7.5 Reset Specifications

Table 16. Reset Specifications

Nbr.	Symbol	Parameter	Min	Max	Unit	Notes
P1	t_{PLPH}	RST# pulse width low	100		ns	1,2,3,4,7
P2	t_{PLRH}	RST# low to device reset during erase		25	µs	1,3,4,7
		RST# low to device reset during program		25		1,3,4,7
P3	t_{VCCPH}	V_{CC} Power valid to RST# de-assertion (high)	300			1,4,5,6

NOTES:
1. These specifications are valid for all device versions (packages and speeds).
2. The device may reset if t_{PLPH} is < $t_{PLPH\ MIN}$, but this is not guaranteed.
3. Not applicable if RST# is tied to Vccq.
4. Sampled, but not 100% tested.
5. If RST# is tied to the V_{CC} supply, device will not be ready until t_{VCCPH} after $V_{CC} \geq V_{CC}$ min.
6. If RST# is tied to any supply/signal with V_{CCQ} voltage levels, the RST# input voltage must not exceed V_{CC} until $V_{CC} \geq V_{CC}$(min).
7. Reset completes within t_{PLPH} if RST# is asserted while no erase or program operation is executing.

Figure 44. Reset Operation Timing



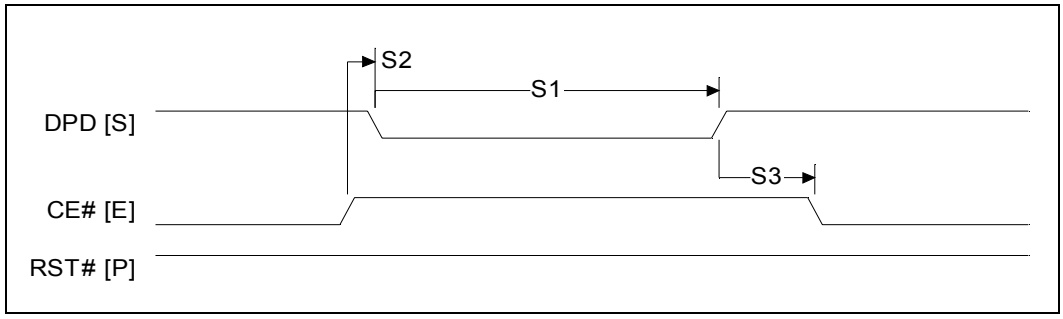
7.6 Deep Power Down Specifications

Table 17. Deep Power Down Specifications

Nbr.	Symbol	Parameter	Min	Max	Unit	Notes
S1	t_{SLSH} (t_{SHSL})	DPD asserted pulse width	100		ns	1,2,3
S2	t_{EHSH} (t_{EHSL})	CE# high to DPD asserted	0		µs	1,2
S3	t_{SHEL} (t_{SLEL})	DPD deasserted to CE# low	75			1,2
S4	t_{PHEL}	RST# high during DPD state to CE# low (DPD deasserted to CE# low)	75			1,2

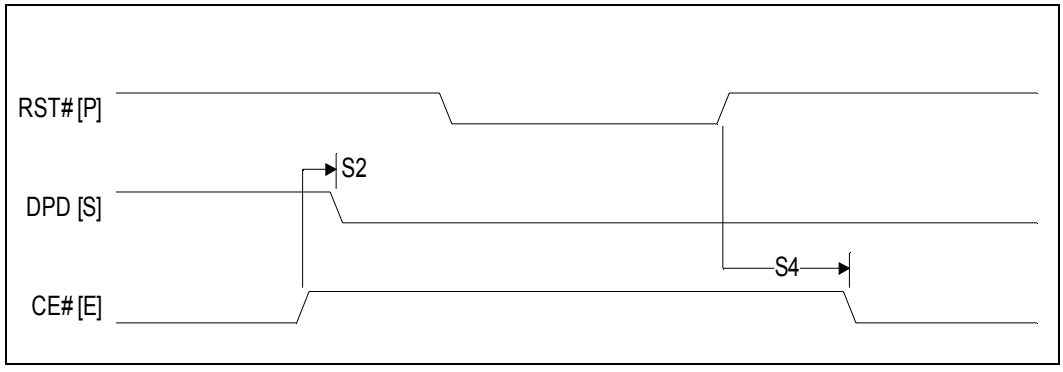
NOTES:
1. These specifications are valid for all device versions (packages and speeds).
2. Sampled, but not 100% tested.
3. DPD must remain asserted for the duration of Deep Power Down mode. DPD current levels are achieved 40 µs after entering the DPD mode.

Figure 45. Deep Power Down Operation Timing



Note: DPD pin is low-true (ECR14 = 0)

Figure 46. Reset During Deep Power Down Operation Timing



Note: DPD pin is low-true (ECR14 = 0)

8.0 NOR Flash Bus Interface

The flash device uses low-true control signal inputs, and is selected by asserting the chip enable (CE#) input. The output enable (OE#) input is asserted for read operations, while the write enable (WE#) input is asserted for write operations. OE# and WE# should never be asserted at the same time; otherwise, indeterminate device operation will result. All bus cycles to or from the flash memory conform to standard microcontroller bus cycles.

Commands are written to the device to control all operations.

Table 18 shows the logic levels that must be applied to the control-signal inputs of the device for the various bus operations.

Table 18. Flash Memory Control Signals

Operation	RST#	DPD[2]	CE#[1]	OE#[1]	WE#[1]	Address[1]	Data I/O
Reset	Low	High	X	X	X	X	High-Z
Read	High	High	Low	Low	High	Valid	Output
Output Disable	High	High	Low	High	High	X	High-Z
Write	High	High	Low	High	⌐¬	Valid	Input
	High	High	¬⌐	High	Low	Valid	Input
Standby	High	High	High	X	X	X	High-Z
Deep Power-Down	High	Low	High	X	X	X	High-Z

Notes:
1. X = Don't care (High or Low)
2. DPD polarity determined by ECR14. Shown low-true here.

8.1 Bus Reads

To perform a read operation, both CE# and OE# must be asserted; RST# and WE# must be deasserted. OE# is the data-output control and when asserted, the output data is driven on to the data I/O bus. All read operations are independent of the voltage level on VPP.

The Automatic Power Savings (APS) feature provides low power operation following reads during active mode. After data is read from the memory array and the address lines are quiescent, APS automatically places the device into standby. In APS, device current is reduced to I_{CCAPS}.

The device supports two read configurations:

- Asynchronous reads. RCR15 = 1. This is the default configuration after power-up/reset.
  - — Non-multiplexed devices support asynchronous page-mode reads. AD-Multiplexed devices support only asychronous single-word reads.
- Synchronous Burst reads. RCR15 = 0.

8.1.1 Asynchronous single-word reads

In asynchronous single-word read mode, a single word of data corresponding to the address is driven onto the data bus after the initial access delay. The address is latched when ADV# is deasserted. For AD-multiplexed devices, ADV# must be deasserted before OE# is asserted.

If only asynchronous reads are to be performed, CLK must be tied to a valid V_{IH} level, and the WAIT signal can be floated. In addition, for non-multiplexed devices, ADV# must be tied to ground.

8.1.2 Asynchronous Page Mode (Non-multiplexed devices only)

In asynchronous page mode, sixteen data words are “sensed” simultaneously from the flash memory array and loaded into an internal page buffer. The buffer word corresponding to the initial address is driven onto the data bus after the initial access delay. Subsequent words in the page are output after the page access delay. A[3:0] bits determine which page word is output during a read operation. A[MAX:4] and ADV# must be stable throughout the page access.

WAIT is deasserted during asynchronous page mode. ADV# can be driven high to latch the address, or held low throughout the read cycle. CLK is not used for asynchronous page-mode reads, and is ignored.

8.1.3 Synchronous Burst Mode

Synchronous burst mode is a clock-synchronous read operation that improves the read performance of flash memory over that of asynchronous reads.

Synchronous burst mode is enabled by programming the Read Configuration Register (RCR) of the flash memory device. The RCR is also used to configure the burst parameters of the flash device, including Latency Count, burst length of 8, 16 and continuous, and WAIT polarity.

Three additional signals are used for burst mode: CLK, ADV#, and WAIT.

The address for synchronous read operations is latched on the ADV# rising edge or the first rising CLK edge after ADV# low, whichever occurs first for devices that support up to 108 MHz. For devices that support upto 133 MHz, the address is latched on the last CLK edge when ADV# is low.

During synchronous read modes, the first word is output from the data buffer on the rising CLK edge after the initial access latency delay. Subsequent data is output on rising CLK edges following a t_{CHQV} delay. However, for a synchronous non-array read, the same word of data will be output on successive rising clock edges until the burst length requirements are satisfied.

8.1.3.1 WAIT Operation

Upon power up or exit from reset, WAIT polarity defaults to low-true operation (RCR10 = 0). During *synchronous* reads (RCR15 = 0), WAIT asserts when read data is *invalid*, and deasserts when read data is *valid*. During *asynchronous* reads (RCR15 = 1), WAIT is deasserted. During writes, WAIT is High-Z on non-mux devices, and deasserted on AD-mux devices. Table 19 summarizes WAIT behavior.

Table 19. WAIT Behavior Summary

Device Operation		CE#	OE#	WE#	WAIT	Notes
Device not selected	Standby	High	X	X	High-Z	1
Non-Mux Device	Output Disable	Low	High	High	High-Z	
	Sync Read		Low	High	Active	2
	Async Read		Low	High	Deasserted	
	Write		High	Low	High-Z	
AD-Mux Device	Output Disable		High	High	Deasserted	
	Sync Read		Low	High	Active	2
	Async Read		Low	High	Deasserted	
	Write		High	Low	Deasserted	

NOTES:
1. X = don't care (high or low).
2. Active: WAIT asserted = invalid data; WAIT deasserted = valid data.

8.2 Bus Writes

To perform a write operation, both CE# and WE# are asserted while RST# and OE# are deasserted. All device write operations are asynchronous, with CLK being ignored, but CLK can be kept active/toggling. During a write operation, address and data are latched on the rising edge of WE# or CE#, whichever occurs first.

8.3 Reset

The device enters a reset mode when RST# is asserted. In reset mode, internal circuitry is turned off and outputs are placed in a high-impedance state. The device shuts down any operation in progress, a process which takes a minimum amount of time to complete.

To return from reset mode, RST# must be deasserted. Normal operation is restored after a wake-up interval.

8.4 Deep Power-Down

The device enters DPD mode when the following two conditions are met: ECR15 is set(1) and DPD is asserted. The two conditions can be satisfied in any order. ECR14 bit determines the DPD asserted logic level. While in this mode, RST# and CE# must be deasserted.

The device exits DPD mode when DPD is deasserted. There is an exit latency before the device returns to standby mode and any operations are allowed. See Section 7.6, "Deep Power Down Specifications" on page 61 for the timing specifications.

The device should not be placed in DPD mode when a program/erase operation is ongoing or suspended. If the device enters DPD mode in the middle of a program, erase or suspend, the operation is terminated and the memory contents at the aborted location (for a program) or block (for an erase) are no longer valid.

While in DPD mode, the read-mode of each partition, configuration registers (RCR and ECR), and block lock bits, are preserved. Status register is reset to 0080h; i.e., if the Status register contains error bits, they will be cleared.

8.5 Standby

When CE# is deasserted, the device is deselected and placed in standby, substantially reducing power consumption. In standby, data outputs are placed in high-Z, independent of the level placed on OE#. If deselected during a Program or Erase operation, the device continues to consume active power until the operation is complete. There is no additional latency for subsequent read operations.

8.6 Output Disable

When OE# is deasserted with CE# asserted, the device outputs are disabled. Output pins are placed in a high-impedance state. WAIT is deasserted in AD-muxed devices and driven to High-Z in non-multiplexed devices.

8.7 Bus Cycle Interleaving

When issuing commands to the device, a read operation can occur between the two writes cycles of a 2-cycle command. (See Figure 47 and Figure 48) However, a write operation cannot occur between the two write cycles of a 2-cycle command and will cause a command sequence error (See Figure 49).

Figure 47. Operating Mode with Correct Command Sequence Example

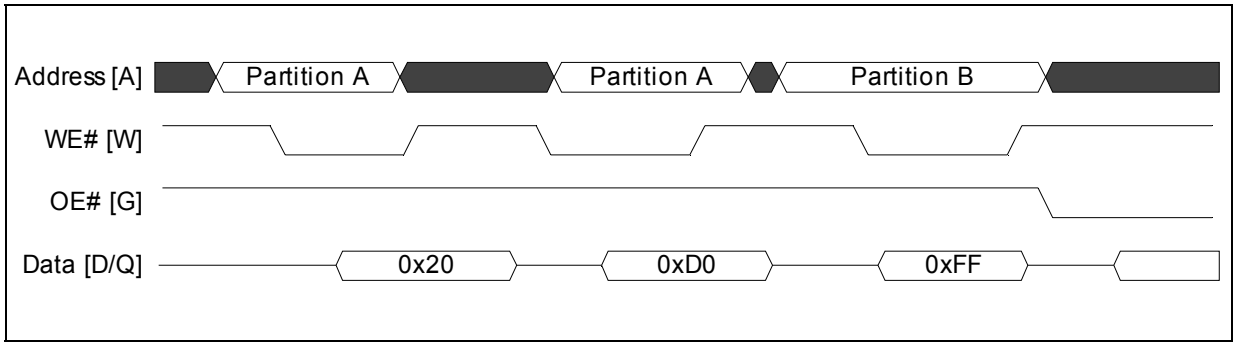


Figure 48. Operating Mode with Correct Command Sequence Example

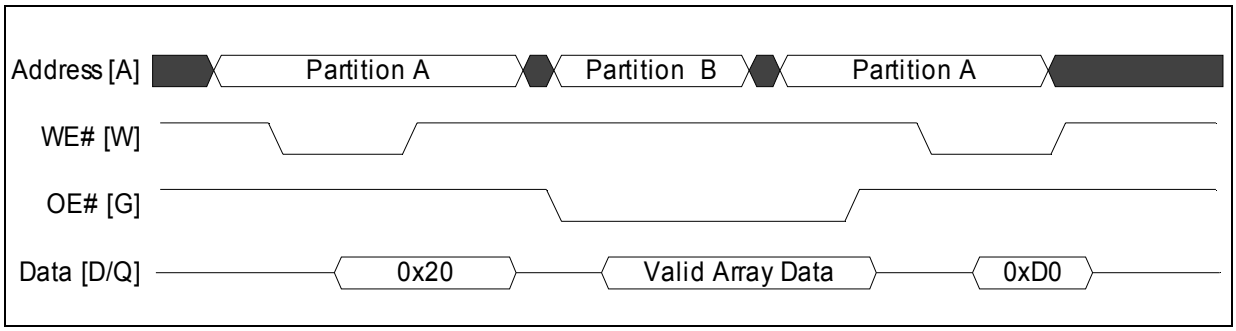
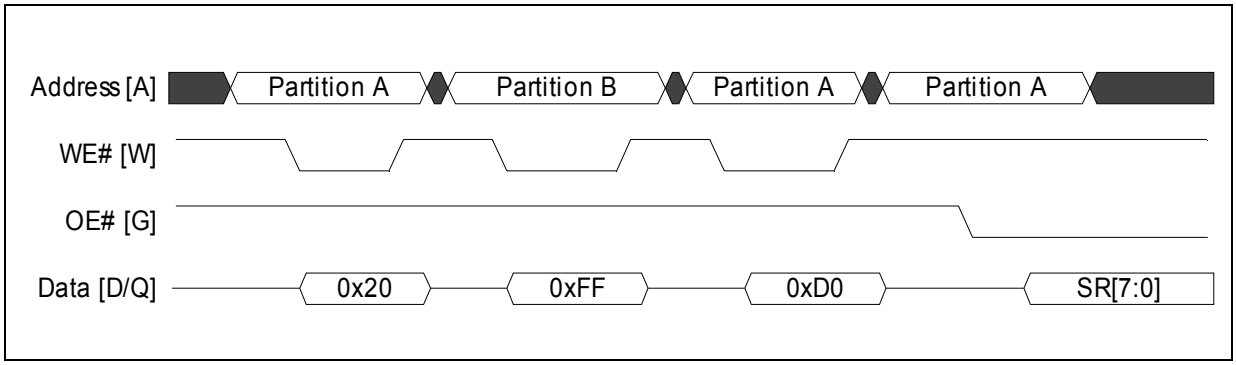


Figure 49. Operating Mode with Illegal Command Sequence Example



8.7.1 Read Operation During Program Buffer fill

Due to the large buffer size of M18 devices, the system interrupt latency may be impacted during the buffer fill phase of a buffered programming operation. Please refer to the relevant Application Note listed in Appendix F, "Additional Information" to implement a software solution for your system.

8.8 Read-to-Write and Write-to-Read Bus Transitions

Consecutive read and write bus cycles must be properly separated from each other to avoid bus contention. These cycle separation specs are described in the sections below.

8.8.1 Write to Asynchronous read transition

To transition from a bus write to an asynchronous read operation, either CE# or ADV# must be toggled after WE# goes high.

8.8.2 Write to synchronous read transition

To transition from a bus write to a synchronous read operation, either CE# or ADV# must be toggled after WE# goes high. In addition, W19 (t_{WHCH} -WE# high to CLK high) must be met.

8.8.3 Asynchronous/Synchronous read to write transition

To transition from a asynchronous/synchronous read to a write operation, either CE# or ADV# must be toggled after OE# goes high.

8.8.4 Bus write with active clock

To perform a bus write when the device is in synchronous mode and the clock is active, W21 (t_{VHWL}- ADV# High to WE# Low) or W22 (t_{CHWL} -Clock high to WE# low) must be met.

9.0 NOR Flash Operations

This section describes the operational features of NOR flash memory. Operations are command-based—command codes are first issued to the device, and then the device performs the desired operation. All command codes are issued to the device using bus-write cycles (see Chapter 8.0, "NOR Flash Bus Interface"). A complete list of available command codes can be found in Appendix A, "Device Command Codes".

9.1 Initialization

Proper device initialization and operation is dependent on the power-up/down sequence, reset procedure, and adequate power-supply decoupling. The following sections describe each of these areas.

9.1.1 Power-Up/Down Characteristics

To prevent conditions that could result in spurious program or erase operations, the power-up/power-down sequence shown in Table 20 is recommended. Note that each power supply must reach its minimum voltage range before applying/removing the next supply voltage.

Table 20. Power-Up/Down Sequence

Power Supply Voltage	Power-UpSequence				Power-Down Sequence			
$V_{CC(min)}$	1st	1st	1st*	Sequencing not required*	3rd	2nd	2nd*	Sequencing not required*
$V_{CCQ(min)}$	2nd	2nd*			2nd	1st*		
$V_{PP(min)}$	3rd		2nd		1st		1st	

* Power supplies connected or sequenced together.

Device inputs must not be driven until all supply voltages reach their minimum range. RST# should be low during power transitions.

Note: If V_{CCQ} is below V_{LKOQ}, the device is reset.

9.1.2 Reset Characteristics

During power-up and power-down, RST# should be asserted to prevent spurious program or erase operations. While RST# is low, device operations are disabled, all inputs (e.g., address, control) are ignored, and all outputs (e.g., data, WAIT) are placed in High-Z. Invalid bus conditions are effectively masked out.

Upon power-up, RST# can be deasserted after t_{VCCPH}, allowing the device to exit from reset. Upon exiting from reset, the device defaults to asynchronous Read Array mode, and the Status Register defaults to 0080h. Array data is available after t_{PHQV}, or a bus-write cycle can begin after t_{PHWL}.

If RST# is asserted during a program or erase operation, the operation will abort and array contents at that location will be invalid.

For proper system initialization, connect RST# to the low-true reset signal that asserts whenever the processor is reset. This will ensure the flash device is in the expected read mode (i.e., Read Array) upon startup.

9.1.3 Power Supply Decoupling

High-speed flash memories require adequate power-supply decoupling to prevent external transient noise from affecting device operations, and to prevent internally-generated transient noise from affecting other devices in the system.

Ceramic .01 to 0.1 µfd capacitors should be used between all VCC, VCCQ, VPP supply connections and system ground. These high-frequency, inherently low-inductance capacitors should be placed as close as possible to the device package, or on the opposite side of the printed circuit board close to the center of the device-package footprint.

Larger (4.7 µfd to 33.0 µfd) electrolytic or tantulum bulk capacitors should also be distributed as needed throughout the system to compensate for voltage sags caused by circuit-board trace inductance.

Transient current magnitudes depend on the capacitive and inductive loading on the device's outputs. For best signal integrity and device performance, high-speed design rules should be used when designing the printed-circuit board. Circuit-trace impedances should match output-driver impedance with adequate ground-return paths. This will help minimize signal reflections (overshoot/undershoot) and noise caused by high-speed signal edge rates.

9.2 Status Register

The Status Register (SR) is a 16-bit, read-only register that indicates device and partition status, and operational errors. To read the Status Register, issue the Read Status Register command. Subsequent reads output Status Register information on AD/DQ[9:0], and 00h on AD/DQ[15:10].

SR *status bits* are set and cleared by the device. SR *error bits* are set by the device, and must be cleared using the Clear Status Register command. Upon power-up or exit from reset, the Status Register defaults to 0080h. Table 21 shows Status Register bit definitions.

Table 21. Status Register Bit Definitions

Status Register (SR)									Default Value = 0080h
Reserved	Region Program Status	Ready Status	Erase Suspend Status	Erase Error	Program Error	Program/ Erase Voltage Error	Program Suspend Status	Block-Locked Error	Partition Status
15-10	9-8	7	6	5	4	3	2	1	0

Bit	Name		Description
15-10	Reserved		Reserved for future use; these bits will always be set to zero.
9-8	Region Program Status		SR9 SR8 0 0 = Region program successful. 1 0 = Region program error - Attempted write with object data to Control Mode region. 0 1 = Region program error - Attempted rewrite to Object Mode region. 1 1 = Region program error - Attempted write using illegal command. SR4 will also be set along with SR[8,9] for the above error conditions.
7	Ready Status		0 = Device is busy; SR[9:8], SR[6:1] are invalid; 1 = Device is ready; SR[9:8], SR[6:1] are valid.
6	Erase Suspend Status		0 = Erase suspend not in effect. 1 = Erase suspend in effect.
5	Erase Error / Blank Check Error	Command Sequence Error	SR5 SR4 0 0 = Program or erase operation successful. 0 1 = Program error - operation aborted. 1 0 = Erase error - operation aborted / Blank check error - operation failed. 1 1 = Command sequence error - command aborted.
4	Program Error		
3	V_{PP} Error		0 = V_{PP} within acceptable limits during program or erase operation. 1 = V_{PP} not within acceptable limits during program or erase operation.
2	Program Suspend Status		0 = Program suspend not in effect. 1 = Program suspend in effect.
1	Block-Locked Error		0 = Block NOT locked during program or erase - operation successful. 1 = Block locked during program or erase - operation aborted.
0	Partition Status		SR7 SR0 0 0 = Active program or erase operation in addressed partition. BEFP: Program or Verify complete, or Ready for data. 0 1 = Active program or erase operation in other partition. BEFP: Program or Verify in progress. 1 0 = No active program or erase operation in any partition. BEFP: Operation complete 1 1 = Reserved.

9.2.1 Clearing the Status Register

The Status Register (SR) contain status and error bits which are set by the device. SR *status bits* are cleared by the device, however SR *error bits* are cleared by issuing the Clear Status Register command (see Table 22). Resetting the device also clears the Status Register.

Table 22. Clear Status Register Command Bus Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Clear Status Register	Device Address	0050h	---	---

Issuing the Clear Status Register command places the addressed partition in Read Status Register mode. Other partitions are not affected.

Note: Care should be taken to avoid Status Register ambiguity. If a command sequence error occurs while in an Erase Suspend condition, the Status Register will indicate a Command Sequence error by setting SR4 and SR5. When the erase operation is resumed (and finishes), any errors that may have occurred during the erase operation will be masked by the Command Sequence error. To avoid this situation, clear the Status Register prior to resuming a suspended erase operation.

The Clear Status Register command functions independent of the voltage level on VPP.

9.3 Read Configuration Register

The Read Configuration Register (RCR) is a 16-bit read/write register used to select bus-read modes, and to configure synchronous-burst read characteristics of the flash device. All Read Configuration Register bits are set and cleared using the Program Read Configuration Register command. Section 9.3.2 describes how to program the Read Configuration Register.

Upon power-up or exit from reset, the Read Configuration Register defaults to asynchronous mode (RCR15 = 1; RCR[14:11] and RCR[9:0] are ignored). Table 23 shows the Read Configuration Register bit definitions.

To read the RCR value, issue the Read Device Information command to the desired partition. Subsequent reads from the <partition base address> + 05h outputs RCR[15:0] on the data bus.

Table 23. Read Configuration Register Bit Definitions

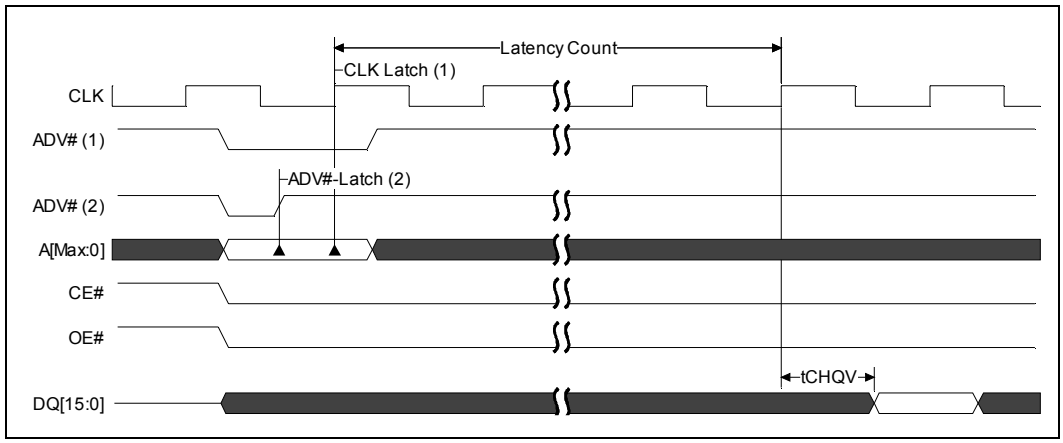
Read Configuration Register (RCR)											Default: CR15 = 1
Read Mode	Latency Count				WAIT Polarity	R	WAIT Delay	Reserved	Burst Length		
15	14	13	12	11	10	9	8	7:3	2	1	0

Bit	Name	Description
15	Read Mode	0 = Synchronous burst-mode reads 1 = Asynchronous page-mode reads (default)
14:11	Latency Count	00 1 1= Code 3 01 0 0= Code 4 01 0 1= Code 5 01 1 0= Code 6 01 1 1= Code 7 10 0 0= Code 8 10 0 1= Code 9 10 1 0= Code 10 10 1 1= Code 11 11 0 0= Code 12 (Other bit settings are reserved)
10	WAIT Polarity	0 =WAIT signal is active low (default) 1 =WAIT signal is active high
9	Reserved	Write 0 to reserved bits
8	WAIT Delay	0 = WAIT de-asserted with valid data 1 = WAIT de-asserted one cycle before valid data (default)
7:3	Reserved	Write 0 to reserved bits
2:0	Burst Length	01 0 = 8-word burst (wrap only) 01 1 = 16-word burst (wrap only) 11 1 = Continuous-word burst (no-wrap; default) (Other bit settings are reserved)

9.3.1 Latency Count

The Latency Count value programmed into RCR[14:11] is the number of valid CLK edges from address-latch to the start of the data-output delay. When the Latency Count has been satisfied, output data is driven after tCHQV (see Figure 50, “Latency Count Period” on page 73).

Figure 50. Latency Count Period



Notes:
1. Address latched on valid clock edge with ADV# low and LC count begins.
2. Address latched on ADV# rising edge. LC count begins on subsequent valid CLK edge.

Table 24. CLK Frequencies for LC Settings

V_{CCQ} = 1.7 V to 2.0 V	
Latency Count Setting	**Frequency Supported (MHz)**
4	≤ 40 MHz
5	≤ 54 MHz
7	≤ 66 MHz
10	≤ 108 MHz
13	≤ 133 MHz

9.3.2 Programming the RCR

The Read Configuration Register (RCR) is programmed by issuing the Program Read Configuration Register command. This is a two-cycle command sequence requiring a setup command to be issued first, followed by a Confirm command (see Table 25). Bus-write cycles to the flash device between the setup and confirm commands are not allowed — a command sequence error will result. However, flash bus-read cycles between the setup and confirm commands are allowed.

Table 25. Program Read Configuration Register Command Bus Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	**Data Bus**	**Address Bus**	**Data Bus**
Program Read Configuration Register	Register Data	0060h	Register Data	0003h

To program the RCR, the desired settings for RCR[15:0] are placed on the address bus. The setup command (0060h) is driven on the data bus. Upon issuing the setup command, the device/ addressed partition is automatically changed to Read Status Register mode.

Next, the Confirm command (0003h) is driven on the data bus. After issuing the confirm command, the addressed partition is automatically switched to Read Array mode.

Note: Since the desired register value is placed on the address lines, any hardware-connection offsets between the host's address outputs and the flash device's address inputs must be considered. For example, if the host's address outputs are aligned to the flash device's address inputs such that host address bit A1 is connected to flash address bit A0, the desired register value may need to be left-shifted internally by one (example: 2532h becomes 4A64h) before programming the Read Configuration Register.

Caution: Care must be exercised when switching to synchronous mode. Synchronous read accesses cannot occur until both the flash device and the memory controller's chip select have reached synchronous operating mode. The software instructions used to perform the Read Configuration Register programming sequence and the chip select configuration must be guaranteed not to fetch from the flash device, i.e., in system RAM or locked in cache. This also applies when switching back to asynchronous mode from synchronous mode.

9.4 Enhanced Configuration Register

The Enhanced Configuration Register (ECR) is a volatile 16-bit, read/write register used to select Deep Power Down (DPD) operation and to modify the output-driver strength of the flash device. All Enhanced Configuration Register bits are set and cleared using the Program Enhanced Configuration Register command. Section 9.4.2 describes how to program the Enhanced Configuration Register.

Upon power-up or exit from reset, the Enhanced Configuration Register defaults to 0004h. Table 26 shows the Enhanced Configuration Register bit definitions.

To read the value of the ECR, issue the Read Device Information command to the desired partition. Subsequent reads from the <partition base address> + 06h returns ECR[15:0].

Table 26. Enhanced Configuration Register Bit Definitions (Sheet 1 of 2)

Enhanced Configuration Register					Default = 0004h
Deep Power Down (DPD) Mode	DPD Polarity	Reserved	Output Driver Control		
15	14	13:3	2	1	0

Bit	Name	Description
15	Deep Power Down (DPD) Mode	0 = DPD Disabled (default) 1 = DPD Enabled

Table 26. Enhanced Configuration Register Bit Definitions (Sheet 2 of 2)

Enhanced Configuration Register					Default = 0004h
Deep Power Down (DPD) Mode	DPD Polarity	Reserved	Output Driver Control		
15	14	13:3	2	1	0

Bit	Name	Description
14	DPD Pin Polarity	0 = Active Low (default) 1 = Active High
13:3	Reserved	Write 0 to reserved bits
2:0	Output Driver Control	0 0 1 = Code 1 0 1 0 = Code 2 0 1 1 = Code 3 1 0 0 = Code 4 (default) 1 0 1 = Code 5 1 1 0 = Code 6 (Other bit settings are reserved)

9.4.1 Output Driver Control

Output Driver Control enables the user to adjust the device's output-driver strength of the data I/O bus and WAIT signal. Upon power-up or reset, ECR[2:0] defaults to an output impedance setting of 30 Ohms. To change the output-driver strength, ECR[2:0] must be programmed to the desired setting as shown in Table 27.

Table 27. Output Driver Control Characteristics

Control Bits ECR[2:0]	Impedance @ VCCQ/2 (Ohm)	Driver Multiplier	Load Driven at Same Speed (pF)
001	90	1/3	10
010	60	1/2	15
011	45	2/3	20
100 (default)	30	1	30
101	20	3/2	35
110	15	2	40

9.4.2 Programming the ECR

The ECR is programmed by issuing the Program Enhanced Configuration Register command. This is a two-cycle command sequence requiring a setup command to be issued first, followed by a Confirm command (see Table 28). Bus-write cycles to the flash device between the setup and confirm commands are not allowed — a command sequence error will result. However, flash bus-read cycles between the setup and confirm commands are allowed.

Table 28. Program Enhanced Configuration Register Command Bus Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Program Enhanced Configuration Register	Register Data	0060h	Register Data	0004h

To program the Enhanced Configuration Register, the desired settings for ECR[15:0] are placed on the address bus. The setup command (0060h) is driven on the data bus. Upon issuing the setup command, the device/addressed partition is automatically changed to Read Status Register mode.

Next, the Confirm command (0004h) is driven on the data bus. After issuing the Confirm command, the addressed partition is automatically switched to Read Array mode.

This command functions independently of the applied V_{PP} voltage.

Since the desired register value is placed on the address lines, any hardware-connection offsets between the host's address outputs and the flash device's address inputs must be considered, similar to programming the RCR.

9.5 Read Operations

Five types of data can be read from the device: array data, device information, CFI data, device status, and extended flash array (EFA) data. Upon power-up or return from reset, the device defaults to Read Array mode. To change the device's read mode, the appropriate command must be issued to the device. Table 29 shows the command codes used to configure the device for the desired read mode. The following sections describe each read mode.

Table 29. Read Mode Command Bus Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Read Array	Partition Address	00FFh	---	---
Read Status Register	Partition Address	0070h	---	---
Read Device Information	Partition Address	0090h	---	---
CFI Query	Partition Address	0098h	---	---
Read Extended Flash Array (EFA) Block	Partition Address	0094h	---	---

9.5.1 Read Array

Upon power-up or exit from reset, the device defaults to Read Array mode. Issuing the Read Array command places the addressed partition in Read Array mode. Subsequent reads output array data. The addressed partition remains in Read Array mode until a different read command is issued, or a program or erase operation is performed in that partition, in which case, the read mode is automatically changed to Read Status.

To change a partition to Read Array mode while it is programming or erasing, first issue the Suspend command. After the operation has been suspended, issue the Read Array command to the partition. When the program or erase operation is subsequently resumed, the partition will automatically revert back to Read Status mode.

Note: Issuing the Read Array command to a partition that is actively programming or erasing causes subsequent reads from that partition to output invalid data. Valid array data is output only after the program or erase operation has finished.

The Read Array command functions independent of the voltage level on VPP.

9.5.2 Read Status Register

Issuing the Read Status Register command places the addressed partition in Read Status Register mode. Subsequent reads from that partition output Status Register information. The addressed partition remains in Read Status Register mode until a different read-mode command is issued to that partition. Performing a program, erase, or block-lock operation also changes the partition's read mode to Read Status Register mode.

The Status Register is updated on the falling edge of CE#, or OE# when CE# is low. Status Register contents are valid only when SR7 = 1.

The Read Status Register command functions independent of the voltage level on VPP.

9.5.3 Read Device Information

Issuing the Read Device Information command places the addressed partition in Read Device Information mode. Subsequent reads output device information on the data bus. Table 30 shows the address offset for reading the available device information.

Table 30. Device Information Summary

Device Information	Address Bus	Data Bus
Device Manufacturer Code (Intel)	Partition Base Address + 00h	0089h
Device ID Code	Partition Base Address + 01h	(See Appendix B, "Device ID Codes.")
Main Block Lock Status	Block Base Address + 02h	D0 = Lock Status D1 = Lock-Down Status
EFA Block Lock Status	Block Base Address + 02h	D4 = Lock Status D5 = Lock-Down Status
Read Configuration Register	Partition Base Address + 05h	Configuration Register Data
Enhanced Configuration Register	Partition Base Address + 06h	Enhanced Configuration Register Data
OTP Lock Register 0	Partition Base Address + 80h	Lock Register 0 Data
OTP Register - Factory Segment	Partition Base Address + 81h to 84h	Factory-Programmed Data
OTP Register - User-Programmable Segment	Partition Base Address + 85h to 88h	User Data
OTP Lock Register 1	Partition Base Address + 89h	Lock Register 1 Data
OTP Registers 1 through 16	Partition Base Address + 8Ah to 109h	User Data

The addressed partition remains in Read Device Information mode until a different read command is issued. Also, performing a program, erase, or block-lock operation changes the addressed partition to Read Status Register mode.

Note: Issuing the Read Device Information command to a partition that is actively programming or erasing changes that partition's read mode to Read Device Information mode. Subsequent reads from that partition will return invalid data until the program or erase operation has completed.

The Read Device Information command functions independent of the voltage level on VPP.

9.5.4 CFI Query

Issuing the CFI Query command places the addressed partition in CFI Query mode. Subsequent reads from that partition output CFI information (see Appendix D, "Common Flash Interface").

The addressed partition remains in CFI Query mode until a different read command is issued, or a program or erase operation is performed, which changes the read mode to Read Status Register mode.

Note: Issuing the CFI Query command to a partition that is actively programming or erasing changes that partition's read mode to CFI Query mode. Subsequent reads from that partition will return invalid data until the program or erase operation has completed

The CFI Query command functions independent of the voltage level on VPP.

9.5.5 Read Extended Flash Array (EFA)

Issuing the Read Extended Flash Array (EFA) Block command to a partition remaps that partition's block addresses to corresponding EFA block addresses. Subsequent reads from that partition output EFA data. The partition's main flash array blocks are hidden until a Read Array command (FFh) is issued to that partition. Data from EFA blocks are read using single asynchronous or synchronous non-array reads only.

Note: Issuing the Read EFA command to a partition that is actively programming or erasing changes that partition's read mode to Read EFA mode. Subsequent reads from that partition will return invalid data until the program or erase operation has completed.

The Read EFA command functions independent of the voltage level on VPP.

9.6 Programming Modes

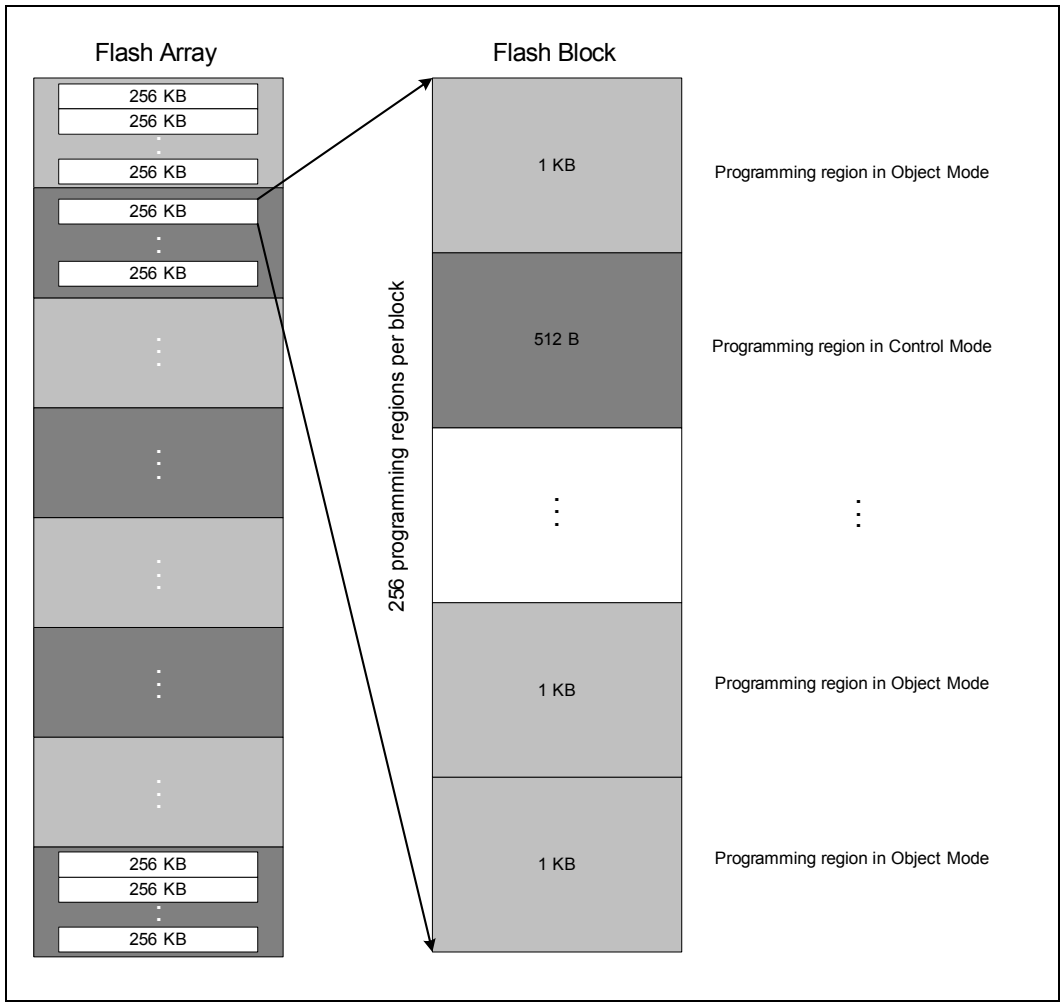
Each programming region in a flash block can be configured for one of two programming modes: Control Mode or Object Mode. Programming mode is automatically set based on the data pattern upon the first program to a blank region. Programming mode selection is driven primarily by the specific needs of the system with consideration given to two types of information:

- Control: Flash File System (FFS) or Header, frequently changing code or data
- Object: larger, infrequently changing code or data (e.g. objects or payloads)

By implementing the appropriate programming mode, software can efficiently organize how information is stored in the flash memory array.

Control Mode programming regions and Object Mode programming regions can be intermingled within the same erase block. However, the programming mode of any region within a block can be changed only after erasing the entire block. The following sections describe the two programming modes.

Figure 51. Configurable Programming Regions



9.6.1 Control Mode

Control Mode programming is invoked when only the A-half (A3 = 0) of the programming region is programmed to 0s (refer to Figure 52). The B-half (A3 = 1) remains erased. Control mode allows up to 512 bytes of data to be programmed in the region. The information can be programmed in bits, bytes, or words.

Control Mode supports the following programming methods:

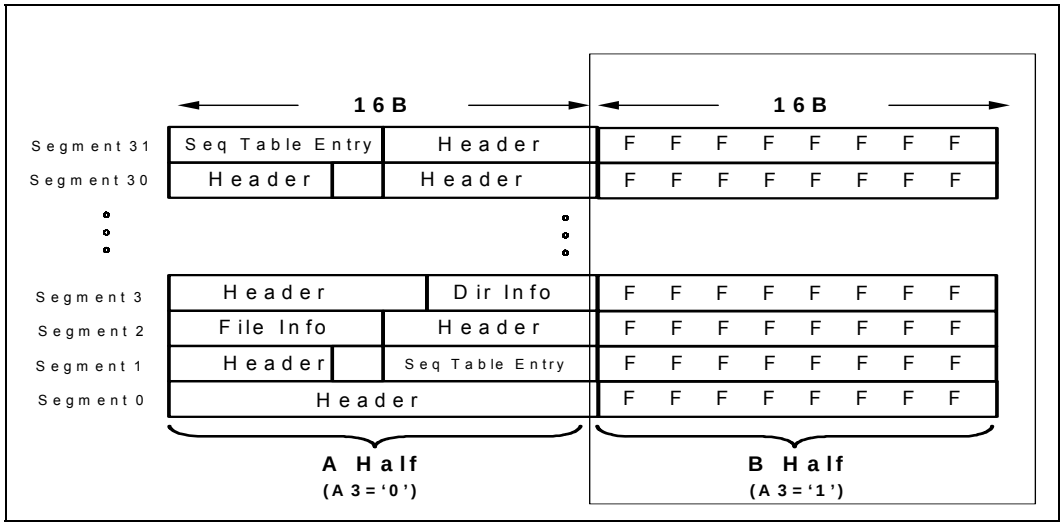
- Single-word Programming (41h)
- Buffered Programming (E9h/D0h), and
- Buffered Enhanced Factory Programming (80h/D0h)

When buffered programming is used in Control Mode, all addresses must be in the A-half of the buffer (A3 = 0). During buffer fill, the B-half (A3 = 1) addresses do not need to be filled with 0xFFFF.

Control Mode programming is useful for storing dynamic information, such as FFS Headers, File Info, etc. Typically, it does not require the entire 512 bytes of data to be programmed at once. It may also contain data that is changed after initial programming using a technique known as “bit twiddling”. Header information can be augmented later with additional new information within a Control Mode-programmed region. This allows implementation of legacy file systems, as well as transaction-based power-loss recovery.

In a control mode region, programming operations can be performed multiple times. However, care must be taken to avoid programming any zero’s in the B-half (A3 = 1) of the region. Violation of this usage will cause SR4 and SR9 to be set, and the program operation will be terminated. See Table 31, “Programming Region Next State Table” on page 81 for details.

Figure 52. Configured Programming Region in Control Mode



9.6.2 Object Mode

Object mode programming is invoked when one or more bits are programmed to zero in the B-half of the programming region (A3 = 1). Object mode allows up to 1KB to be stored in a programming region. Multiple regions are used to store more than 1Kbyte of information. If the object is less than 1Kbyte, the unused content will remain as 0xFFFF (erased).

Object Mode supports two programming methods:

- Buffered Programming (E9h/D0h), and
- Buffered Enhanced Factory Programming (80h/D0h)

Single-word programming is not supported in Object mode. To perform multiple programming operations within a programming region, Control mode must be used.

Object mode is useful for storing static information, such as objects or payloads, that rarely change.

Once the programming region is configured in Object mode, it cannot be augmented or over-written without first erasing the entire block containing the region. Subsequent programming operations to a programming region configured in Object mode will cause SR4 and SR8 to be set and the program operation to be terminated. See Table 31, “Programming Region Next State Table” on page 81 for details.

Note: Issuing the 41h command to the B-half of an erased region will set error bits SR8 and SR9, and the programming operation will not proceed. See Table 31, “Programming Region Next State Table” on page 81 for more details.

Figure 53. Configured Programming Region in Object Mode

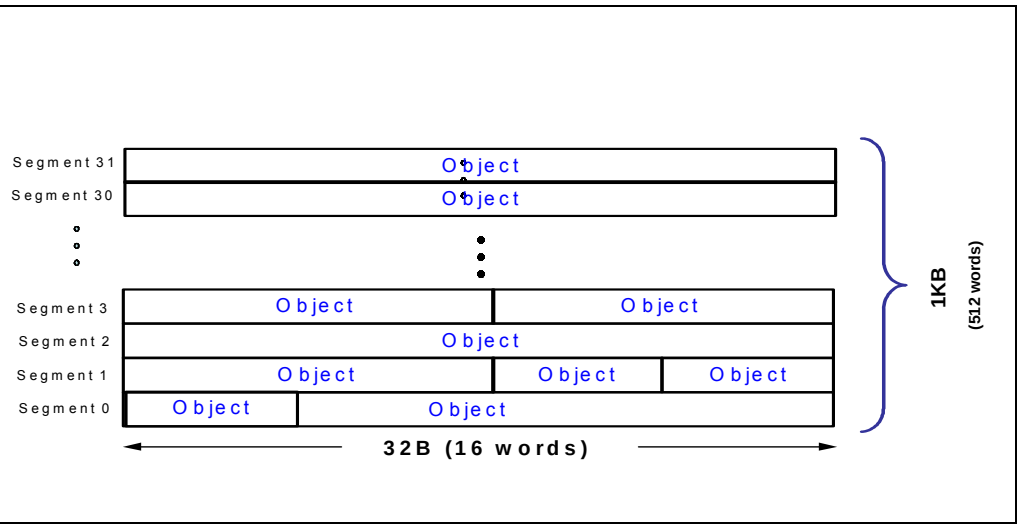


Table 31. Programming Region Next State Table

Current State of Programming region	Command Issued			
	41h to B-half (A3 = 1)	41h to A-half (A3 = 0)	E9h to B-half (A3 = 1)	E9h to A-half (A3 = 0)
Erased	Program Fail; Illegal Command SR[4,8,9] = 1	Program Successful SR[4,8,9] = 0 Region configured to Control Mode	Program Successful SR[4,8,9] = 0 Region configured to Object Mode	Program Successful SR[4,8,9] = 0 Region configured to Control Mode
Control Mode		Program Successful SR[4,8,9] = 0	Program Fail; Object data to Control mode region SR[4,9] = 1 SR8 = 0	Program Successful SR[4,8,9] = 0
Object Mode		Program Fail; Rewrite to Object mode region SR[4,8] = 1 SR9 = 0		

9.7 Programming Operations

Programming the flash array changes ‘ones’ to ‘zeros’. To change zeros to ones, an erase operation must be performed (see Section 9.8, “Block Erase Operations”). Only one programming operation can occur at a time. Programming is permitted during Erase Suspend.

Information is programmed into the flash array by issuing the appropriate command. Table 32 shows the two-cycle command sequences used for programming.

Table 32. Programming Commands Bus Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Single-Word Program	Device Address	0041h	Device Address	Array Data
Buffered Program	Device Address	00E9h	Device Address	00D0h
Buffered Enhanced Factory Program	Device Address	0080h	Device Address	00D0h
EFA Program	EFA Address	0044h	EFA Address	EFA Data

Caution: All programming operations require the addressed block to be unlocked, and a valid V_{PP} voltage applied throughout the programming operation. Otherwise, the programming operation will abort, setting the appropriate Status Register error bit(s).

The following sections describe each programming method.

9.7.1 Single-Word Programming

Main array programming is performed by first issuing the Single-Word Program command. This is followed by writing the desired data at the desired array address. The read mode of the addressed partition is automatically changed to Read Status Register mode, which remains in effect until another read-mode command is issued.

Note: Issuing the Read Status Register command to another partition switches that partition’s read mode to Read Status Register mode, thereby allowing programming progress to be monitored from that partition’s address.

Single-Word Programming is supported in Control mode only. The programming array address specified must be in the A-half of the programming region.

During programming, the Status Register indicates a busy status (SR7 = 0b). Upon completion, the Status Register indicates a ready status (SR7 = 1b). The Status Register should be checked for any errors, then cleared.

The only valid commands during programming are Read Array, Read Device Information, CFI Query, Read Status and Program Suspend. After programming has finished, any valid command can be issued.

Note: Issuing the Read Array command to a partition that is actively programming causes subsequent reads from that partition to output invalid data. Valid array data is output only after the program operation has finished.

Standby power levels are not realized until the programming operation has finished. Asserting RST# immediately aborts the programming operation, and array contents at the addressed location are indeterminate. The addressed block should be erased, and the data re-programmed.

9.7.2 Buffered Programming

Buffered Programming programs multiple words simultaneously into the flash memory array. Data is first written to a write buffer and then programmed into the flash memory array in buffer-size increments. This can significantly reduce the effective word-write time. Appendix C, "Flow Charts" contains a flow chart of the buffered-programming operation.

Buffered Programming is supported in both Control mode and Object mode. In Object mode, the region must be programmed only once between erases. However in Control mode, the region may be programmed multiple times.

Caution: When using the Buffered Program command in Object mode, the start address must be aligned to the 512-word buffer boundary. In Control mode, the programming array address specified must be in the A-half of the programming region.

To perform a buffered programming operation, first issue the Buffered Program setup command at the desired starting address.

Poll SR7 to determine write-buffer availability (0 = not available, 1 = available). If the write buffer is not available, re-issue the setup command and check SR7; repeat until SR7 = 1.

Next, issue a word count at the desired starting address. The word count is the total number of words to be written into the write buffer, minus one. This value can range from 00h (one word) up to a maximum of 1FF (512 words). Exceeding the allowable range causes the higher order data bits to be ignored.

Following the word count, subsequent bus-write cycles fill the write buffer with user-data up to the word count.

Note: User-data is programmed into the flash array at the address issued when filling the write buffer.

The Confirm command is issued after all user-data is written into the write buffer. The read mode of the device/addressed partition is automatically changed to Read Status Register mode. If other than the Confirm command is issued to the device, a command sequence error occurs and the operation aborts.

After the Confirm command has been issued, the write-buffer contents are programmed into the flash memory array. The Status Register indicates a busy status (SR7 = 0) during array programming.

During array programming, the only valid commands are Read Array, Read Device Information, CFI Query, Read Status, and Program Suspend. After array programming has completed (SR7 = 1), any valid command can be issued. Reading from another partition is allowed while data is being programmed into the flash memory array from the write buffer.

Note: Issuing the Read Array command to a partition that is actively programming or erasing causes subsequent reads from that partition to output invalid data. Valid array data is output only after the program or erase operation has finished.

Upon completion of array programming, the Status Register indicates ready (SR7 = 1b). A full Status Register check should be performed to check for any programming errors. Then the Status Register should be cleared using the Clear Status Register command.

A subsequent buffered programming operation can be initiated by issuing another setup command, and repeating the buffered programming sequence. Any errors in the Status Register caused by the previous operation must be cleared to prevent them from masking any errors that may occur during the subsequent operation.

9.7.3 Buffered Enhanced Factory Programming (BEFP)

Buffered Enhanced Factory Programming (BEFP) improves programming performance through the use of the write buffer, $V_{PPH}$and enhanced programming algorithm. User-data is written into the write buffer, then the buffer contents are automatically written into the flash array in buffer-size increments.

BEFP is allowed in both Control Mode and Object Mode. The programming mode selection for the entire flash array block is driven by the specific type of information, e.g., header or object data.

Each 1KB of header or object data is configured to an aligned 1KB programming region to fill the entire main array block. The code/data pattern for headers does not contain zeros in the A3 = 1 addresses, and the code/data pattern for objects does contain zeros in the A3 = 1 addresses.

Internal verification during programming (inherent to MLC technology) and Status Register error checking are used to determine proper completion of the programming operation. This eliminates delays incurred when switching between single-word program and verify operations.

BEFP consists of three distinct phases:

1. Setup Phase: V_{PPH} and block-lock checks
2. Program/Verify Phase: buffered programming and verification
3. Exit Phase: block-error check

Appendix C, “Flow Charts” contains a flow chart of the BEFP operation. Table 33 lists specific BEFP requirements and considerations.

Table 33. BEFP Requirements and Considerations

BEFP Requirements	Temperature (T_{CASE}) must be 25 °C, ± 5 °C
	Voltage on V_{CC} must be within the allowable operating range
	Voltage on VPP must be within the allowable operating range [1]
	Block being programmed must be erased and unlocked
BEFP Considerations	Block cycling below 100 erase cycles [2]
	Reading from another partition during EFP (RWW) is not allowed
	BEFP programs within one block at a time
	BEFP cannot be suspended

Notes:

1. V_{PP} restrictions apply. See Section 5.0, “Maximum Ratings and Operating Conditions”.
2. Recommended for optimal BEFP performance. If exceeded, some degradation in performance may occur, however, the internal algorithm will still function properly.

9.7.3.1 Setup Phase

Issuing the BEFP Setup and Confirm command sequence starts the BEFP algorithm. The read mode of the addressed partition is automatically changed to Read Status Register mode.

The address used when issuing the setup/confirm commands must be buffer-size aligned within the block being programmed -- buffer contents cannot cross block boundaries.

Caution: The Read Status Register command must not be issued -- it will be interpreted as data to be written to the write buffer.

A setup delay ($t_{BEFP/Setup}$) occurs while the internal algorithm checks V_{PP} and block-lock status. If errors are detected, the appropriate Status Register error bits are set and the operation aborts.

The Status Register should be polled for successful BEFP setup, indicated by SR[7,0] = 0 (Device Busy, Buffer Ready for Data).

9.7.3.2 Program/Verify Phase

Data is first written into the write buffer, then programmed into the flash array. During the buffer-fill sequence, the address used must be buffer-size aligned. Use of any other address will cause the operation to abort with a program fail error, and any data previously loaded in the buffer will not be programmed into the array.

The buffer-fill data is stored in sequential buffer locations starting at address 00h. A word count equal to the maximum buffer size is used, therefore, the buffer must be completely filled. If the amount of data is less than the maximum buffer size, the remaining buffer locations must be “padded” with FFFFh to completely fill the buffer.

Flash array programming starts as soon as the write buffer is full. Data words from the write buffer are programmed into sequential array locations. SR0 = 1 indicates the write buffer is not available while the BEFP algorithm programs the array.

The Status Register should be polled for SR0 = 0 (Buffer Ready for Data) to determine when the array programming has completed, and the write buffer is again available for loading. The internal address is automatically incremented to enable subsequent array programming to continue from where the previous buffer-fill/array-program sequence ended within the block. This cycle can be repeated to program the entire block.

To exit the Program/Verify Phase, write FFFFh to an address outside of the block.

9.7.3.3 Exit Phase

The Status Register should be polled for SR7 = 1 (Device Ready) indicating the BEFP algorithm has finished running, and the device has returned to normal operation. A full error check should be performed to ensure the block was programmed successfully.

9.7.4 EFA Word Programming

EFA programming is performed by first issuing the EFA Program command. This is followed by writing the desired data at the desired EFA address. This places the EFA plane in the foreground in the addressed partition. The read mode of the addressed partition is changed to Read Status Register mode, which remains in effect until another read-mode command is issued.

Note: Issuing the Read Status Register command to any other partition switches that partition's read mode to the Read Status Register, thereby allowing programming progress to be monitored from that partition's address.

During programming, the Status Register indicates a busy status (SR7 = 0). Upon completion, the Status Register indicates a ready status (SR7 = 1). The Status Register should be checked for any errors, then cleared.

Issuing the EFA Program command outside of the EFA block address range results in the Status Register indicating a program error.

The only valid commands during programming are Read Array, Read Device Information, CFI Query, Read Status and Program Suspend. After programming has finished, any valid command can be issued.

Note: Issuing the Read Array command to a EFA-mapped partition that is actively programming causes subsequent reads from that partition to output invalid data. Valid array data is output only after the program operation has finished.

Standby power levels are not be realized until the programming operation has finished. Also, asserting RST# aborts the programming operation, and array contents at the addressed location are indeterminate. The addressed block should be erased, and the data re-programmed.

9.8 Block Erase Operations

Erasing a block changes 'zeros' to 'ones'. To change ones to zeros, a program operation must be performed (see Section 9.7, "Programming Operations"). Erasing is performed on a block basis—an entire block is erased each time an erase command sequence is issued. Once a block is fully erased, all addressable locations within that block read as logical 'ones' (FFFFh).

Only one block-erase operation can occur at a time. A block-erase operation is not permitted during Program Suspend.

To perform a block-erase operation, issue the Block Erase or EFA Block Erase command sequence at the desired block address. Table 34 shows the two-cycle Block Erase command sequence.

Table 34. Block-Erase Command Bus Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Block Erase	Device Address	0020h	Block Address	00D0h
EFA Block Erase	EFA Address	0024h	EFA Block Address	00D0h

Erase operations performed on EFA blocks are similar to erase operations performed on main-array blocks. Issuing the EFA Block Erase command places the EFA plane in the foreground of the corresponding partition.

Issuing the EFA Block Erase command outside of the EFA plane's address range causes the operation to abort, and the Status Register indicates an erase error (SR[7,5] = 1).

Caution: All block-erase operations require the addressed block to be unlocked, and a valid voltage applied to VPP throughout the block-erase operation. Otherwise, the operation aborts, setting the appropriate Status Register error bit(s).

The Erase Confirm command latches the address of the block to be erased. The addressed block is preconditioned (programmed to all zeros), erased, and then verified. The read mode of the addressed partition is automatically changed to Read Status Register mode, and remains in effect until another read-mode command is issued.

Note: Issuing the Read Status Register command to another partition switches that partition's read mode to the Read Status Register, thereby allowing block-erase progress to be monitored from that partition's address. SR0 indicates whether the addressed partition or other partition is erasing.

During a block-erase operation, the Status Register indicates a busy status (SR7 = 0). Upon completion, the Status Register indicates a ready status (SR7 = 1). The Status Register should be checked for any errors, and then cleared. If any errors did occur, subsequent erase commands to that partition are ignored unless the Status Register is cleared.

The only valid commands during a block erase operation are Read Array, Read Device Information, CFI Query, Read Status and Erase Suspend. After the block-erase operation has completed, any valid command can be issued.

Note: Issuing the Read Array command to a partition that is actively erasing a main block or EFA block causes subsequent reads from that partition (or EFA-mapped partition) to output invalid data. Valid array data is output only after the block-erase operation has finished.

Standby power levels are not realized until the block-erase operation has finished. Asserting RST# immediately aborts the block-erase operation, and array contents at the addressed location are indeterminate. The addressed block should be erased, and the data re-programmed.

9.9 Blank Check Operation

Blank Check is used to see if a main-array block is completely erased. Blank Check for EFA blocks is not supported . A Blank Check operation is performed one block at a time, and cannot be used during Program Suspend or Erase Suspend.

Blank Check speeds up flash programming and reclaim in customer manufacturing flows. Automated programmer systems can use this one-step method instead of slower sequential reads of the entire block. This operation should not be used to determine erase-operation success or failure, such as after an aborted erase.

To use Blank Check, first issue the Blank Check setup command (see Table 35) followed by the confirm command. The read mode of the addressed partition is automatically changed to Read Status Register mode, which remains in effect until another read-mode command is issued.

Table 35. Blank Check Command Bus Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Blank Check	Block Address	00BCh	Block Address	00D0h

During a blank check operation, the Status Register indicates a busy status (SR7 = 0). Upon completion, the Status Register indicates a ready status (SR7 = 1).

Note: Issuing the Read Status Register command to another partition switches that partition's read mode to Read Status Register mode, thereby allowing the blank check operation to be monitored from that partition's address.

The Status Register should be checked for any errors, and then cleared. If the Blank Check operation fails, i.e., the block is not completely erased, then the Status Register will indicate a Blank Check error (SR[7,5] = 1).

The only valid command during a Blank Check operation is Read Status. Blank Check cannot be suspended. After the blank check operation has completed, any valid command can be issued.

9.10 Suspend and Resume

Program and erase operations of the main array or EFA can be suspended to perform other device operations, and then subsequently resumed. However, OTP Register programming or blank check operations cannot be suspended.

To suspend an on-going erase or program operation, issue the Suspend command to any device address; the corresponding partition is not affected. Table 36 shows the Suspend and Resume command bus-cycles.

Note: Issuing the Suspend command does not change the read mode of the partition. The partition will be in Read Status Register mode from when the erase or program command was first issued, unless the read mode was changed prior to issuing the Suspend command.

Table 36. Suspend and Resume Command Bus Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Suspend	Device Address	00B0h	---	---
Resume	Device Address	00D0h	---	---

The program or erase operation suspends at pre-determined points during the operation after a delay of t_{SUSP}. Suspend is achieved when SR[7,6] = 1 (erase-suspend) or SR[7,2] = 1 (program-suspend).

Note: Throughout the Block Erase Suspend or Program Suspend period, the addressed block must remain unlocked and a valid voltage applied to VPP. Otherwise, the erase or program operation will abort, setting the appropriate Status Register error bit(s). Also, WP# must remain unchanged.

Asserting RST# aborts suspended block-erase and programming operations -- array contents at the addressed locations are indeterminate. The addressed block should be erased, and the data re-programmed.

Not all commands are allowed when the device is suspended. Table 37 shows which device commands are allowed during Program Suspend or Erase Suspend.

Table 37. Valid Commands During Suspend

Device Command	Program Suspend	Erase Suspend
Read Array	Allowed	Allowed
Read Status Register	Allowed	Allowed
Clear Status Register	Allowed	Allowed
Read Device Information	Allowed	Allowed
CFI Query	Allowed	Allowed
Word Program / EFA Program	Not Allowed	Allowed
Buffered Program	Not Allowed	Allowed
Buffered Enhanced Factory Program	Not Allowed	Not Allowed
Block Erase / EFA Erase	Not Allowed	Not Allowed
Program/Erase Suspend	Not Allowed	Not Allowed
Program/Erase Resume	Allowed	Allowed

During Suspend, main array-read and EFA-read operations are not allowed in blocks being erased or programmed. Also, programming operations are not allowed in blocks in erase-suspend state and if attempted, will result in Status Register program error to be set (SR4 = 1).

A block-erase under program-suspend is not allowed. However, word-program under erase-suspend is allowed, and can be suspended. This results in a simultaneous erase-suspend/ program-suspend condition, indicated by SR[7,6,2] = 1.

To resume a suspended program or erase operation, issue the Resume command to any device address. The read mode of the resumed partition is unchanged; issue the Read Status Register command to return the partition to Read Status mode. The operation continues where it left off, and the respective Status Register suspend bits are cleared.

When the Resume command is issued during a simultaneous erase-suspend/ program-suspend condition, the programming operation is resumed first. Upon completion of the programming operation, the Status Register should be checked for any errors, and cleared. The resume command must be issued again to complete the erase operation. Upon completion of the erase operation, the Status Register should be checked for any errors, and cleared.

9.11 Simultaneous Operations

The multi-partition architecture of the flash device allows programming or erasing to occur in one partition while reads are performed from another partition. Only status reads are allowed in partitions that are busy programming or erasing.

Note: When OTP Register or EFA commands are issued to any partition address, the OTP Register or EFA plane is mapped onto that partition.

Table 38 shows the rules for reading from a partition while simultaneously programming or erasing within another partition.

Table 38. Read-While-Program and Read-While-Erase Rules

	Read modes allowed when program/erase busy in partition A		
Active Operation	**Read Status**	**Array Reads**	**Non-Array Reads[1]**
Main-Array Program	All partitions	All partitions except busy partition A	All partitions except busy partition A
Main-Array Erase	All partitions	All partitions except busy partition A	All partitions except busy partition A
OTP Register Program	All partitions	All partitions except busy partition A	Not allowed
EFA Program or Erase	All partitions	All partitions except busy partition A	Not allowed

Notes:
1. OTP Register, Device Information, CFI Query, EFA.

Table 39. Simultaneous Operation Restrictions

OTP Register or CFI	Parameter Partition Array Data	Other Partitions	Notes
Read	(See Notes)	Write/Erase	While programming or erasing in a main partition, the Protection Register or CFI data may be read from any other partition. Reading the parameter partition array data is not allowed if the Protection Register or Query data is being read from addresses within the parameter partition.
(See Notes)	Read	Write/Erase	While programming or erasing in a main partition, read operations are allowed in the parameter partition. Accessing the Protection Registers or CFI data from parameter partition addresses is not allowed when reading array data from the parameter partition.
Read	Read	Write/Erase	While programming or erasing in a main partition, read operations are allowed in the parameter partition. Accessing the Protection Registers or CFI data in a partition that is *different* from the one being programed/erased, and also *different* from the parameter partition is allowed.
Write	No Access Allowed	Read	While programming the Protection Register, reads are only allowed in the other main partitions. Access to array data in the parameter partition is not allowed. Programming of the Protection Register can only occur in the parameter partition, which means this partition is in Read Status.
No Access Allowed	Write/Erase	Read	While programming or erasing the parameter partition, reads of the Protection Registers or CFI data are not allowed in *any* partition. Reads in partitions other than the parameter partition are supported.

9.12 Security

The flash device incorporates features for protecting main-array contents and for implementing system-level security schemes. The following sections describe the available features.

9.12.1 Block Locking

Upon power up or exit from reset, all main array and EFA blocks are locked, but not locked down. Locked blocks cannot be erased or programmed.

Two methods of block-lock control are available: software and hardware. Software control uses the Block Lock and Block Unlock commands; hardware control uses WP# along with the Block Lock-Down command.

Block lock and unlock operations are independent of the voltage level on V_{PP}.

Table 40 summarizes the command bus-cycles.

Table 40. Block Locking Command Bus Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Lock Block	Block Address	0060h	Block Address	0001h
Unlock Block	Block Address	0060h	Block Address	00D0h
Lock-Down Block	Block Address	0060h	Block Address	002Fh
Lock EFA Block	Block Address	0064h	Block Address	0001h
Unlock EFA Block	Block Address	0064h	Block Address	00D0h
Lock-Down EFA Block	Block Address	0064h	Block Address	002Fh

To lock, unlock, or lock-down a block, first issue the setup command to any address within the desired block. The read mode of the addressed partition is automatically changed to Read Status Register mode. Next, issue the desired confirm command to the block's address. Note that the confirm command determines the operation performed. The Status Register should be checked for any errors, and then cleared.

The lock status of a block can be determined by issuing the Read Device Information command, and then reading from <block base address> + 02h. DQ0 indicates the lock status of the addressed block (0 = unlocked, 1 = locked), and DQ1 indicates the lock-down status of the addressed block (0 = lock-down not issued; 1 = locked-down issued). Section 9.5.3, "Read Device Information" on page 77 summarizes the details of this operation.

Blocks cannot be locked or unlocked while being actively programmed or erased. Blocks can be locked or unlocked during erase-suspend, but not during program-suspend.

Note: If a block-erase operation is suspended, and then the block is locked or locked down, the lock status of the block will be changed immediately. When resumed, the erase operation will still complete.

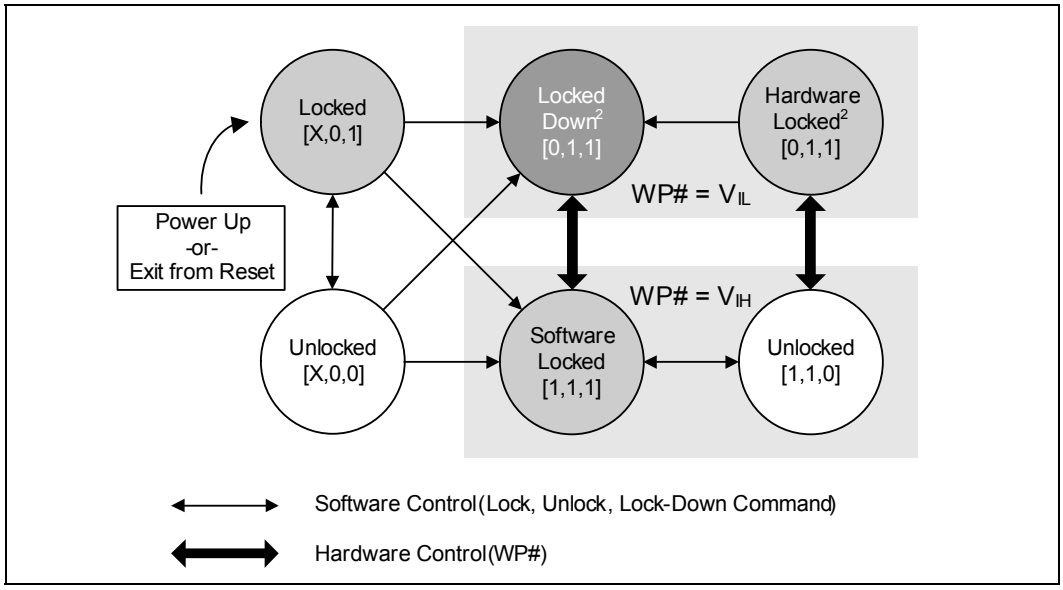
Block lock-down protection is dependent on WP#. When WP# = V_{IL}, blocks locked down are locked, and cannot be unlocked using the Block Unlock command. When WP# = V_{IH}, block lock-down protection is disabled - locked-down blocks can be individually unlocked using the Block

Unlock command. Subsequently, when WP# = V_{IL}, previously locked-down blocks are once again locked and locked-down, including locked-down blocks that may have been unlocked while WP# was de-asserted.

A locked-down block can only be unlocked by issuing the Unlock Block command with WP# deasserted. To return an unlocked block to the locked-down state, a Lock-Down command must be issued prior to asserting WP#.

Issuing the Block Lock-Down command to an unlocked block does not lock the block. However, asserting WP# after issuing the Block Lock-Down command locks (and locks down) the block. Lock-down for all blocks is cleared upon power-up or exit from reset. Figure 54 summarizes block-locking operations.

Figure 54. Block Locking Operations



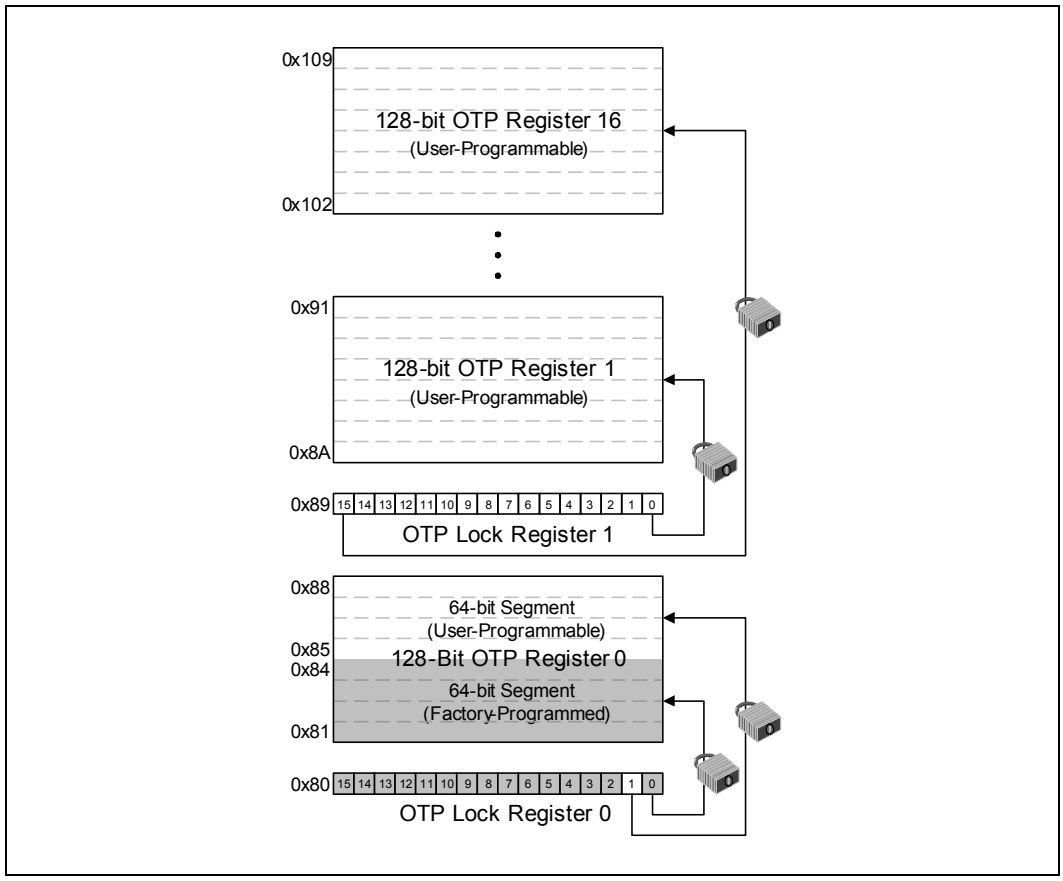
Notes:
1. [n,n,n] denotes logical state of WP#, DQ1,and DQ0, respectively; X = Don't Care.
2. [0,1,1] states should be tracked by system software to differentiate between the Hardware-Locked state and the Lock-Down state.

9.12.2 One-Time Programmable (OTP) Registers

The device contains seventeen 128-bit One-Time Programmable (OTP) Registers, and two 16-bit OTP Lock Registers, as shown in Figure 55, "2-Kbit OTP Registers" on page 93. OTP Lock Register 0 is used for locking OTP Register 0, and OTP Lock Register 1 is used for locking OTP Registers 1 through 16.

OTP Register 0 consists of two 64-bit segments: a lower segment that is pre-programmed with a unique 64-bit value and locked at the factory; and an upper segment that contains all "ones" and is user-programmable. OTP Registers 1 through 16 contain all "ones" and are user-programmable.

Figure 55. 2-Kbit OTP Registers



Each register contains OTP bits that can only be programmed from “one” to “zero” - register bits cannot be erased from “zero” back to “one”. This feature makes the OTP registers particularly useful for implementing system-level security schemes, for permanently storing data, or for storing fixed system parameters.

OTP Lock Register bits “lock out” subsequent programming of the corresponding OTP register. Each OTP Register can be locked by programming its corresponding lock bit to zero. As long as an OTP register remains unlocked (i.e., its lock bit = 1), any of its remaining “one” bits can be programmed to “zero”.

Caution: Once an OTP Register is locked, it cannot be unlocked. Attempts to program a locked OTP Register will fail with error bits set.

To program any OTP bits, first issue the Program OTP Register setup command at any device address (see Table 41). Next, write the desired OTP Register data at the desired OTP Register address. OTP Register and OTP Lock Register programming is performed 16 bits at a time; only “zeros” within the data word affect any change to the OTP register bits.

Table 41. Program OTP Register Command Bus Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Program OTP Register	Device Address	00C0h	OTP Register Address	Register Data

Attempting to program an OTP register outside of the OTP register space causes a program error (SR4 = 1). Attempting to program a locked OTP Register causes a program error and a lock error (SR4 = 1, SR1 = 1).

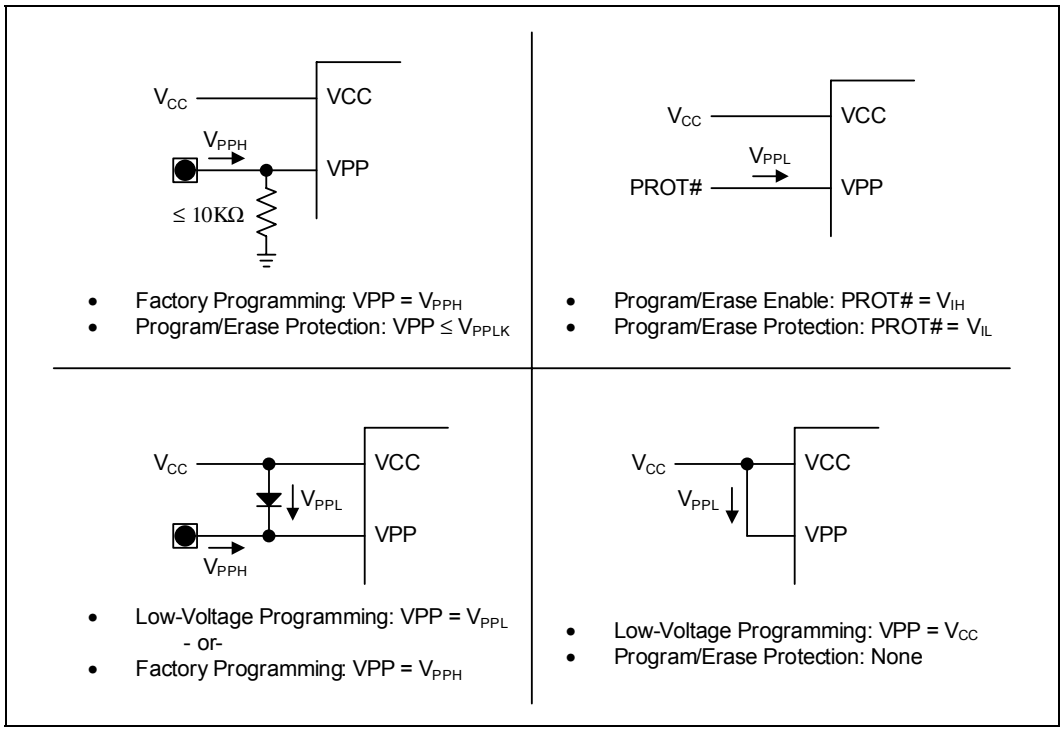
To read from any of the OTP registers, first issue the Read Device Information command. Then read from the desired OTP Register address offset. For additional details, refer to Section 9.5.3, "Read Device Information" on page 77.

9.12.3 Global Main-Array Protection

Global main-array protection can be implemented by controlling V_{PP}. When programming or erasing main-array or EFA blocks, V_{PP} must be equal to, or greater than, the lock-out voltage, V_{PPLK}. When V_{PP} is below V_{PPLK}, program or erase operations are inhibited, thus providing absolute protection of the main array.

Various methods exist for controlling V_{PP}, ranging from simple logic control to off-board voltage control. Figure 56 shows example V_{PP} supply connections that can be used to support program/erase operations and main-array protection.

Figure 56. Example VPP Supply Connections



Appendix A Device Command Codes

A.1 Flash Command Codes

Table 42. Command Bus Operations (Sheet 1 of 2)

Command		Code (Setup/ Confirm)	Description
Registers	Program Read Configuration Register	0060h/ 0003h	Issuing this command sequence programs the Read Configuration Register. The RCR value is placed on the address bus.
	Program Enhanced Configuration Register	0060h/ 0004h	Issuing this command sequence programs the Enhanced Configuration Register. The ECR value is placed on the address bus.
	Program OTP Register	00C0h	Issuing this command programs the Protection Registers or the Lock Registers associated with them.
Read Modes	Read Array	00FFh	Issuing this command places the addressed partition in Read Array mode. Subsequent reads outputs array data.
	Read Status Register	0070h	Issuing this command places the addressed partition in Read Status mode. Subsequent reads outputs Status Register data.
	Clear Status Register	0050h	Issuing this command clears all error bits in the Status Register.
	Read Device Information	0090h	Issuing this command places the addressed partition in Read Device Information mode. Subsequent reads from specified address offsets outputs unique device information.
	CFI Query	0098h	Issuing this command places the addressed partition in CFI Query mode. Subsequent reads from specified address offsets outputs CFI data.
Program/Erase Operations	Word Program	0041h	This command prepares the device for programming a single word into the flash array. On the next bus write cycle, the address and data are latched and written to the flash array. The addressed partition automatically switches to Read Status Register mode.
	Buffered Program	00E9h/ 00D0h	This command sequence initiates and executes a buffered programming operation. Additional bus write/read cycles are required between the setup and confirm commands to properly perform this operation. The addressed partition automatically switches to Read Status Register mode.
	Buffered Enhanced Factory Program	0080h/ 00D0h	This command sequence initiates and executes a BEFP operation. Additional bus write/read cycles are required after the confirm command to properly perform the operation. The addressed partition automatically switches to Read Status Register mode.
	Block Erase	0020h/ 00D0h	Issuing this command sequence erases the addressed block. The addressed partition automatically switches to Read Status mode.
	Program/Erase Suspend	00B0h	Issuing this command to any device address *initiates* a suspend of a program or block-erase operation already in progress. SR6 = 1 indicates erase suspend, and SR2 = 1 indicates program suspend.
	Program/Erase Resume	00D0h	Issuing this command to any device address resumes a suspended program or block-erase operation. A program suspend nested within an erase suspend is resumed first.
	Blank Check	00BCh/ 00D0h	This command sequence initiates the blank check operation on a block.

Table 42. Command Bus Operations (Sheet 2 of 2)

Command		Code (Setup/ Confirm)	Description
Security	Lock Block	0060h/ 0001h	Issuing this command sequence sets the lock bit of the addressed block.
	Unlock Block	0060h/ 00D0h	Issuing this command sequence clears the lock bit of the addressed block.
	Lock Down Block	0060h/ 002Fh	Issuing this command sequence locks down the addressed block.
Extended Flash Array	Read EFA	0094h	Issuing this command places the addressed partition in Read EFA mode. Subsequent reads outputs EFA data.
	Program EFA	0044h	This command prepares the device for programming a single word into the Extended Flash Array. On the next bus write cycle, the address and data are latched and written to the EFA. The addressed partition automatically switches to Read Status Register mode.
	Erase EFA	0024h/ 00D0h	Issuing this command sequence erases the addressed block in the EFA. The addressed partition automatically switches to Read Status mode.
	Lock EFA Block	0064h/ 0001h	Issuing this command sequence sets the lock bit of the addressed block in the EFA.
	Unlock EFA Block	0064h/ 00D0h	Issuing this command sequence clears the lock bit of the addressed block in the EFA.
	Lock Down EFA Block	0064h/ 002Fh	Issuing this command sequence locks down the addressed block in the EFA.

Appendix B Device ID Codes

The following table lists the Device ID codes for the Intel StrataFlash® Cellular Memory.

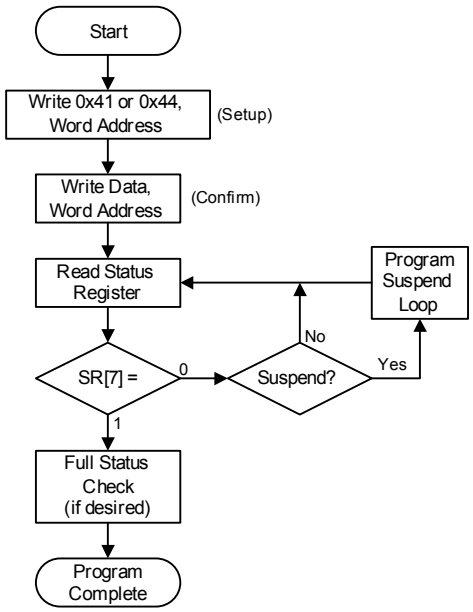
Table 43. Device ID codes

Density	Product	Device Identifier Code (Hex)
512 Mbit	Non-Mux	887E
	AD-Mux	8881
256 Mbitt	Non-Mux	8901
	AD-Mux	8904

Appendix C Flow Charts

Figure 57. Word Program for Main Array and EFA Flowchart

WORD PROGRAM PROCEDURE



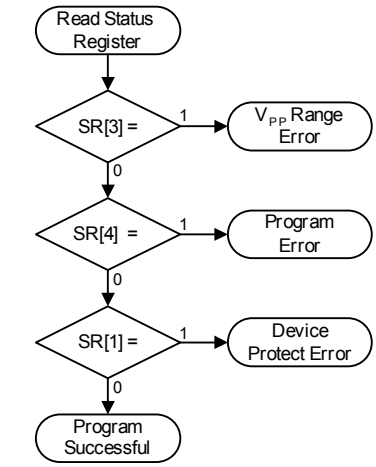
Bus Operation	Command	Comments
Write	Program Setup	Data = 0x41 or 0x44 Addr = Location to program
Write	Data	Data = Data to program Addr = Location to program
Read	None	Status register data
Idle	None	Check SR[7] 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent Word Program operations.

Full Status Register check can be done after each program, or after a sequence of program operations.

Write 0xFF after the last operation to set to the Read Array state.

FULL STATUS CHECK PROCEDURE

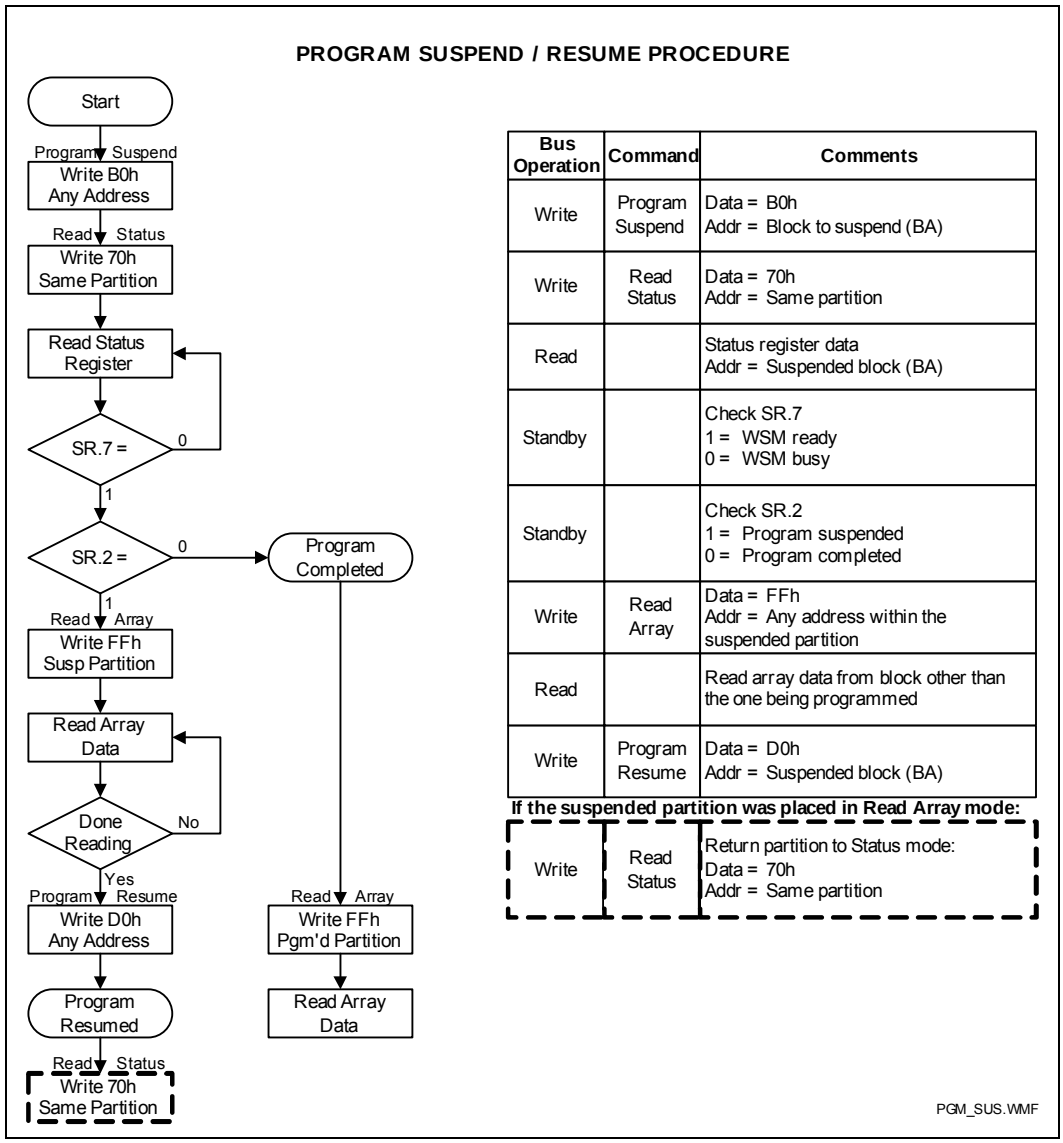


Bus Operation	Command	Comments
Idle	None	Check SR[3]: 1 = V_{PP} Error
Idle	None	Check SR[4]: 1 = Data Program Error
Idle	None	Check SR[1]: 1 = Block locked; operation aborted

SR[3] MUST be cleared before the Write State Machine will allow further program attempts.

If an error is detected, clear the Status Register before continuing operations - only the Clear Staus Register command clears the Status Register error bits.

Figure 58. Program Suspend/Resume Flowchart

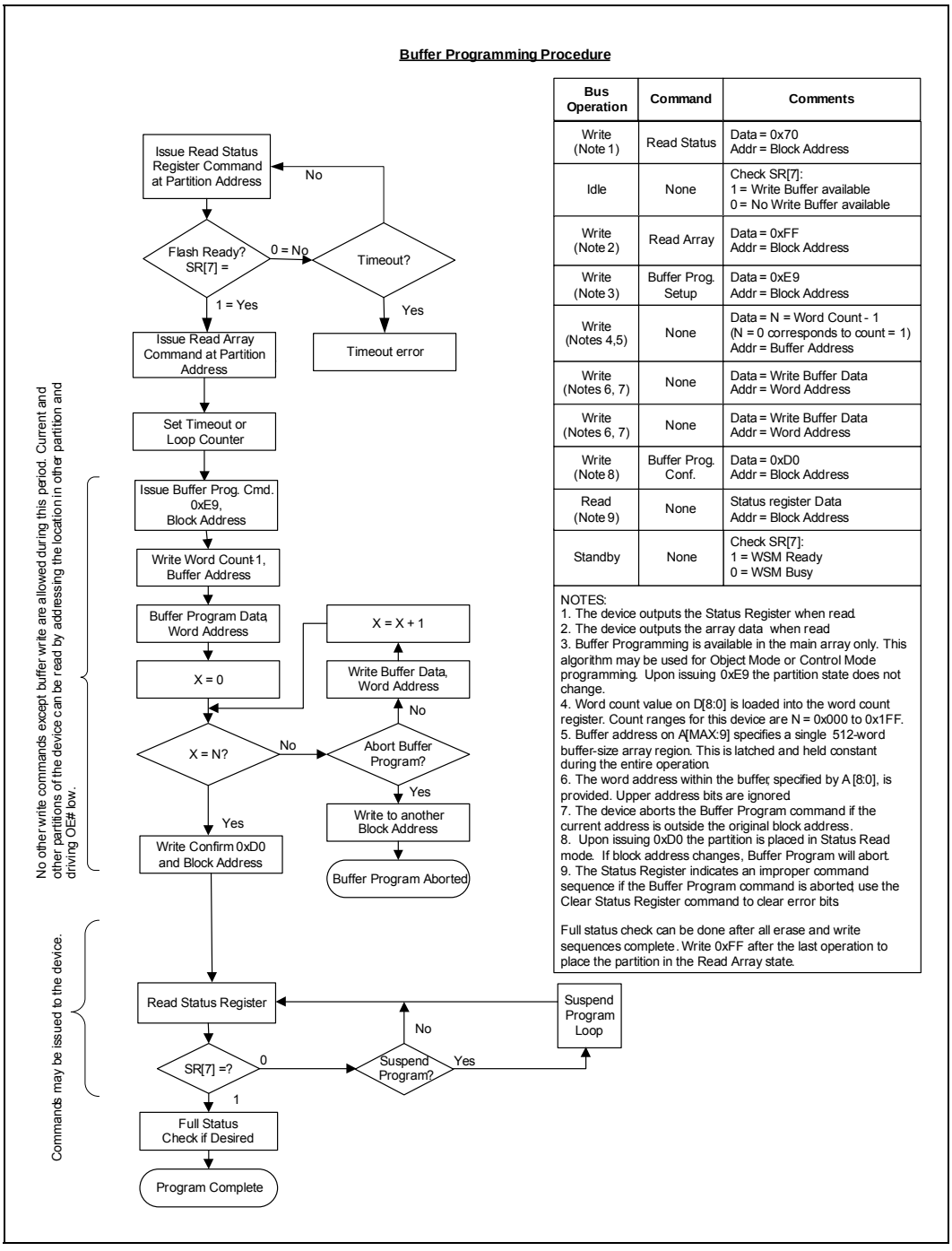


Bus Operation	Command	Comments
Write	Program Suspend	Data = B0h Addr = Block to suspend (BA)
Write	Read Status	Data = 70h Addr = Same partition
Read		Status register data Addr = Suspended block (BA)
Standby		Check SR.7 1 = WSM ready 0 = WSM busy
Standby		Check SR.2 1 = Program suspended 0 = Program completed
Write	Read Array	Data = FFh Addr = Any address within the suspended partition
Read		Read array data from block other than the one being programmed
Write	Program Resume	Data = D0h Addr = Suspended block (BA)

If the suspended partition was placed in Read Array mode:

Write	Read Status	Return partition to Status mode: Data = 70h Addr = Same partition

Figure 59. Buffered Program Flowchart

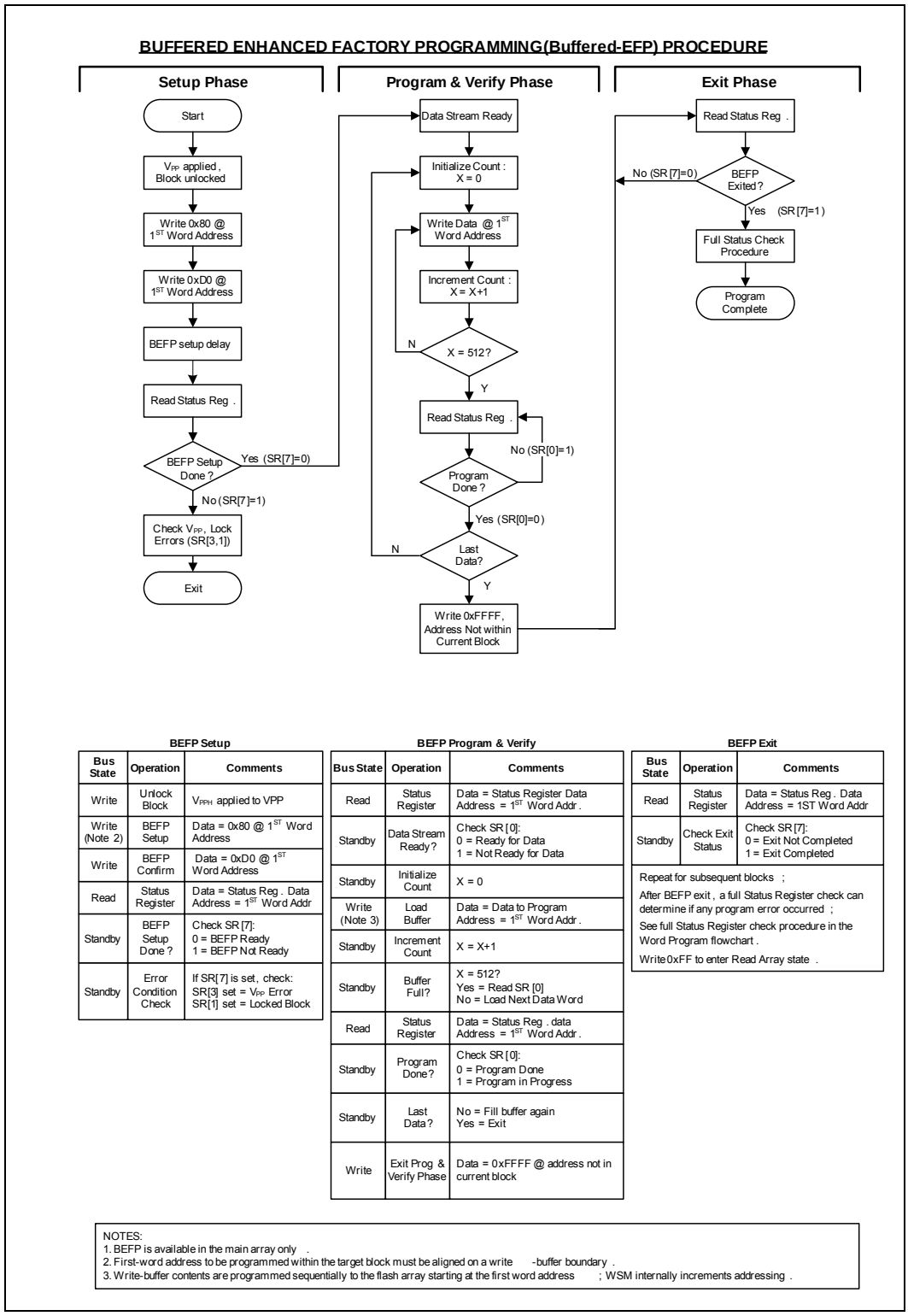


Bus Operation	Command	Comments
Write (Note 1)	Read Status	Data = 0x70 Addr = Block Address
Idle	None	Check SR[7]: 1 = Write Buffer available 0 = No Write Buffer available
Write (Note 2)	Read Array	Data = 0xFF Addr = Block Address
Write (Note 3)	Buffer Prog. Setup	Data = 0xE9 Addr = Block Address
Write (Notes 4,5)	None	Data = N = Word Count - 1 (N = 0 corresponds to count = 1) Addr = Buffer Address
Write (Notes 6, 7)	None	Data = Write Buffer Data Addr = Word Address
Write (Notes 6, 7)	None	Data = Write Buffer Data Addr = Word Address
Write (Note 8)	Buffer Prog. Conf.	Data = 0xD0 Addr = Block Address
Read (Note 9)	None	Status register Data Addr = Block Address
Standby	None	Check SR[7]: 1 = WSM Ready 0 = WSM Busy

NOTES:
1. The device outputs the Status Register when read.
2. The device outputs the array data when read.
3. Buffer Programming is available in the main array only. This algorithm may be used for Object Mode or Control Mode programming. Upon issuing 0xE9 the partition state does not change.
4. Word count value on D[8:0] is loaded into the word count register. Count ranges for this device are N = 0x000 to 0x1FF.
5. Buffer address on A[MAX:9] specifies a single 512-word buffer-size array region. This is latched and held constant during the entire operation.
6. The word address within the buffer, specified by A [8:0], is provided. Upper address bits are ignored.
7. The device aborts the Buffer Program command if the current address is outside the original block address.
8. Upon issuing 0xD0 the partition is placed in Status Read mode. If block address changes, Buffer Program will abort.
9. The Status Register indicates an improper command sequence if the Buffer Program command is aborted, use the Clear Status Register command to clear error bits.

Full status check can be done after all erase and write sequences complete. Write 0xFF after the last operation to place the partition in the Read Array state.

Figure 60. Buffered EFP Flowchart



BEFP Setup

Bus State	Operation	Comments
Write	Unlock Block	V_{PPH} applied to VPP
Write (Note 2)	BEFP Setup	Data = 0x80 @ 1ST Word Address
Write	BEFP Confirm	Data = 0xD0 @ 1ST Word Address
Read	Status Register	Data = Status Reg . Data Address = 1ST Word Addr
Standby	BEFP Setup Done ?	Check SR[7]: 0 = BEFP Ready 1 = BEFP Not Ready
Standby	Error Condition Check	If SR[7] is set, check: SR[3] set = V_{PP} Error SR[1] set = Locked Block

BEFP Program & Verify

Bus State	Operation	Comments
Read	Status Register	Data = Status Register Data Address = 1ST Word Addr .
Standby	Data Stream Ready?	Check SR[0]: 0 = Ready for Data 1 = Not Ready for Data
Standby	Initialize Count	X = 0
Write (Note 3)	Load Buffer	Data = Data to Program Address = 1ST Word Addr .
Standby	Increment Count	X = X+1
Standby	Buffer Full?	X = 512? Yes = Read SR [0] No = Load Next Data Word
Read	Status Register	Data = Status Reg . data Address = 1ST Word Addr .
Standby	Program Done?	Check SR[0]: 0 = Program Done 1 = Program in Progress
Standby	Last Data?	No = Fill buffer again Yes = Exit
Write	Exit Prog & Verify Phase	Data = 0xFFFF @ address not in current block

BEFP Exit

Bus State	Operation	Comments
Read	Status Register	Data = Status Reg . Data Address = 1ST Word Addr
Standby	Check Exit Status	Check SR[7]: 0 = Exit Not Completed 1 = Exit Completed

Repeat for subsequent blocks ;

After BEFP exit , a full Status Register check can determine if any program error occurred ;

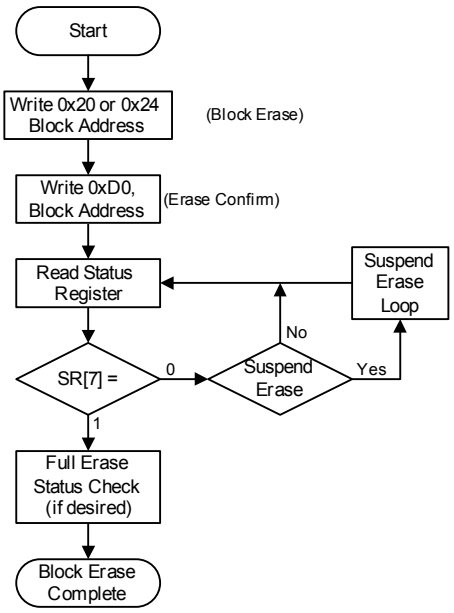
See full Status Register check procedure in the Word Program flowchart .

Write 0xFF to enter Read Array state .

NOTES:
1. BEFP is available in the main array only .
2. First-word address to be programmed within the target block must be aligned on a write -buffer boundary .
3. Write-buffer contents are programmed sequentially to the flash array starting at the first word address ; WSM internally increments addressing .

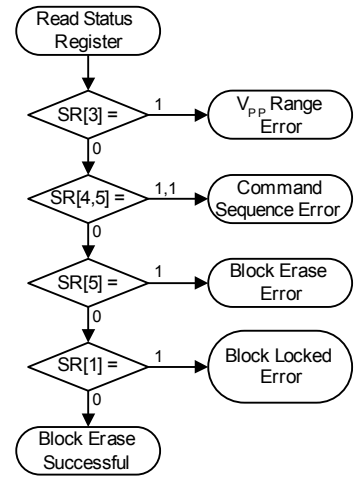
Figure 61. Block Erase for Main Array and EFA Flowchart

BLOCK ERASE PROCEDURE



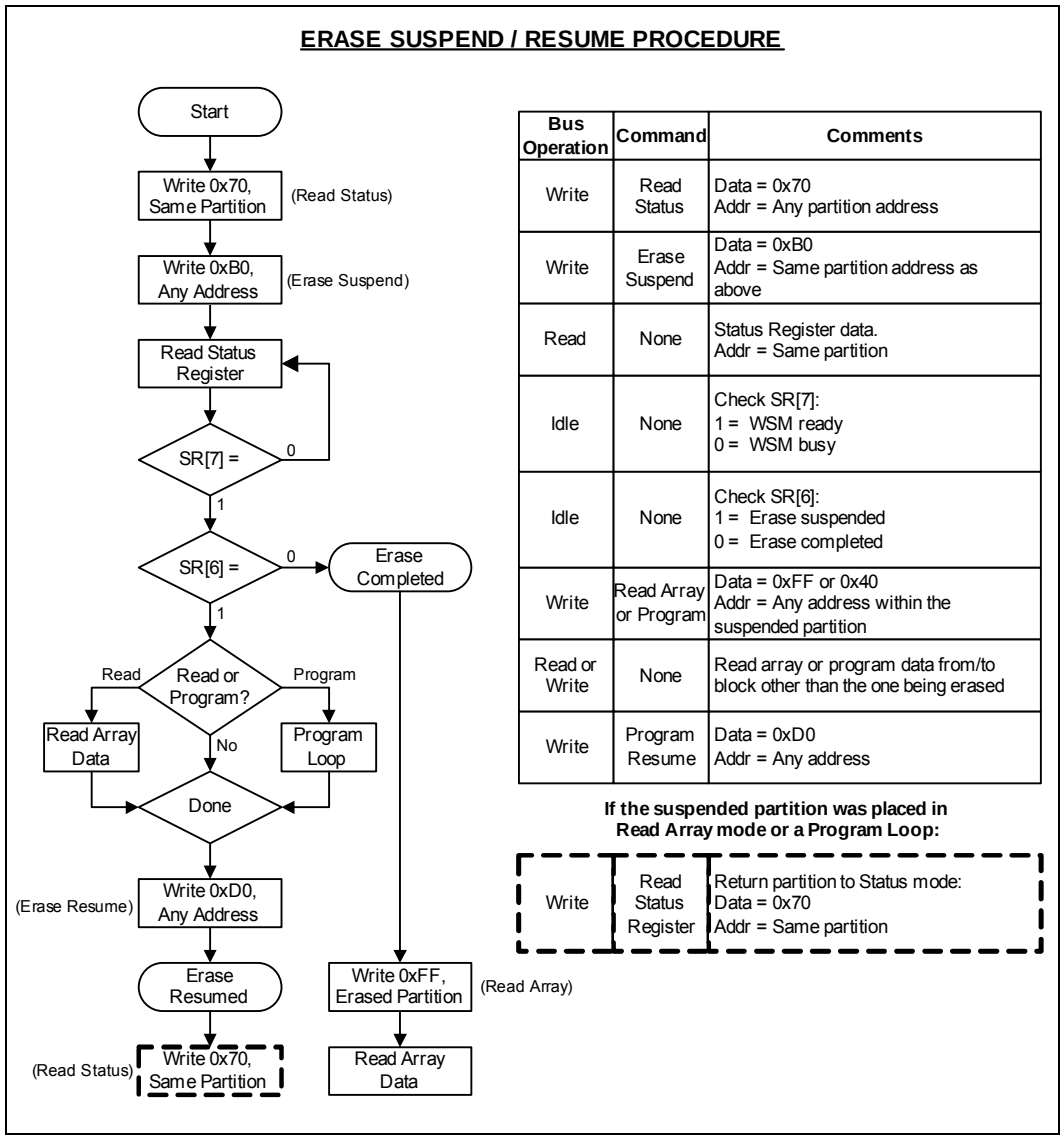
Bus Operation	Command	Comments
Write	Block Erase Setup	Data = 0x20 or 0x24 Addr = Block to be erased (BA)
Write	Erase Confirm	Data = 0xD0 Addr = Block to be erased (BA)
Read	None	Status Register data.
Idle	None	Check SR[7]: 1 = WSM ready 0 = WSM busy
Repeat for subsequent block erasures. Full Status register check can be done after each block erase or after a sequence of block erasures. Write 0xFF after the last operation to enter read array mode.		

FULL ERASE STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Idle	None	Check SR[3]: 1 = V_{PP} Range Error
Idle	None	Check SR[4,5]: Both 1 = Command Sequence Error
Idle	None	Check SR[5]: 1 = Block Erase Error
Idle	None	Check SR[1]: 1 = Attempted erase of locked block; erase aborted.
SR[1,3] must be cleared before the Write State Machine will allow further erase attempts. Only the Clear Status Register command clears SR[1, 3, 4, 5]. If an error is detected, clear the Status register before attempting an erase retry or other error recovery.		

Figure 62. Erase Suspend/Resume Flowchart

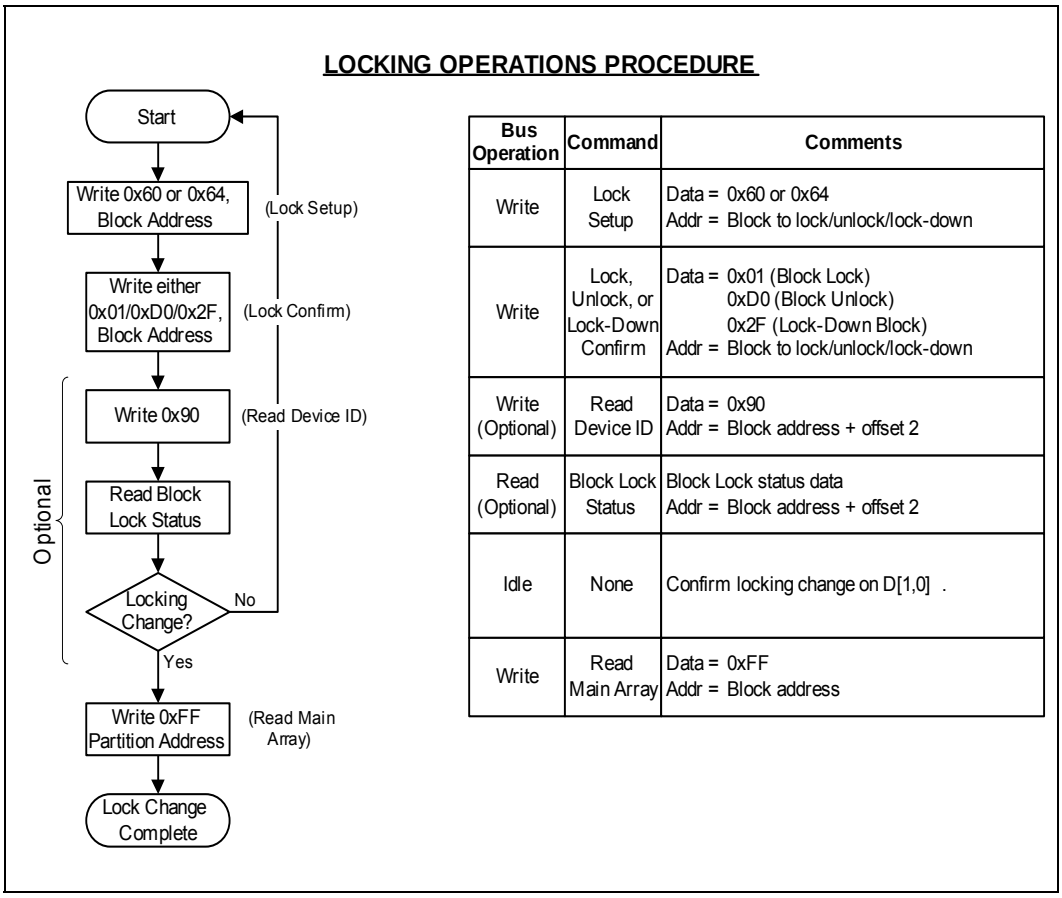


Bus Operation	Command	Comments
Write	Read Status	Data = 0x70 Addr = Any partition address
Write	Erase Suspend	Data = 0xB0 Addr = Same partition address as above
Read	None	Status Register data. Addr = Same partition
Idle	None	Check SR[7]: 1 = WSM ready 0 = WSM busy
Idle	None	Check SR[6]: 1 = Erase suspended 0 = Erase completed
Write	Read Array or Program	Data = 0xFF or 0x40 Addr = Any address within the suspended partition
Read or Write	None	Read array or program data from/to block other than the one being erased
Write	Program Resume	Data = 0xD0 Addr = Any address

If the suspended partition was placed in Read Array mode or a Program Loop:

Write	Read Status Register	Return partition to Status mode: Data = 0x70 Addr = Same partition

Figure 63. Main Array and EFA Block Lock Operations Flowchart



Bus Operation	Command	Comments
Write	Lock Setup	Data = 0x60 or 0x64 Addr = Block to lock/unlock/lock-down
Write	Lock, Unlock, or Lock-Down Confirm	Data = 0x01 (Block Lock) 0xD0 (Block Unlock) 0x2F (Lock-Down Block) Addr = Block to lock/unlock/lock-down
Write (Optional)	Read Device ID	Data = 0x90 Addr = Block address + offset 2
Read (Optional)	Block Lock Status	Block Lock status data Addr = Block address + offset 2
Idle	None	Confirm locking change on D[1,0] .
Write	Read Main Array	Data = 0xFF Addr = Block address

Figure 64. Protection Register Programming Flowchart

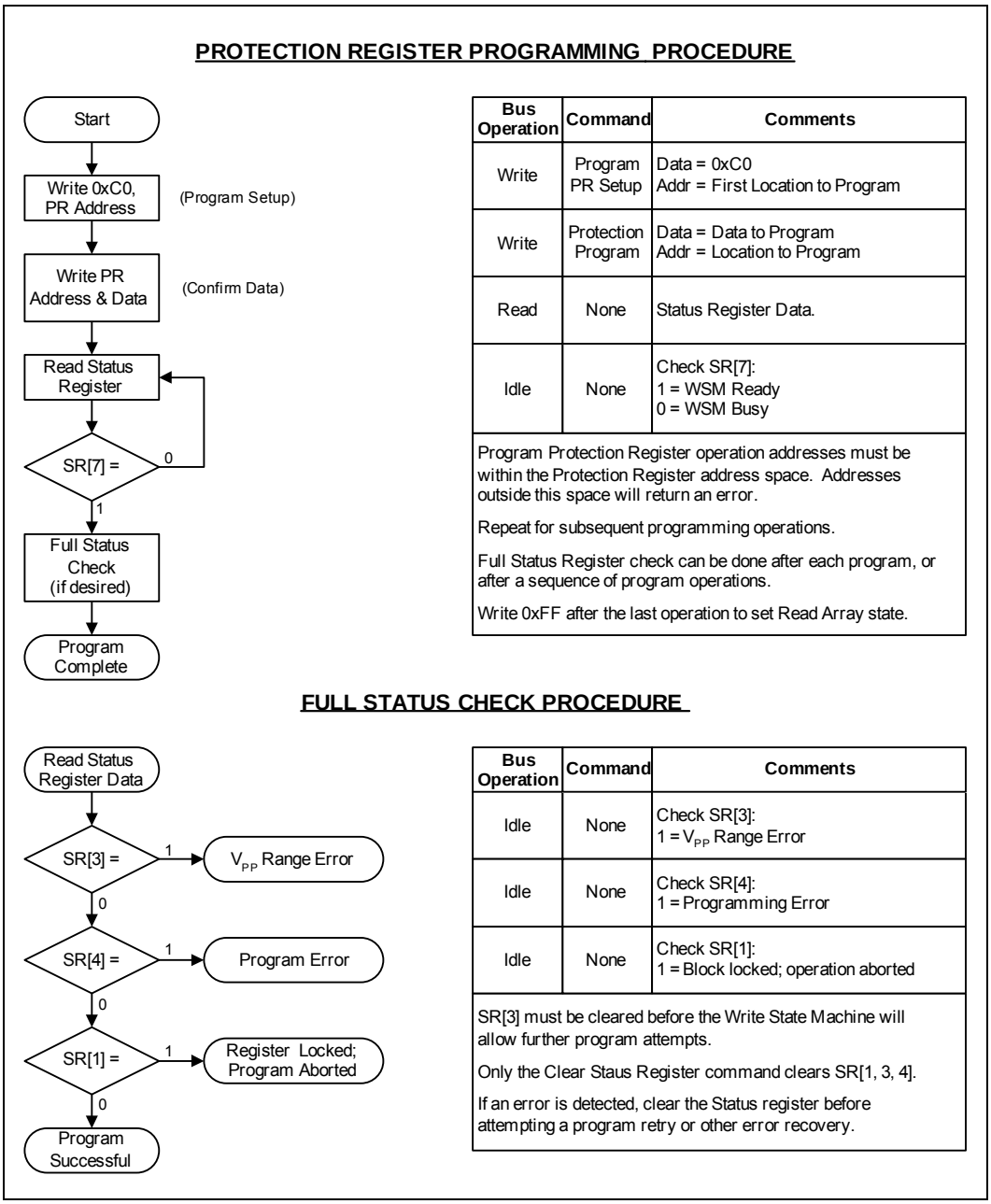
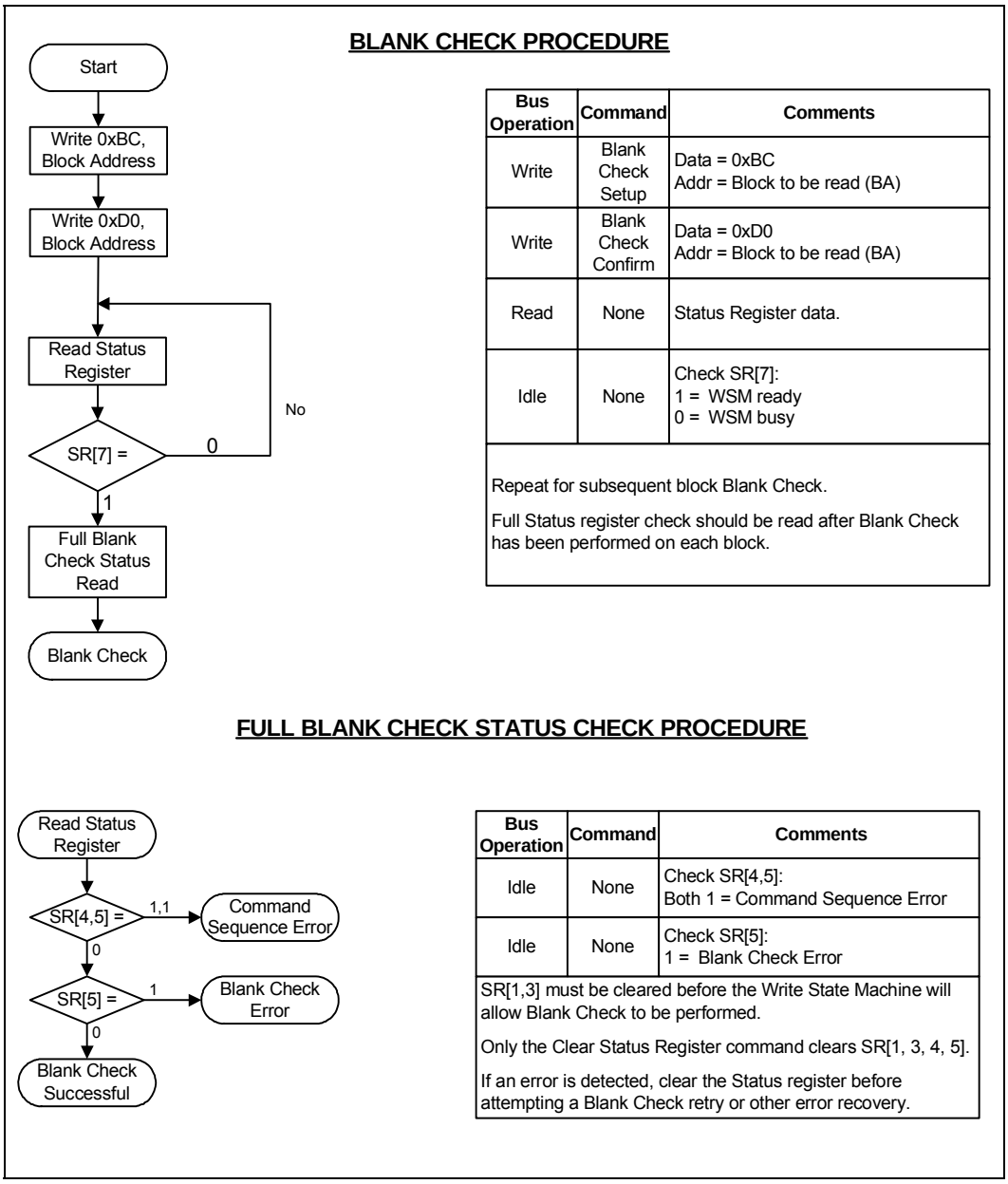


Figure 65. Blank Check Operation Flowchart



Bus Operation	Command	Comments
Write	Blank Check Setup	Data = 0xBC Addr = Block to be read (BA)
Write	Blank Check Confirm	Data = 0xD0 Addr = Block to be read (BA)
Read	None	Status Register data.
Idle	None	Check SR[7]: 1 = WSM ready 0 = WSM busy

Repeat for subsequent block Blank Check.

Full Status register check should be read after Blank Check has been performed on each block.

Bus Operation	Command	Comments
Idle	None	Check SR[4,5]: Both 1 = Command Sequence Error
Idle	None	Check SR[5]: 1 = Blank Check Error

SR[1,3] must be cleared before the Write State Machine will allow Blank Check to be performed.

Only the Clear Status Register command clears SR[1, 3, 4, 5].

If an error is detected, clear the Status register before attempting a Blank Check retry or other error recovery.

Appendix D Common Flash Interface

The Common Flash Interface (CFI) is part of an overall specification for multiple command-set and control-interface descriptions. This appendix describes the database structure containing the data returned by a read operation after issuing the CFI Query command (see Section 9.5.4, "CFI Query" on page 78). System software can parse this database structure to obtain information about the flash device, such as block size, density, bus width, and electrical specifications. The system software will then know which command set(s) to use to properly perform flash writes, block erases, reads and otherwise control the flash device.

D.2 Query Structure Output

The Query database allows system software to obtain information for controlling the flash device. This section describes the device's CFI-compliant interface that allows access to Query data.

Query data are presented on the lowest-order data outputs (A/DQ_{7-0}) only. The numerical offset value is the address relative to the maximum bus width supported by the device. On this family of devices, the Query table device starting address is a 10h, which is a word address for x16 devices.

For a word-wide (x16) device, the first two Query-structure bytes, ASCII "Q" and "R," appear on the low byte at word addresses 10h and 11h. This CFI-compliant device outputs 00h data on upper bytes. The device outputs ASCII "Q" in the low byte (A/DQ_{7-0}) and 00h in the high byte (A/DQ_{15-8}).

At Query addresses containing two or more bytes of information, the least significant data byte is presented at the lower address, and the most significant data byte is presented at the higher address.

In all of the following tables, addresses and data are represented in hexadecimal notation, so the "h" suffix has been dropped. In addition, since the upper byte of word-wide devices is always "00h," the leading "00" has been dropped from the table notation and only the lower byte value is shown. Any x16 device outputs can be assumed to have 00h on the upper byte in this mode.

Table 44. Summary of Query Structure Output as a Function of Device and Mode

Device	Hex Offset	Hex Code	ASCII
Device Addresses	00010:	51	"Q"
	00011:	52	"R"

Table 45. Example of Query Structure Output of x16 Devices

Word Addressing:			Byte Addressing:		
Offset	**Hex Code**	**Value**	**Offset**	**Hex Code**	**Value**
A_X–A_0	**D_{15}–D_0**		**A_X–A_0**	**D_7–D_0**	
00010h	0051	"Q"	00010h	51	"Q"
00011h	0052	"R"	00011h	52	"R"
00012h	0059	"Y"	00012h	59	"Y"
00013h	P_ID_{LO}	PrVendor	00013h	P_ID_{LO}	PrVendor
00014h	P_ID_{HI}	ID #	00014h	P_ID_{LO}	ID #
00015h	P_{LO}	PrVendor	00015h	P_ID_{HI}	ID #
00016h	P_{HI}	TblAdr	00016h	...	...
00017h	A_ID_{LO}	AltVendor	00017h		
00018h	A_ID_{HI}	ID #	00018h		

D.3 Block Status Register

The Block Status Register indicates whether an erase operation completed successfully or whether a given block is locked or can be accessed for flash program/erase operations.

Block Erase Status (BSR[1]) allows system software to determine the success of the last block erase operation. BSR[1] can be used just after power-up to verify that the VCC supply was not accidentally removed during an erase operation. Only issuing another operation to the block resets this bit. The Block Status Register is accessed from word address 02h within each block.

Table 46. Block Status Register

Offset	Length	Description	Add.	Value
(BA+2)h[1]	1	Block Lock Status Register	BA+2	–00 or –01
		BSR.0 Block lock status 0 = Unlocked 1 = Locked	BA+2	(bit 0): 0 or 1
		BSR.1 Block lock-down status 0 = Not locked down 1 = Locked down	BA+2	(bit 1): 0 or 1
		BSR.4 EFA Block lock status 0 = Unlocked 1 = Locked	BA+2	(bit 4): 0 or 1
		BSR.5 EFA Block lock-down status 0 = Not locked down 1 = Locked down	BA+2	(bit 5): 0 or 1
		BSR 2–3, 6-7: Reserved for future use	BA+2	(bit 2–3, 6-7): 0

1. BA = The beginning location of a Block Address (i.e., 020000h is block 1's (256KB block) beginning location in word mode)

D.4 CFI Query Identification String

The Identification String provides verification that the component supports the Common Flash Interface specification. It also indicates the specification version and supported vendor-specified command set(s).

Table 47. CFI Identification

Offset	Length	Description	Add.	Hex Code	Value
10h	3	Query-unique ASCII string “QRY“	10: 11: 12:	--51 --52 --59	"Q" "R" "Y"
13h	2	Primary vendor command set and control interface ID code. 16-bit ID code for vendor-specified algorithms	13: 14:	--00 --02	
15h	2	Extended Query Table primary algorithm address	15: 16:	--0A --01	
17h	2	Alternate vendor command set and control interface ID code. 0000h means no second vendor-specified algorithm exists	17: 18:	--00 --00	
19h	2	Secondary algorithm Extended Query Table address. 0000h means none exists	19: 1A:	--00 --00	

Table 48. System Interface Information

Offset	Length	Description	Add.	Hex Code	Value
1Bh	1	V_{CC} logic supply minimum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 BCD volts	1B:	--17	1.7V
1Ch	1	V_{CC} logic supply maximum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 BCD volts	1C:	--20	2.0V
1Dh	1	V_{PP} [programming] supply minimum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 HEX volts	1D:	--85	8.5V
1Eh	1	V_{PP} [programming] supply maximum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 HEX volts	1E:	--95	9.5V
1Fh	1	“n” such that typical single word program time-out = 2^n µ-sec	1F:	--06	64µs
20h	1	“n” such that typical full buffer write time-out = 2^n µ-sec	20:	--0B	2048µs
21h	1	“n” such that typical block erase time-out = 2^n m-sec	21:	--0A	1s
22h	1	“n” such that typical full chip erase time-out = 2^n m-sec	22:	--00	NA
23h	1	“n” such that maximum word program time-out = 2^n times typical	23:	--02	256µs
24h	1	“n” such that maximum buffer write time-out = 2^n times typical	24:	--02	8192µs
25h	1	“n” such that maximum block erase time-out = 2^n times typical	25:	--02	4s
26h	1	“n” such that maximum chip erase time-out = 2^n times typical	26:	--00	NA

D.5 Device Geometry Definition

Table 49. Device Geometry Definition

Offset	Length	Description	Code		
27h	1	"n" such that device size = 2^n in number of bytes	27:	See table below	
28h	2	Flash device interface code assignment: "n" such that n+1 specifies the bit field that represents the flash device width capabilities as described in the table: 7 6 5 4 3 2 1 0 — — — — x64 x32 x16 x8 15 14 13 12 11 10 9 8 — — — — — — — —	28: 29:	--01 --00	x16
2Ah	2	"n" such that maximum number of bytes in write buffer = 2^n	2A: 2B:	--0A --00	1024
2Ch	1	Number of erase block regions (x) within device: 1. x = 0 means no erase blocking; the device erases in bulk 2. x specifies the number of device regions with one or more contiguous same-size erase blocks. 3. Symmetrically blocked partitions have one blocking region	2C:	See table below	
2Dh	4	Erase Block Region 1 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes	2D: 2E: 2F: 30:	See table below	
31h	4	Reserved for future erase block region information	31: 32: 33: 34:	See table below	
35h	4	Reserved for future erase block region information	35: 36: 37: 38:	See table below	

Figure 66. Device Geometry Definition (Continued)

Address	256 Mbit		512 Mbit	
	–B	–T	–B	–T
27:	--19		--1A	
28:	--01		--01	
29:	--00		--00	
2A:	--0A		--0A	
2B:	--00		--00	
2C:	--01		--01	
2D:	--7F		--FF	
2E:	--00		--00	
2F:	--00		--00	
30:	--04		--04	

D.6 Intel-Specific Extended Query Table

Table 50. Primary Vendor-Specific Extended Query

Offset[1] P = 10Ah	Length	Description (Optional flash features and commands)	Add.	Hex Code	Value
(P+0)h	3	Primary extended query table	10A	--50	"P"
(P+1)h		Unique ASCII string "PRI"	10B:	--52	"R"
(P+2)h			10C:	--49	"I"
(P+3)h	1	Major version number, ASCII	10D:	--31	"1"
(P+4)h	1	Minor version number, ASCII	10E:	--34	"4"
				--E6 (non-Mux)	
(P+5)h	4	Optional feature and command support (1=yes, 0=no)	10F:	--66 (AD-Mux)	
(P+6)h		*bits 10–31 are reserved; undefined bits are "0." If bit 31 is*	110:	--07	
(P+7)h		*"1" then another 31 bit field of Optional features follows at*	111:	--00	
(P+8)h		*the end of the bit–30 field.*	112:	--00	
		bit 0 Chip erase supported		bit 0 = 0	No
		bit 1 Suspend erase supported		bit 1 = 1	Yes
		bit 2 Suspend program supported		bit 2 = 1	Yes
		bit 3 Legacy lock/unlock supported		bit 3 = 0	No
		bit 4 Queued erase supported		bit 4 = 0	No
		bit 5 Instant individual block locking supported		bit 5 = 1	Yes
		bit 6 OTP bits supported		bit 6 = 1	Yes
		bit 7 Pagemode read supported		bit 7 = 0	No (AD-Mux) Yes (Non-Mux)
		bit 8 Synchronous read supported		bit 8 = 1	Yes
		bit 9 Simultaneous operations supported		bit 9 = 1	Yes
		bit 10 Extended Flash Array Blocks supported		bit 10 = 1	Yes
		bit 30 CFI Link(s) to follow		bit 30 = 0	No
		bit 31 Another "Optional Features" field to follow		bit 31 = 0	No
(P+9)h	1	Supported functions after suspend: read Array, Status, Query	113:	--01	
		Other supported operations are:			
		bits 1–7 reserved; undefined bits are "0"			
		bit 0 Program supported after erase suspend		bit 0 = 1	Yes
(P+A)h	2	Block lock status register mask	114:	--33	
(P+B)h		*bits 2-3, 6-15 are Reserved; undefined bits are "0"*	115:	--00	
		bit 0 Block Lock-Bit Status register active		bit 0 = 1	Yes
		bit 1 Block Lock-Down Bit Status active		bit 1 = 1	Yes
		bit 4 EFA Block Lock-Bit Status register active		bit 4 = 1	Yes
		bit 5 EFA Block Lock-Down Bit Status active		bit 5 = 1	Yes
(P+C)h	1	V_{CC} logic supply highest performance program/erase voltage	116:	--18	1.8V
		bits 0–3 BCD value in 100 mV			
		bits 4–7 BCD value in volts			
(P+D)h	1	V_{PP} optimum program/erase supply voltage	117:	--90	9.0V
		bits 0–3 BCD value in 100 mV			
		bits 4–7 HEX value in volts			

Table 51. OTP Register Information

P = 10Ah		(Optional flash features and commands)	Add.	Code	Value
(P+E)h	1	Number of OTP register fields in JEDEC ID space. "00h," indicates that 256 OTP fields are available	118:	--02	2
(P+F)h	4	OTP Field 1: OTP Description	119:	--80	80h
(P+10)h		This field describes user-available One Time Programmable	11A:	--00	00h
(P+11)h		(OTP) register bytes. Some are pre-programmed	11B:	--03	8 byte
(P+12)h		with device-unique serial numbers. Others are user programmable. Bits 0–15 point to the OTP register Lock byte, the section's first byte. The following bytes are factory pre-programmed and user-programmable. bits 0–7 = Lock/bytes Jedec-plane physical low address bits 8–15 = Lock/bytes Jedec-plane physical high address bits 16–23 = "n" such that 2^n = factory pre-programmed bytes bits 24–31 = "n" such that 2^n = user programmable bytes	11C:	--03	8 byte
(P+13)h	10	OTP Field 2: OTP Description	11D:	--89	89h
(P+14)h		Bits 0–31 point to the OTP register physical Lock-word address in the Jedec-plane.	11E:	--00	00h
(P+15)h			11F:	--00	00h
(P+16)h		Following bytes are factory or user-programmable.	120:	--00	00h
(P+17)h		bits 32–39 = "n" € n = factory pgm'd groups (low byte)	121:	--00	0
(P+18)h		bits 40–47 = "n" € n = factory pgm'd groups (high byte)	122:	--00	0
(P+19)h		bits 48–55 = "n" \ 2n = factory programmable bytes/group	123:	--00	0
(P+1A)h		bits 56–63 = "n" € n = user pgm'd groups (low byte)	124:	--10	16
(P+1B)h		bits 64–71 = "n" € n = user pgm'd groups (high byte)	125:	--00	0
(P+1C)h		bits 72–79 = "n" € 2^n = user programmable bytes/group	126:	--04	16

Table 52. Burst Read Information

Offset[1] P = 10Ah	Length	Description (Optional flash features and commands)	Add.	Hex Code	Value
(P+1D)h	1	Page Mode Read capability bits 0–7 = "n" such that 2^n HEX value represents the number of read-page bytes. See offset 28h for device word width to determine page-mode data output width. 00h indicates no read page buffer.	127:	 --05 (Non-Mux) --00 (AD-Mux)	 32-byte (Non-Mux) 0 (AD-Mux)
(P+1E)h	1	Number of synchronous mode read configuration fields that follow. 00h indicates no burst capability.	128:	--03	3
(P+1F)h	1	Synchronous mode read capability configuration 1 Bits 3–7 = Reserved bits 0–2 "n" such that 2^{n+1} HEX value represents the maximum number of continuous synchronous reads when the device is configured for its maximum word width. A value of 07h indicates that the device is capable of continuous linear bursts that will output data until the internal burst counter reaches the end of the device's burstable address space. This field's 3-bit value can be written directly to the Read Configuration Register bits 0–2 if the device is configured for its maximum word width. See offset 28h for word width to determine the burst data output width.	129:	--02	8
(P+20)h	1	Synchronous mode read capability configuration 2	12A:	--03	16
(P+21)h	1	Synchronous mode read capability configuration 3	12B:	--07	Cont

Table 53. Partition and Erase Block Information

Offset[1] P = 10Ah Bottom	Offset[1] P = 10Ah Top	Description (Optional flash features and commands)	See table below Len	See table below Address Bot	See table below Address Top
(P+22)h	(P+22)h	Number of device hardware-partition regions within the device. x = 0: a single hardware partition device (no fields follow). x specifies the number of device partition regions containing one or more contiguous erase block regions.	1	12C:	12C:

Table 54. Partition Region 1 Information

(P+23)h	(P+23)h	Data size of this Parition Region Information field	**2**	12D:	12D
(P+24)h	(P+24)h	(# addressable locations, including this field)		12E	12E
(P+25)h	(P+25)h	Number of identical partitions within the partition region	2	12F:	12F:
(P+26)h	(P+26)h			130:	130:
(P+27)h	(P+27)h	Number of program or erase operations allowed in a partition bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	131:	131:
(P+28)h	(P+28)h	Simultaneous program or erase operations allowed in other partitions while a partition in this region is in Program mode bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	132:	132:
(P+29)h	(P+29)h	Simultaneous program or erase operations allowed in other partitions while a partition in this region is in Erase mode bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	133:	133:
(P+2A)h	(P+2A)h	Types of erase block regions in this Partition Region. x = 0 = no erase blocking; the Partition Region erases in bulk x = number of erase block regions w / contiguous same-size erase blocks. Symmetrically blocked partitions have one blocking region. Partition size = (Type 1 blocks)x(Type 1 block sizes) + (Type 2 blocks)x(Type 2 block sizes) +... + (Type n blocks)x(Type n block sizes)	1	134:	134:
(P+2B)h	(P+2B)h	Partition Region 1 Erase Block Type 1 Information	4	135:	135:
(P+2C)h	(P+2C)h	bits 0–15 = y, y+1 = # identical-size erase blks in a partition		136:	136:
(P+2D)h	(P+2D)h	bits 16–31 = z, region erase block(s) size are z x 256 bytes		137:	137:
(P+2E)h	(P+2E)h			138:	138:
(P+2F)h	(P+2F)h	Partition 1 (Erase Block Type 1)	2	139:	139:
(P+30)h	(P+30)h	Block erase cycles x 1000		13A:	13A:
(P+31)h	(P+31)h	Partition 1 (erase block Type 1) bits per cell; internal EDAC bits 0–3 = bits per cell in erase region bit 4 = internal EDAC used (1=yes, 0=no) bits 5–7 = reserve for future use	1	13B:	13B:
(P+32)h	(P+32)h	Partition 1 (erase block Type 1) page mode and synchronous mode capabilities defined in Table 10. bit 0 = page-mode host reads permitted (1=yes, 0=no) bit 1 = synchronous host reads permitted (1=yes, 0=no) bit 2 = synchronous host writes permitted (1=yes, 0=no) bits 3–7 = reserved for future use	1	13C:	13C:
		Partition Region 1 (Erase Block Type 1) Programming Region Information	6		
(P+33)h	(P+33)h	bits 0–7 = x, 2^x = Programming Region aligned size (**bytes**)		13D:	13D:
(P+34)h	(P+34)h	bits 8–14 = Reserved; bit 15 = Legacy flash operation (ignore 0:7)		13E:	13E:
(P+35)h	(P+35)h	bits 16–23 = y = Control Mode **valid** size in bytes		13F:	13F:
(P+36)h	(P+36)h	bits 24-31 = Reserved		140:	140:
(P+37)h	(P+37)h	bits 32-39 = z = Control Mode **invalid** size in bytes		141:	141:
(P+38)h	(P+38)h	bits 40-46 = Reserved; bit 47 = Legacy flash operation (ignore 23:16 & 39:32)		142:	142:

Table 55. Extended Flash Array Partition and Erase Block Information

Offset(1) 0 Bottom	Offset(1) 0 Top	Description (Optional flash features and commands)	See table below Len	See table below Address Bot	See table below Address Top
(P+39)h	(P+39)h	Number of device hardware-partition regions within the device. x = 0: a single hardware partition device (no fields follow). x specifies the number of device partition regions containing one or more contiguous erase block regions.	1	143:	143:

Figure 67. Extended Flash Array Partition Region 1 Information

(P+3A)h (P+3B)h	(P+3A)h (P+3B)h	Data size of this Parition Region Information field (# addressable locations, including this field)	**2**	144: 145	144 145
(P+3C)h (P+3D)h	(P+3C)h (P+3D)h	Number of identical partitions within the partition region	2	146: 147:	146: 147:
(P+3E)h	(P+3E)h	Number of program or erase operations allowed in a partition bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	148:	148:
(P+3F)h	(P+3F)h	Simultaneous program or erase operations allowed in other partitions while a partition in this region is in Program mode bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	149:	149:
(P+40)h	(P+40)h	Simultaneous program or erase operations allowed in other partitions while a partition in this region is in Erase mode bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	14A:	14A:
(P+41)h	(P+41)h	Types of erase block regions in this Partition Region. x = 0 = no erase blocking; the Partition Region erases in bulk x = number of erase block regions w/ contiguous same-size erase blocks. Symmetrically blocked partitions have one blocking region. Partition size = (Type 1 blocks)x(Type 1 block sizes) + (Type 2 blocks)x(Type 2 block sizes) +…+ (Type n blocks)x(Type n block sizes)	1	14B:	14B:
(P+42)h (P+43)h (P+44)h (P+45)h	(P+42)h (P+43)h (P+44)h (P+45)h	EFA Partition Region Erase Block Type 1 Information bits 0–15 = y, y+1 = # identical-size erase blks in a partition bits 16–31 = z, region erase block(s) size are z x 256 bytes	4	14C: 14D: 14E: 14F:	14C: 14D: 14E: 14F:
(P+46)h (P+47)h	(P+46)h (P+47)h	EFA (Erase block Type 1) Block erase cycles x 1000	2	150: 151:	150: 151:
(P+48)h	(P+48)h	EFA (erase block Type 1) bits per cell; internal EDAC bits 0–3 = bits per cell in erase region bit 4 = internal EDAC used (1=yes, 0=no) bits 5–7 = reserve for future use	1	152:	152:
(P+49)h	(P+49)h	EFA (erase block Type 1) pagemode and synchronous mode capabilities as defined in Table 10. bit 0 = page-mode host reads permitted (1=yes, 0=no) bit 1 = synchronous host reads permitted (1=yes, 0=no) bit 2 = synchronous host writes permitted (1=yes, 0=no) bits 3–7 = reserved for future use	1	153:	153:
		EFA (Erase Block Type 1) Programming Region Information	4		
(P+4A)h	(P+4A)h	bits 0–7 = y, 2^y = Programming Region aligned size (**bytes**)		154:	154:
(P+4B)h	(P+4B)h	bits 8–14 = Reserved; bit 15 = Legacy flash operation (ignore 0:7)		155:	155:
(P+4C)h	(P+4C)h	bits 16–23 = y = Control Mode **valid** size in bytes		156:	156:
(P+4D)h	(P+4D)h	bits 24-31 = Reserved		157:	157:
(P+4E)h	(P+4E)h	bits 32-39 = z = Control Mode **invalid** size in bytes		158:	158:
(P+4F)h	(P+4F)h	bits 40-46 = Reserved; bit 47 = Legacy flash operation (ignore 23:16 & 39:32)		159:	159:

Table 56. Partition and Erase Block Region Information

Address	256 Mbit		512 Mbit	
	–B	–T	–B	–T
12C:	--01		--01	
12D:	--16		--16	
12E:	--00		--00	
12F:	--08		--08	
130:	--00		--00	
131:	--11		--11	
132:	--00		--00	
133:	--00		--00	
134:	--01		--01	
135:	--0F		--1F	
136:	--00		--00	
137:	--00		--00	
138:	--04		--04	
139:	--64		--64	
13A:	--00		--00	
13B:	--12		--12	
13C:	--02 (AD-Mux) --03 (Non-Mux)		--02 (AD-Mux) --03 (Non-Mux)	
13D:	--0A		--0A	
13E:	--00		--00	
13F:	--10		--10	
140:	--00		--00	
141:	--10		--10	
142:	--00		--00	
143:	--01		--01	
144:	--16		--16	
145:	--00		--00	
146:	--01		--01	
147:	--00		--00	
148:	--11		--11	
149:	--00		--00	
14A:	--00		--00	
14B:	--01		--01	
14C:	--03		--03	
14D:	--00		--00	
14E:	--20		--20	
14F:	--00		--00	
150:	--64		--64	
151:	--00		--00	
152:	--01		--01	
153:	--02 (AD-Mux) --03 (Non-Mux)		--02 (AD-Mux) --03 (Non-Mux)	
154:	--00		--00	
155:	--80		--80	
156:	--00		--00	
157:	--00		--00	
158:	--00		--00	
159:	--80		--80	

Appendix E Next State Table

Table 57 through Table 62 show the command state transitions (Next State Table) based on incoming commands. Only one partition can be actively programming or erasing at a time. Each partition stays in its last read state (Read Array, Read Device ID, Read CFI, Read EFA or Read Status Register) until a new command changes it. The next state does not depend on the partition's output state.

Table 57. Next State Table (Sheet 1 of 6)

		Command Input to Chip and resulting *Chip* Next State											
Current Chip State (8)		Read Array (3)	Read EFA	Word Program (4,5,12)	Program EFA	Write to Buffered Program (BP)	Erase Setup (4,5,12)	EFA Block Erase Setup	Buffered Enhanced Factory Pgm Setup (4,12)	BE Confirm, Blank Check Confirm P/E Resume, ULB Confirm (9)	BP / Prg / Erase Suspend	Read Status	Clear Status Register (6)
		(FFH)	(94H)	(41H)	(44h)	(E9H)	(20H)	(24H)	(80H)	(D0H)	(B0H)	(70H)	(50H)
Ready		Ready		Program Setup	EFA Program Setup	BP Setup	Erase Setup	EFA Block Erase Setup	BEFP Setup	Ready			
Lock/RCR/ECR Setup		Ready (Lock Error [Botch])								Ready (Unlock Block)	Ready (Lock Error [Botch])		
Lock EFA Block Setup		Ready (Lock Error [Botch])								Ready (Unlock Block)	Ready (Lock Error [Botch])		
OTP	Setup	OTP Busy											
	Busy			IS in OTP Busy	IS in OTP Busy	OTP Busy	IS in OTP Busy			OTP Busy			
	IS in OTP Busy	OTP Busy											
Word Program (or) EFA Word Program	Setup	Word Program Busy											
	Busy	Program Busy		Illegal State (IS) in pgm busy		Program Busy	Illegal State(IS) in pgm busy			Program Busy	Word Pgm Suspend	Word Program Busy	
	Illegal state (IS) in pgm busy	Word Program Busy											
	Suspend	Program Suspend		IS in pgm suspend		Program Suspend	IS in pgm suspend			Program Busy	Word Program Suspend		Word Program Suspend (Error bits cleared)
	Illegal state (IS) in pgm Suspend	Word Program Suspend											
BP	Setup	BP Load 1											
	BP Load 1 (10)	BP Load 2 if w ord count >0, else BP confirm											
	BP Load 2 (10)	BP Confirm if data load in program buffer is complete, ELSE BP load 2											
	BP Confirm	Ready (Error [Botch])								BP Busy	Ready (Error [Botch])		
	BP Busy	BP Busy		IS in BP busy		BP Busy	IS in BP busy			BP Busy	BP Suspend	BP Busy	
	Illegal state in BP busy	BP busy											
	BP Suspend	BP Suspend		Illegal state (IS) in BP suspend		BP Suspend	Illegal state (IS) in BP suspend			BP Busy	BP Suspend		BP Suspend (Error bits cleared)
	Illegal state in BP Suspend	BP Suspend											
Erase (or) EFA Block Erase	Setup	Ready (Error [Botch])								Erase Busy	Ready (Error [Botch])		
	Busy	Erase Busy		Illegal state (IS) in Erase Busy		Erase Busy	Illegal state (IS) in Erase Busy			Erase Busy	Erase Suspend	Erase Busy	
	Illegal state(IS) in Erase Busy	Erase Busy											
	Suspend	Erase Suspend		Word Program Setup in Erase Suspend	EFA Word Program in Erase Suspend	BP Setup in Erase Suspend	IS in Erase Suspend			Erase Busy	Erase Suspend		Erase Suspend (Error bits cleared)
	Illegal state in Erase Suspend	Erase Suspend											

Table 58. Next State Table (Sheet 2 of 6)

Current Chip State [8]		Command Input to Chip and resulting *Chip* Next State											
		Read Array [3]	Read EFA	Word Program [4,5,12]	Program EFA	Write to Buffered Program (BP)	Erase Setup [4,5,12]	EFA Block Erase Setup	Buffered Enhanced Factory Pgm Setup [4,12]	BE Confirm, Blank Check Confirm P/E Resume, ULB Confirm [9]	BP / Prg / Erase Suspend	Read Status	Clear Status Register [6]
		(FFH)	(94H)	(41H)	(44h)	(E9H)	(20H)	(24H)	(80H)	(D0H)	(B0H)	(70H)	(50H)
Word Program in Erase Suspend (or) EFA Word Program in Erase Suspend	Setup	Word Program Busy in Erase Suspend											
	Busy	Word Pgm Busy in Ers Sus		IS in pgm busy in ers sus		Word Pgm Busy in Ers Sus	IS in pgm busy in ers sus			Word Pgm Busy in Ers Sus	Word Program Suspend in Erase Suspend	Word Pgm Busy in Ers Sus	
	Illegal state(IS) in Pgm busy in Erase Suspend	Word Program Busy in Erase Suspend											
	Suspend	Word Program Suspend in Erase Suspend		IS in pgm sus in ers sus		Word Program Suspend in Erase Suspend	IS in pgm sus in ers sus			Word Pgm Busy in Ers Sus	Word Program Suspend in Erase Suspend		Word Program Suspend in erase suspend (Error bits cleared)
	Illegal State in Word Program Suspend in Erase Suspend	Word Program Suspend in Erase Suspend											
BP in Erase Suspend	Setup	BP Load 1											
	BP Load 1 [10]	BP Load 2 if word count >1, else BP confirm											
	BP Load 2 [10]	BP Confirm if data load in program buffer is complete, ELSE BP load 2											
	BP Confirm	Erase Suspend (Error [Botch BP])								BP Busy in Erase Suspend	Erase Suspend (Error [Botch BP])		
	BP Busy	BP Busy in Erase Suspend		IS in BP busy in ers sus		BP Busy in Erase Suspend	Illegal state (IS) in BP busy in Erase sus			BP Busy in Erase Suspend	BP Suspend in Erase Suspend	BP Busy in Erase Suspend	
	Illegal State(IS) in BP Busy in Erase Suspen	BP Busy in Erase Suspend											
	BP Suspend	BP Suspend in Erase Suspend		IS in BP sus in Ers sus		BP Suspend in Erase Suspend	IS in BP sus in Ers sus			BP Busy in Erase Suspend	BP Suspend in Erase Suspend		BP Suspend in Erase Suspend (Error bits cleared)
	Illegal state(IS) in BP Suspend in Erase Suspend	BP Suspend in Erase Suspend											
Lock/RCR/ECR/Lock EFA Block Setup in Erase Suspend		Erase Suspend (Lock Error [Botch])								Erase Suspend (Unlock Blk)	Erase Suspend (Lock Error [Botch])		
Blank Check	Setup	Ready (Error [Botch])								Blank Check Busy	Ready (Error [Botch])		
	Blank Check Busy	Blank Check Busy		IS in Blank Check Busy		Blank Check Busy	IS in Blank Check Busy			Blank Check Busy			
	Illegal state in Blank Check Busy	Blank Check Busy											
Buffered Enhanced Factory Program Mode	Setup	Ready (Error [Botch])								BEFP Loading Data	Ready (Error [Botch])		
	BEFP Busy	BEFP Program and Verify Busy (if Block Address given matches address given on BEFP Setup command). Commands treated as data. (7)											

Table 59. Next State Table (Sheet 3 of 6)

Current Chip State [8]		Command Input to Chip and resulting Chip Next State										
		Read ID/Query	Lock, Unlock, Lock-down, RCR/ECR setup [5]	Lock, Unlock, Lock-down Lock EFA Blocks setup	Blank Check[5]	OTP Setup [5]	Lock Block Confirm [9]	Lock-Down Block Confirm [9]	Write RCR/ECR Confirm [9]	Block Address (≠WA0) [11]	Illegal Cmds or BEFP Data [2]	WSM Operation Completes
		(90H, 98H)	(60H)	(64H)	(BCH)	(C0H)	(01H)	(2FH)	(03H,04H)	(XXXXH)	(all other codes)	
Ready		Ready	Lock/RCR/ECR Setup	Lock EFA Block setup	Blank Check Setup	OTP Setup	Ready			N/A	Ready	N/A
Lock/RCR/ECR Setup		Ready (Lock Error [Botch])				Ready (Lock Error [Botch])	Ready (Lock Block)	Ready (Lock Down Blk)	Ready (Set CR)	N/A	Ready (Lock Error [Botch])	
Lock EFA Block Setup		Ready (Lock Error [Botch])				Ready (Lock Error [Botch])	Ready (Lock Block)	Ready (Lock Down Blk)	Ready (Lock Error [Botch])	N/A	Ready (Lock Error [Botch])	
OTP	Setup	OTP Busy				OTP Busy				N/A	OTP Busy	Ready
	Busy	OTP Busy	IS in OTP Busy			OTP Busy						
	IS in OTP Busy	OTP Busy										
Word Program (or) EFA Word Program	Setup	Word Program Busy				Word Program Busy				N/A	Word Program Busy	N/A
	Busy	Word Program Busy	Illegal State (IS) in word pgm busy			IS in Word Pgm Busy	Word Program Busy			N/A	Word Program Busy	Ready
	Illegal state in pgm busy	Word Program Busy										
	Suspend	Word Program Suspend	IS in pgm suspend			IS in Word Program Suspend	Word Program Suspend			N/A	Word Program Suspend	N/A
	Illegal state (IS) in pgm Suspend	Word Program Suspend										
BP	Setup	BP Load 1										
	BP Load 1	BP Load 2 if word count>0, else BP Confirm										
	BP Load 2	BP Confirm if data load in program buffer is complete, else BP load 2								Ready (Error [Botch])	BP Confirm if data load in program buffer is complete, else BP load 2	
	BP Confirm	Ready (Error [Botch])				Ready (Error [Botch])						
	BP Busy	BP Busy	IS in BP busy			IS in BP Busy	BP Busy			N/A	BP Busy	Ready
	Illegal state in BP busy	BP busy										
	BP Suspend	BP Suspend	Illegal state (IS) in BP suspend			IS in BP suspend	BP suspend			N/A	BP suspend	N/A
	Illegal state in BP Suspend	BP Suspend				BP suspend						
Erase (or) EFA Block Erase	Setup	Ready (Error [Botch])				Ready (Error [Botch])				N/A	Ready (Error [Botch])	Ready
	Busy	Erase Busy	Illegal state (IS) in Erase Busy			IS in Erase Busy	Erase Busy			N/A	Erase Busy	
	Illegal state in Erase Busy	Erase Busy				Erase Busy						
	Suspend	Erase Suspend	Lock/RCR/ECR Setup in Erase Suspend	Lock EFA Block setup in Erase Suspend	Erase Suspend	IS in Erase Suspend	Erase Suspend			N/A	Erase Suspend	N/A
	Illegal state in Erase Suspend	Erase Suspend				Erase Suspend						

Table 60. Next State Table (Sheet 4 of 6)

Current Chip State (8)		Command Input to Chip and resulting Chip Next State										
		Read ID/Query	Lock, Unlock, Lock-down, RCR/ECR setup (5)	Lock, Unlock, Lock-down Lock EFA Blocks setup	Blank Check(5)	OTP Setup (5)	Lock Block Confirm (9)	Lock-Down Block Confirm (9)	Write RCR/ECR Confirm (9)	Block Address (≠WA0) (11)	Illegal Cmds or BEFP Data (2)	WSM Operation Completes
		(90H, 98H)	(60H)	(64H)	(BCH)	(C0H)	(01H)	(2FH)	(03H,04H)	(XXXXH)	(all other codes)	
Word Program in Erase Suspend (or) EFA Word Program in Erase Suspend	Setup	Word Program Busy in Erase Suspend				Word Program Busy in Erase Suspend				N/A	Word Program Busy in Erase Suspend	N/A
	Busy	Word Pgm Busy in Ers Sus	Illegal State in Word Pgm Busy in Erase Suspend			IS in Word Program Busy in Erase Suspend	Word Program Busy in Erase Suspend			N/A	Word Program Busy in Erase Suspend	Erase Suspend
	Illegal state in Pgm busy in Erase Suspend	Word Program Busy in Erase Suspend				Word Program Busy in Erase Suspend				N/A	Word Program Busy in Erase Suspend	IS in Erase Suspend
	Suspend	Word Program Suspend in Erase Suspend	IS in Word Program Suspend in Erase Suspend			IS in Word Program Suspend in Erase Suspend	Word Program Suspend in Erase Suspend			N/A	Word Program Suspend in Erase Suspend	
	Illegal State in Word Program Suspend in Erase Suspend	Word Program Suspend in Erase Suspend				Word Program Suspend in Erase Suspend				N/A	Word Program Suspend in Erase Suspend	
BP in Erase Suspend	Setup	BP Load 1 in Erase Suspend {Give word count load [N-1]}; If N=0 (word count =1) go to BP Confirm; Else N<>0 go to BP Load 2				BP Load 1						N/A
	BP Load 1	BP Load 2 in Erase Suspend (Give data load)				BP Load 2 if word count>1, else BP Confirm						
	BP Load 2	BP Confirm in Erase Suspend when count=0, ELSE BP load 2				BP Confirm if data load in program buffer is complete, else BP load 2				Erase Suspend (Error [Botch BP])	BP Confirm in Erase Suspend when N=0, ELSE BP load 2	
	BP Confirm	Erase Suspend (Error [Botch BP])										
	BP Busy	BP Busy in Erase Suspend	Illegal state (IS) in BP busy in Erase sus			IS in BP Busy in Erase Suspend	BP Busy in Erase Suspend			N/A	BP Busy in Erase Suspend	Erase Suspend
	Illegal State in BP Busy in Erase Suspen	BP Busy in Erase Suspend				BP Busy in Erase Suspend						IS in Erase Suspend
	BP Suspend	BP Suspend in Erase Suspend	IS in BP sus in Ers sus			IS in BP Suspend in Erase Suspend	BP Suspend in Erase Suspend			N/A	BP Suspend in Erase Suspend	
	Illegal state in BP Suspend in Erase Suspend	BP Suspend in Erase Suspend				BP Suspend in Erase Suspend				N/A	BP Suspend in Erase Suspend	N/A
Lock/RCR/ECR Setup in Erase Suspend		Erase Suspend (Lock Error [Botch])				Erase Suspend (Error [Botch])	Erase Suspend (Lock Blk)	Erase Suspend (Lock Down Blk)	Erase Suspend (Set CR)	N/A	Erase Suspend (Lock Error [Botch])	
Blank Check	Setup	Ready (Error [Botch])				Ready (Error [Botch])				N/A	Ready (Error [Botch])	
	Blank Check Busy	Blank Check Busy	IS in Blank Check Busy			IS in Blank Check Busy	Blank Check Busy			N/A	Blank Check Busy	Ready
	Illegal state in Blank Check Busy	Blank Check Busy								N/A	Blank Check Busy	
Buffered Enhanced Factory Program Mode	Setup	Ready (Error [Botch])				Ready (Error [Botch])						N/A
	BEFP Busy	BEFP Program and Verify Busy (if Block Address given matches address given on BEFP Setup command). Commands treated as data. (7)				BEFP Program and Verify Busy (if Block Address given matches address given on BEFP Setup command). Commands treated as data. (7)				Ready	BEFP Busy	Ready

Table 61. Next State Table (Sheet 5 of 6)

Current chip state	Command Input to Chip and resulting *Output* Mux Next State											
	Read Array [3]	Read EFA	Word Program Setup (4,5,12)	EFA Word Program	BP Setup	Erase Setup [4,5,12]	EFA Block Erase Setup	Buffered Enhanced Factory Pgm Setup [4,12]	BE Confirm, Blank Check Confirm, P/E Resume, ULB Confirm [9]	Program/ Erase Suspend	Read Status	Clear Status Register [6]
	(FFH)	(94H)	(41H)	(44h)	(E9H)	(20H)	(24H)	(80H)	(D0H)	(B0H)	(70H)	(50H)
BEFP Setup, BEFP Pgm & Verify Busy, Erase Setup, OTP Setup, BP Confirm, Word Pgm Setup, Word Pgm Setup in Erase Susp, BP Confirm in Erase Suspend Blank Check Setup, Blank Check Busy	Status Read											
EFA Word Pgm Setup, EFA Word Pgm Setup in Erase Susp EFA Block Erase Setup, EFA Block Suspend												
Lock/RCR/ECR Setup, Lock/RCR/ECR Setup in Erase Susp												
EFA Block Lock Setup, EFA Block Lock Setup in Erase Susp												
BP Setup, Load 1, Load 2 BP Setup, Load1, Load 2 - in Erase Susp.	Output MUX does not change											
BP Busy BP Busy in Erase Suspend	Read Array	Read EFA	Status Read	See Note 13	Status Read				Status Read	Output mux does not change.	Status Read	Output mux does not change.
Ready, Word Program Busy, BP Busy, Erase Busy, Word Pgm Suspend, BP Suspend, Erase Suspend, Word Pgm Busy in Erase Suspend, BP Suspend in Erase Suspend									Output mux does not change.			
OTP Busy												

Table 62. Next State Table (Sheet 6 of 6)

Current chip state	Command Input to Chip and resulting *Output* Mux Next State										
	Read ID/Query	Lock, Unlock, Lock-down, RCR/ECR setup [5]	Lock, Unlock, Lock-down Lock EFA Blocks setup	Blank Check[5]	OTP Setup [5]	Lock Block Confirm [9]	Lock-Down Block Confirm [9]	Write RCR/ECR Confirm [9]	Block Address (WA0)	Illegal Cmds or BEFP Data [2]	WSM Operation Completes
	(90H, 98H)	(60H)	(64H)	(BCH)	(C0H)	(01H)	(2FH)	(03H,04H)	(FFFFH)	(all other codes)	
BEFP Setup, BEFP Pgm & Verify Busy, Erase Setup, OTP Setup, BP Confirm, Word Pgm Setup, Word Pgm Setup in Erase Susp, BP Confirm in Erase Suspend Blank Check Setup, Blank Check Busy	Status Read										Output mux does not change
EFA Word Pgm Setup, EFA Word Pgm Setup in Erase Susp EFA Block Erase Setup, EFA Block Suspend											
Lock/RCR/ECR Setup, Lock/RCR/ECR Setup in Erase Susp	Status Read							Array Read	Status Read		
EFA Block Lock Setup, EFA Block Lock Setup in Erase Susp											
BP Setup, Load 1, Load 2 BP Setup, Load1, Load 2 - in Erase Susp.	Output MUX will not change										
BP Busy BP Busy in Erase Suspend	ID/ Query Read	Status Read				Output mux does not change.			Array Read	Output mux does not change.	
Ready, Word Program Busy, BP Busy, Erase Busy, Word Pgm Suspend, BP Suspend, Erase Suspend, Word Pgm Busy in Erase Suspend, BP Suspend in Erase Suspend											
OTP Busy	Status Read										

NOTES:

1. The "Partition Data When Read" field shows what the user will read from the flash chip after issuing the appropriate command given the Partition Address is not changed from the address given during the command. "Read-while-write" functionality gives more flexibility in data output from the device. The data read from the chip depends on the Partition Address applied to the device; Each partition is placed into one of 3 possible output states during commands: Read Array, Read Status or Read ID/CFI, depending on the command given to the chip; This partition's output state is retained until a new command is given to the chip at that Partition Address; For example, this allows the user to set partition #1's output state to Read Array, and partition #4's output state to Read Status; Every time the partition address is changed to partition #4 (without issuing a new command), the Status will be read from the chip.
2. "Illegal commands" include commands outside of the allowed command set (allowed commands: 41H[pgm], 20H [erase], etc.)
3. If a "Read Array" is attempted from a busy partition, the result will be "indeterminate" data. The key point is that the output mux for that partition will be pointing to the "array", but “indeterminate” data will be output. When the user returns to this partition address some time in the future, the output mux will be in the "Read Array" state from its last visit. "Read ID" and "Read Query" commands do the exact same thing in the device. The ID and Query data are located at different locations in the address map.
4. 1st and 2nd cycles of "2 cycles write commands" must be given to the same partition address, or unexpected results will occur.
5. The 2nd cycle of the following 2 cycle commands will be ignored by the user interface: Program Setup, Erase Setup, OTP Setup, Lock/Unlock/Lock-down/RCR/ECR Setup and Blank Check when issued in an "illegal condition". Illegal conditions are such as "pgm setup while busy", "erase setup while busy", etc.
6. The Clear Status command only clears the error bits in the status register if the device is not in these modes: WSM running (Pgm Busy, Erase Busy, OTP Busy, BEFP modes);
7. BEFP writes are only allowed when the status register bit #0 = 0, or else the data is ignored.

8. The "current state" is that of the "chip" and not of the "partition"; each partition "remembers" which output (Array, ID/CFI or Status) it was last pointed to on the last instruction to the "chip", but the next state of the chip does not depend on where the partition's output mux is presently pointing to.
9. Confirm commands (Lock Block, Unlock Block, Lock-Down Block, Configuration Register and Blank Check) perform the operation and then move to the Ready State.
10. Buffered programming will botch when a different block address (as compared to address given with E8 command) is written during the BP Load1 and BP Load2 states
11. WA0 refers to the block address latched during the first write cycle of the current operation
12. All two cycle commands will be considered as a contiguous whole during device suspend states. Individual commands will not be parsed separately; that is, the second cycle of an erase command issued in program suspend will NOT resume the program operation.
13. For M18 108 MHz, output mux changes to Read Status; For M18 133 MHz, output mux does not change.

Appendix F Additional Information

Order Number	Document/Tool
AP-822	Designing with Intel StrataFlash® Wireless Memory and Pre-enabling Intel StrataFlash® Cellular Memory
AP-816	Effect of Program Buffer Size on System Interrupt Latency
AP-841	Intel StrataFlash® Cellular Memory (M18 SCSP) to ARM® PrimeCell™ Design Guide

Notes:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.Intel.com for technical documentation and tools.
3. For the most current information on Intel flash products, visit our website at http://developer.intel.com/design/flash/.

Appendix G Ordering Information

Figure 68 provides the device part number decoder and Table 63 provides the available combinations. For combinations not listed, please contact your local Intel sales office.

Figure 68. M18 Flash memory part number decoder

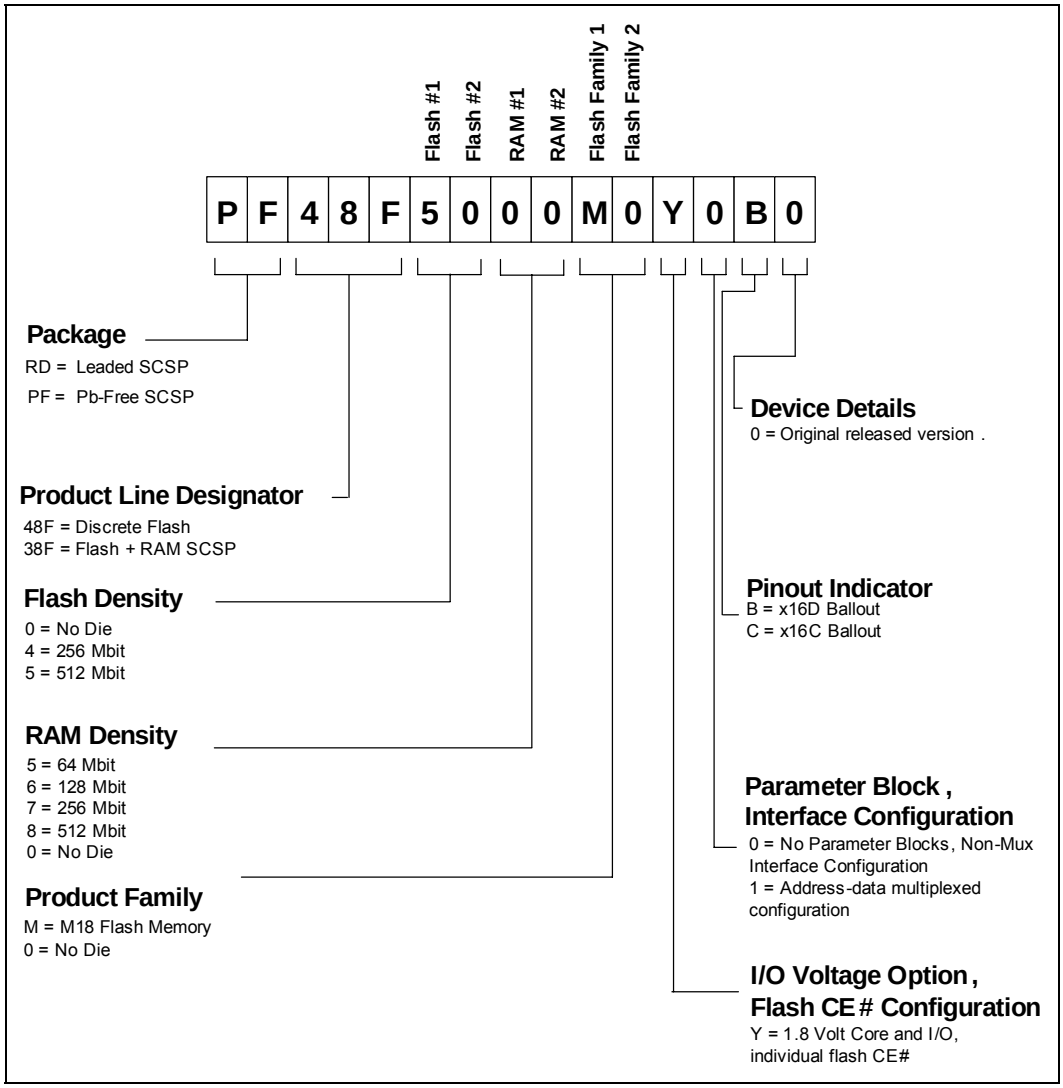


Table 63. Package Ordering Information

I/O Voltage	Flash Component	RAM Component	Package			Part Order Number
(V)	Density in Mbit and Family	Density in Mbit and Type	Size (mm)	Ball Type	Type	
Non-Mux, x16C						
1.8	256 Non-Mux	64 PSRAM	8 x 11 x 1.2	x16C 107-ball	Lead-Free	PF38F4050M0Y0C0
1.8	512 Non-Mux	64 PSRAM	8 x 11 x 1.2	x16C 107-ball	Lead-Free	PF38F5050M0Y0C0
1.8	512 Non-Mux	128 PSRAM	8 x 11 x 1.2	x16C 107-ball	Lead-Free	PF38F5060M0Y0C0
1.8	512 + 512 Non-Mux	128 + 128 PSRAM	8 x 11 x 1.4	x16C 107-ball	Lead-Free	PF38F5566MMY0C0
Non-Mux, x16D						
1.8	512 Non-Mux	128 LPSDRAM	9 x 11 x 1.2	x16D 105-ball	Lead-Free	PF38F5060M0Y0B0
1.8	512 Non-Mux	256 LPSDRAM	9 x 11 x 1.2	x16D 105-ball	Lead-Free	PF38F5070M0Y0B0
1.8	512 + 512 Non-Mux	N/A	8 x 10 x 1.4	x16D 105-ball	Lead-Free	PF48F5500M0Y0B0
Mux, x16D						
1.8	512 + 512 Mux	N/A	8 x 10 x 1.4	x16D 105-ball	Lead-Free	PF48F5500M0Y1B0

Note: To order any of the parts listed above and to obtain a datasheet for the M18 SCSP parts, please contact your local Intel sales office.